Cat. No. W393-E1-02

SYSMAC CJ Series
CJ1G/H-CPU□□H, CJ1G-CPU□□
Programmable Controllers

OPERATION MANUAL

OMRON

SYSMAC CJ Series
CJ1G/H-CPU□□H, CJ1G-CPU□□
Programmable Controllers

Operation Manual

Revised October 2001

Notice:

OMRON products are manufactured for use according to proper procedures by a qualified operator and only for the purposes described in this manual.

The following conventions are used to indicate and classify precautions in this manual. Always heed the information provided with them. Failure to heed precautions can result in injury to people or damage to property.

⚠DANGER Indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.

⚠WARNING Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

⚠Caution Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury, or property damage.

OMRON Product References

All OMRON products are capitalized in this manual. The word “Unit” is also capitalized when it refers to an OMRON product, regardless of whether or not it appears in the proper name of the product.

The abbreviation “Ch,” which appears in some displays and on some OMRON products, often means “word” and is abbreviated “Wd” in documentation in this sense.

The abbreviation “PC” means Programmable Controller and is not used as an abbreviation for anything else.

Visual Aids

The following headings appear in the left column of the manual to help you locate different types of information.

Note Indicates information of particular interest for efficient and convenient operation of the product.

1,2,3... 1. Indicates lists of one sort or another, such as procedures, checklists, etc.

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About this Manual:

This manual describes the installation and operation of the CJ-series Programmable Controllers (PCs) and includes the sections described on the following page. The CS Series and CJ Series are subdivided as shown in the following table.

Unit	CS Series	CJ Series
CPU Units	CS1-H CPU Units: CS1H-CPU□□H CS1G-CPU□□H	CJ1-H CPU Units: CJ1H-CPU□□H CJ1G-CPU□□H
	CS1 CPU Units: CS1H-CPU□□-EV1 CS1G-CPU□□-EV1	CJ1 CPU Units: CJ1G-CPU□□-EV1
Basic I/O Units	CS-series Basic I/O Units	CJ-series Basic I/O Units
Special I/O Units	CS-series Special I/O Units	CJ-series Special I/O Units
CPU Bus Units	CS-series CPU Bus Units	CJ-series CPU Bus Units
Power Supply Units	CS-series Power Supply Units	CJ-series Power Supply Units

Please read this manual and all related manuals listed in the following table and be sure you understand information provided before attempting to install or use CJ1G-CPU□□ or CJ1G/H-CPU□□H CPU Units in a PC System.

Name	Cat. No.	Contents
SYSMAC CJ Series CJ1G/H-CPU□□H CJ1G-CPU□□ Programmable Controllers Operation Manual	W393	Provides an outlines of and describes the design, installation, maintenance, and other basic operations for the CJ-series PCs. (This manual)
SYSMAC CS Series CS1G/H-CPU□□-EV1, CS1G/H-CPU□□H Programmable Controllers Operation Manual	W339	Provides an outlines of and describes the design, installation, maintenance, and other basic operations for the CS-series PCs.
SYSMAC CS/CJ Series CS1G/H-CPU□□-EV1, CS1G/H-CPU□□H, CJ1G-CPU□□, CJ1G/H-CPU□□H Programmable Controllers Programming Manual	W394	This manual describes programming and other methods to use the functions of the CS/CJ-series PCs.
SYSMAC CS/CJ Series CS1G/H-CPU□□H, CS1G/H-CPU□□-EV1, CJ1G-CPU□□, CJ1G/H-CPU□□H Programmable Controllers Programming Manual	W340	Describes the ladder diagram programming instructions supported by CS/CJ-series PCs.
SYSMAC CS/CJ Series CQM1H-PRO01-E, C200H-PRO27-E, CQM1-PRO01-E Programming Consoles Operation Manual	W341	Provides information on how to program and operate CS/CJ-series PCs using a Programming Console.
SYSMAC CS/CJ Series CS1G/H-CPU□□H, CS1G/H-CPU□□-EV1, CJ1G-CPU□□, CJ1G/H-CPU□□H CS1W-SCB21/41, CS1W-SCU21, CJ1W-SCU41 Communications Commands Reference Manual	W342	Describes the C-series (Host Link) and FINS communications commands used with CS/CJ-series PCs.
SYSMAC WS02-CXP□□-E CX-Programmer User Manual	W361	Provide information on how to use the CX-Programmer, a programming device that supports the CS/CJ-series PCs, and the CX-Net contained within CX-Programmer.
SYSMAC WS02-CXP□□-E CX-Server User Manual	W362	
SYSMAC CS/CJ Series CS1W-SCB21/41, CS1W-SCU21, CJ1W-SCU41 Serial Communications Boards/Units Operation Manual	W336	Describes the use of Serial Communications Unit and Boards to perform serial communications with external devices, including the usage of standard system protocols for OMRON products.

Name	Cat. No.	Contents
SYSMAC WS02-PSTC1-E CX-Protocol Operation Manual	W344	Describes the use of the CX-Protocol to create protocol macros as communications sequences to communicate with external devices.
SYSMAC CS/CJ Series CJ1W-ETN01/ENT11, CJ1W-ETN11 Ethernet Unit Operation Manual	W343	Describes the installation and operation of CJ1W-ETN01, CJ1W-ENT11, and CJ1W-ETN11 Ethernet Units.

About this Manual, Continued

This manual contains the following sections.

Section 1 introduces the special features and functions of the CJ-series PCs and describes the differences between these PCs and the earlier CS-series and C200HX/HG/HE PCs.

Section 2 provides tables of standard models, Unit specifications, system configurations, and a comparison between different Units.

Section 3 provides names of Unit components and their functions. Dimensions are also provided.

Section 4 outlines the steps required to assemble and operate a CJ PC system.

Section 5 describes how to install a PC System, including mounting and wiring Units. Follow instructions carefully. Improper installation can cause the PC to malfunction, resulting in very dangerous situations.

Section 6 describes DIP switch settings.

Section 7 describes initial hardware and software settings in the PC Setup.

Section 8 describes I/O allocation to Basic I/O Units, Special I/O Units, and CPU Bus Units, as well as and data exchange with CPU Bus Units.

Section 9 describes the structure and functions of the I/O Memory Areas and Parameter Areas.

Section 10 describes the internal operation of CPU Units and the cycle used for internal processing.

Section 11 provides information on hardware and software errors that occur during PC operation.

Section 12 provides information on hardware maintenance and inspections.

The ***Appendices*** provide Unit specifications, current/power consumptions, Auxiliary Area words and bits, internal I/O addresses, and PC Setup settings, and information on RS-232C ports,.

⚠ **WARNING** Failure to read and understand the information provided in this manual may result in personal injury or death, damage to the product, or product failure. Please read each section in its entirety and be sure you understand the information provided in the section and related sections before attempting any of the procedures or operations given.

PRECAUTIONS

This section provides general precautions for using the CJ-series Programmable Controllers (PCs) and related devices.

The information contained in this section is important for the safe and reliable application of Programmable Controllers. You must read this section and understand the information contained before attempting to set up or operate a PC system.

1 Intended Audience

This manual is intended for the following personnel, who must also have knowledge of electrical systems (an electrical engineer or the equivalent).

- Personnel in charge of installing FA systems.
- Personnel in charge of designing FA systems.
- Personnel in charge of managing FA systems and facilities.

2 General Precautions

The user must operate the product according to the performance specifications described in the operation manuals.

Before using the product under conditions which are not described in the manual or applying the product to nuclear control systems, railroad systems, aviation systems, vehicles, combustion systems, medical equipment, amusement machines, safety equipment, and other systems, machines, and equipment that may have a serious influence on lives and property if used improperly, consult your OMRON representative.

Make sure that the ratings and performance characteristics of the product are sufficient for the systems, machines, and equipment, and be sure to provide the systems, machines, and equipment with double safety mechanisms.

This manual provides information for programming and operating the Unit. Be sure to read this manual before attempting to use the Unit and keep this manual close at hand for reference during operation.

⚠WARNING It is extremely important that a PC and all PC Units be used for the specified purpose and under the specified conditions, especially in applications that can directly or indirectly affect human life. You must consult with your OMRON representative before applying a PC System to the above-mentioned applications.

3 Safety Precautions

⚠WARNING The CPU Unit refreshes I/O even when the program is stopped (i.e., even in PROGRAM mode). Confirm safety thoroughly in advance before changing the status of any part of memory allocated to I/O Units, Special I/O Units, or CPU Bus Units. Any changes to the data allocated to any Unit may result in unexpected operation of the loads connected to the Unit. Any of the following operation may result in changes to memory status.

- Transferring I/O memory data to the CPU Unit from a Programming Device.
- Changing present values in memory from a Programming Device.
- Force-setting/-resetting bits from a Programming Device.
- Transferring I/O memory files from a Memory Card or EM file memory to the CPU Unit.
- Transferring I/O memory from a host computer or from another PC on a network.

⚠WARNING Do not attempt to take any Unit apart while the power is being supplied. Doing so may result in electric shock.

⚠ **WARNING** Do not touch any of the terminals or terminal blocks while the power is being supplied. Doing so may result in electric shock.

⚠ **WARNING** Do not attempt to disassemble, repair, or modify any Units. Any attempt to do so may result in malfunction, fire, or electric shock.

⚠ **WARNING** Do not touch the Power Supply Unit while power is being supplied or immediately after power has been turned OFF. Doing so may result in electric shock.

⚠ **WARNING** Provide safety measures in external circuits (i.e., not in the Programmable Controller), including the following items, to ensure safety in the system if an abnormality occurs due to malfunction of the PC or another external factor affecting the PC operation. Not doing so may result in serious accidents.

- Emergency stop circuits, interlock circuits, limit circuits, and similar safety measures must be provided in external control circuits.
- The PC will turn OFF all outputs when its self-diagnosis function detects any error or when a severe failure alarm (FALS) instruction is executed. As a countermeasure for such errors, external safety measures must be provided to ensure safety in the system.
- The PC outputs may remain ON or OFF due to deposition or burning of the output relays or destruction of the output transistors. As a countermeasure for such problems, external safety measures must be provided to ensure safety in the system.
- When the 24-V DC output (service power supply to the PC) is overloaded or short-circuited, the voltage may drop and result in the outputs being turned OFF. As a countermeasure for such problems, external safety measures must be provided to ensure safety in the system.

⚠ **Caution** Confirm safety before transferring data files stored in the file memory (Memory Card or EM file memory) to the I/O area (CIO) of the CPU Unit using a peripheral tool. Otherwise, the devices connected to the output unit may malfunction regardless of the operation mode of the CPU Unit.

⚠ **Caution** Execute online edit only after confirming that no adverse effects will be caused by extending the cycle time. Otherwise, the input signals may not be readable.

⚠ **Caution** Confirm safety at the destination node before transferring a program to another node or changing contents of the I/O memory area. Doing either of these without confirming safety may result in injury.

⚠ **Caution** Tighten the screws on the terminal block of the AC Power Supply Unit to the torque specified in the operation manual. The loose screws may result in burning or malfunction.

4 Operating Environment Precautions

⚠ **Caution** Do not operate the control system in the following locations:

- Locations subject to direct sunlight.
- Locations subject to temperatures or humidity outside the range specified in the specifications.
- Locations subject to condensation as the result of severe changes in temperature.
- Locations subject to corrosive or flammable gases.
- Locations subject to dust (especially iron dust) or salts.
- Locations subject to exposure to water, oil, or chemicals.
- Locations subject to shock or vibration.

⚠ **Caution** Take appropriate and sufficient countermeasures when installing systems in the following locations:

- Locations subject to static electricity or other forms of noise.
- Locations subject to strong electromagnetic fields.
- Locations subject to possible exposure to radioactivity.
- Locations close to power supplies.

⚠ **Caution** The operating environment of the PC System can have a large effect on the longevity and reliability of the system. Improper operating environments can lead to malfunction, failure, and other unforeseeable problems with the PC System. Be sure that the operating environment is within the specified conditions at installation and remains within the specified conditions during the life of the system.

5 Application Precautions

Observe the following precautions when using the PC System.

- You must use the CX-Programmer (programming software that runs on Windows) if you need to program more than one task. A Programming Console can be used to program only one cyclic task plus interrupt tasks. A Programming Console can, however, be used to edit multitask programs originally created with the CX-Programmer.

⚠ **WARNING** Always heed these precautions. Failure to abide by the following precautions could lead to serious or possibly fatal injury.

- Always connect to a ground of 100 Ω or less when installing the Units. Not connecting to a ground of 100 Ω or less may result in electric shock.
- A ground of 100 Ω or less must be installed when shorting the GR and LG terminals on the Power Supply Unit.
- Always turn OFF the power supply to the PC before attempting any of the following. Not turning OFF the power supply may result in malfunction or electric shock.
  - Mounting or dismounting Power Supply Units, I/O Units, CPU Units, or any other Units.

- Assembling the Units.
- Setting DIP switches or rotary switches.
- Connecting cables or wiring the system.
- Connecting or disconnecting the connectors.

⚠ **Caution** Failure to abide by the following precautions could lead to faulty operation of the PC or the system, or could damage the PC or PC Units. Always heed these precautions.

- A CJ-series CPU Unit is shipped with the battery installed and the time already set on the internal clock. It is not necessary to clear memory or set the clock before application, as it is for the CS-series CPU Units.
- The user program and parameter area data in CJ1-H CPU Units is backed up in the built-in flash memory. The BKUP indicator will light on the front of the CPU Unit when the backup operation is in progress. Do not turn OFF the power supply to the CPU Unit when the BKUP indicator is lit. The data will not be backed up if power is turned OFF.
- If, when using a CJ1-H CPU Unit, the PC Setup is set to specify using the mode set on the Programming Console and a Programming Console is not connected, the CPU Unit will start in RUN mode. This is the default setting in the PC Setup. (A CS1 CPU Unit will start in PROGRAM mode under the same conditions.)
- When creating an AUTOEXEC.IOM file from a Programming Device (a Programming Console or the CX-Programmer) to automatically transfer data at startup, set the first write address to D20000 and be sure that the size of data written does not exceed the size of the DM Area. When the data file is read from the Memory Card at startup, data will be written in the CPU Unit starting at D20000 even if another address was set when the AUTOEXEC.IOM file was created. Also, if the DM Area is exceeded (which is possible when the CX-Programmer is used), the remaining data will be written to the EM Area.
- Always turn ON power to the PC before turning ON power to the control system. If the PC power supply is turned ON after the control power supply, temporary errors may result in control system signals because the output terminals on DC Output Units and other Units will momentarily turn ON when power is turned ON to the PC.
- Fail-safe measures must be taken by the customer to ensure safety in the event that outputs from Output Units remain ON as a result of internal circuit failures, which can occur in relays, transistors, and other elements.
- Fail-safe measures must be taken by the customer to ensure safety in the event of incorrect, missing, or abnormal signals caused by broken signal lines, momentary power interruptions, or other causes.
- Interlock circuits, limit circuits, and similar safety measures in external circuits (i.e., not in the Programmable Controller) must be provided by the customer.
- Do not turn OFF the power supply to the PC when data is being transferred. In particular, do not turn OFF the power supply when reading or writing a Memory Card. Also, do not remove the Memory Card when the BUSY indicator is lit. To remove a Memory Card, first press the memory card power supply switch and then wait for the BUSY indicator to go out before removing the Memory Card.

- If the I/O Hold Bit is turned ON, the outputs from the PC will not be turned OFF and will maintain their previous status when the PC is switched from RUN or MONITOR mode to PROGRAM mode. Make sure that the external loads will not produce dangerous conditions when this occurs. (When operation stops for a fatal error, including those produced with the FALS(007) instruction, all outputs from Output Unit will be turned OFF and only the internal output status will be maintained.)
- The contents of the DM, EM, and HR Areas in the CPU Unit are backed up by a Battery. If the Battery voltage drops, this data may be lost. Provide countermeasures in the program using the Battery Error Flag (A40204) to re-initialize data or take other actions if the Battery voltage drops.
- Always use the power supply voltages specified in the operation manuals. An incorrect voltage may result in malfunction or burning.
- Take appropriate measures to ensure that the specified power with the rated voltage and frequency is supplied. Be particularly careful in places where the power supply is unstable. An incorrect power supply may result in malfunction.
- Install external breakers and take other safety measures against short-circuiting in external wiring. Insufficient safety measures against short-circuiting may result in burning.
- Do not apply voltages to the Input Units in excess of the rated input voltage. Excess voltages may result in burning.
- Do not apply voltages or connect loads to the Output Units in excess of the maximum switching capacity. Excess voltage or loads may result in burning.
- Disconnect the functional ground terminal when performing withstand voltage tests. Not disconnecting the functional ground terminal may result in burning.
- Install the Units properly as specified in the operation manuals. Improper installation of the Units may result in malfunction.
- Be sure that all the terminal screws, and cable connector screws are tightened to the torque specified in the relevant manuals. Incorrect tightening torque may result in malfunction.
- Leave the label attached to the Unit when wiring. Removing the label may result in malfunction if foreign matter enters the Unit.
- Remove the label after the completion of wiring to ensure proper heat dissipation. Leaving the label attached may result in malfunction.
- Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Connection of bare stranded wires may result in burning.
- Wire all connections correctly.
- Double-check all wiring and switch settings before turning ON the power supply. Incorrect wiring may result in burning.
- Mount Units only after checking terminal blocks and connectors completely.
- Be sure that the terminal blocks, Memory Units, expansion cables, and other items with locking devices are properly locked into place. Improper locking may result in malfunction.

- Check switch settings, the contents of the DM Area, and other preparations before starting operation. Starting operation without the proper settings or data may result in an unexpected operation.
- Check the user program for proper execution before actually running it on the Unit. Not checking the program may result in an unexpected operation.
- Confirm that no adverse effect will occur in the system before attempting any of the following. Not doing so may result in an unexpected operation.
  - Changing the operating mode of the PC.
  - Force-setting/force-resetting any bit in memory.
  - Changing the present value of any word or any set value in memory.
- Resume operation only after transferring to the new CPU Unit the contents of the DM Area, HR Area, and other data required for resuming operation. Not doing so may result in an unexpected operation.
- Do not pull on the cables or bend the cables beyond their natural limit. Doing either of these may break the cables.
- Do not place objects on top of the cables or other wiring lines. Doing so may break the cables.
- Do not use commercially available RS-232C personal computer cables. Always use the special cables listed in this manual or make cables according to manual specifications. Using commercially available cables may damage the external devices or CPU Unit.
- When replacing parts, be sure to confirm that the rating of a new part is correct. Not doing so may result in malfunction or burning.
- Before touching a Unit, be sure to first touch a grounded metallic object in order to discharge any static build-up. Not doing so may result in malfunction or damage.
- When transporting or storing circuit boards, cover them in antistatic material to protect them from static electricity and maintain the proper storage temperature.
- Do not touch circuit boards or the components mounted to them with your bare hands. There are sharp leads and other parts on the boards that may cause injury if handled improperly.
- Do not short the battery terminals or charge, disassemble, heat, or incinerate the battery. Do not subject the battery to strong shocks. Doing any of these may result in leakage, rupture, heat generation, or ignition of the battery. Dispose of any battery that has been dropped on the floor or otherwise subjected to excessive shock. Batteries that have been subjected to shock may leak if they are used.
- UL standards required that batteries be replaced only by experienced technicians. Do not allow unqualified persons to replace batteries.
- After connecting Power Supply Units, CPU Units, I/O Units, Special I/O Units, or CPU Bus Units together, secure the Units by sliding the sliders at the top and bottom of the Units until they click into place. Correct operation may not be possible if the Units are not securely properly. Be sure to attach the end cover provided with the CPU Unit to the rightmost Unit. CJ-series PCs will not operate properly if the end cover is not attached.

6 Conformance to EC Directives

6-1 Applicable Directives

- EMC Directives
- Low Voltage Directive

6-2 Concepts

EMC Directives

OMRON devices that comply with EC Directives also conform to the related EMC standards so that they can be more easily built into other devices or the overall machine. The actual products have been checked for conformity to EMC standards (see the following note). Whether the products conform to the standards in the system used by the customer, however, must be checked by the customer.

EMC-related performance of the OMRON devices that comply with EC Directives will vary depending on the configuration, wiring, and other conditions of the equipment or control panel on which the OMRON devices are installed. The customer must, therefore, perform the final check to confirm that devices and the overall machine conform to EMC standards.

Note Applicable EMC (Electromagnetic Compatibility) standards are as follows:

EMS (Electromagnetic Susceptibility): EN61000-6-2
EMI (Electromagnetic Interference): EN50081-2
(Radiated emission: 10-m regulations)

Low Voltage Directive

Always ensure that devices operating at voltages of 50 to 1,000 V AC and 75 to 1,500 V DC meet the required safety standards for the PC (EN61131-2).

6-3 Conformance to EC Directives

The CJ-series PCs comply with EC Directives. To ensure that the machine or device in which the CJ-series PC is used complies with EC Directives, the PC must be installed as follows:

1,2,3...

1. The CJ-series PC must be installed within a control panel.
2. You must use reinforced insulation or double insulation for the DC power supplies used for the communications power supply and I/O power supplies.
3. CJ-series PCs complying with EC Directives also conform to the Common Emission Standard (EN50081-2). Radiated emission characteristics (10-m regulations) may vary depending on the configuration of the control panel used, other devices connected to the control panel, wiring, and other conditions. You must therefore confirm that the overall machine or equipment complies with EC Directives.

6-4 Relay Output Noise Reduction Methods

The CJ-series PCs conforms to the Common Emission Standards (EN50081-2) of the EMC Directives. However, noise generated by relay output switching may not satisfy these Standards. In such a case, a noise filter must be connected to the load side or other appropriate countermeasures must be provided external to the PC.

Countermeasures taken to satisfy the standards vary depending on the devices on the load side, wiring, configuration of machines, etc. Following are examples of countermeasures for reducing the generated noise.

Countermeasures

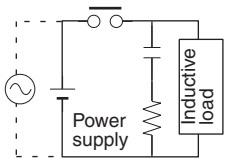
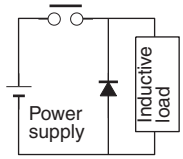
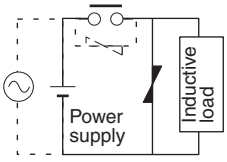
(Refer to EN50081-2 for more details.)

Countermeasures are not required if the frequency of load switching for the whole system with the PC included is less than 5 times per minute.

Countermeasures are required if the frequency of load switching for the whole system with the PC included is more than 5 times per minute.

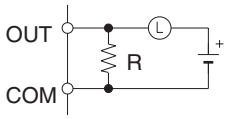
Countermeasure Examples

When switching an inductive load, connect an surge protector, diodes, etc., in parallel with the load or contact as shown below.

Circuit	Current		Characteristic	Required element
	AC	DC		
CR method 	Yes	Yes	If the load is a relay or solenoid, there is a time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the surge protector in parallel with the load. If the supply voltage is 100 to 200 V, insert the surge protector between the contacts.	The capacitance of the capacitor must be 1 to 0.5 μF per contact current of 1 A and resistance of the resistor must be 0.5 to 1 Ω per contact voltage of 1 V. These values, however, vary with the load and the characteristics of the relay. Decide these values from experiments, and take into consideration that the capacitance suppresses spark discharge when the contacts are separated and the resistance limits the current that flows into the load when the circuit is closed again. The dielectric strength of the capacitor must be 200 to 300 V. If the circuit is an AC circuit, use a capacitor with no polarity.
Diode method 	No	Yes	The diode connected in parallel with the load changes energy accumulated by the coil into a current, which then flows into the coil so that the current will be converted into Joule heat by the resistance of the inductive load. This time lag, between the moment the circuit is opened and the moment the load is reset, caused by this method is longer than that caused by the CR method.	The reversed dielectric strength value of the diode must be at least 10 times as large as the circuit voltage value. The forward current of the diode must be the same as or larger than the load current. The reversed dielectric strength value of the diode may be two to three times larger than the supply voltage if the surge protector is applied to electronic circuits with low circuit voltages.
Varistor method 	Yes	Yes	The varistor method prevents the imposition of high voltage between the contacts by using the constant voltage characteristic of the varistor. There is time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the varistor in parallel with the load. If the supply voltage is 100 to 200 V, insert the varistor between the contacts.	---

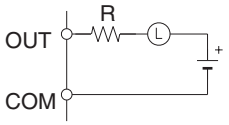
When switching a load with a high inrush current such as an incandescent lamp, suppress the inrush current as shown below.

Countermeasure 1



Providing a dark current of approx. one-third of the rated value through an incandescent lamp

Countermeasure 2



Providing a limiting resistor

SECTION 1
Introduction

This section introduces the special features and functions of the CJ-series PCs and describes the differences between these PCs and the earlier C200HX/HG/HE PCs.

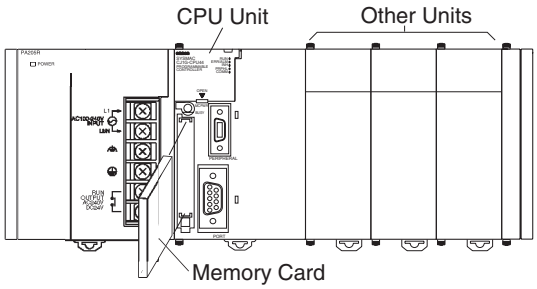
1-1 Overview

The CJ-series PCs are very small-sized Programmable Controllers that feature high speed and advanced functions with the same architecture as the CS-series PCs.

- Only 90 x 65 mm (H x D) for mounting in small spaces in machines and on the same DIN Track as components, contributing to machine downsizing, increased functionality, and modularization.
- Basic instructions executed at 0.02 μs min. and special instructions at 0.06 μs min (for the CJ1-H CPU Units).
- Support the DeviceNet open network and protocol macros (for serial communications) to enable information sharing in machines. Machine-to-machine connections with Controller Link and host connections with Ethernet are also supported for even more advanced information sharing, including seamless message communications across Ethernet, Controller Link, and DeviceNet networks.

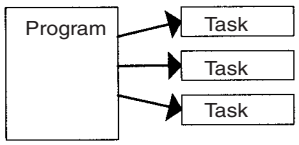
Same Advanced Performance as CS-series PCs

Basic instructions: 0.02 μs
Special instructions: 0.06 μs
Same high-speed CPU bus as CS Series.
Large data memory: 256 Kwords
Program compatibility with CS-series PCs



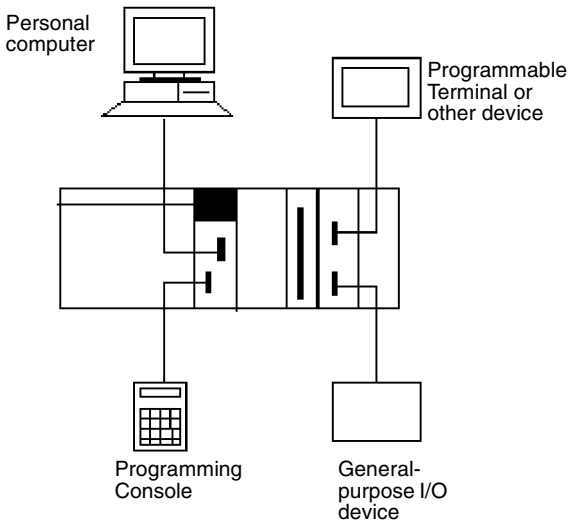
Structured Programming

The program is divided into tasks.
Symbols can be used in programming.
The overall performance of the system is improved by executing only the required tasks.
Modification and debugging are simplified.
The program arrangement can be changed.
Step control and block programming instructions can be used.
Comments can be added to make the program easier to understand.



Protocol Macro Function Serves Multiple Ports

Up to 32 ports can be connected (Serial Communications Units).
Different Protocol Macros can be allocated to each port.



Remote Programming, Monitoring and Seamless Links between Networks

FINS commands allow communications between nodes in different networks: Ethernet, Controller Link, and DeviceNet
Remote programming and monitoring can be performed.

Minimum (fixed) cycle time function
I/O refreshing method selection
PC Setup functions
Use Windows tools to create multiple environments in a single personal computer.

Full Complement of Versatile Functions

Memory Card and file processing functions
Simplify programs with specialized instructions such as the table data and text string processing instructions
Troubleshooting functions
Data tracing function

The CJ-series PCs support the same task-based programming structure, instructions, high-speed instruction execution, I/O memory, functionality, and message communications as the CS-series PCs. The main differences of the CJ-series in comparison to the CS-series PCs are as follows (refer to page 31 for details):

- No Backplanes are required.
- Screw mounting is not supported (only DIN Track mounting).
- Smaller size (30% to 35% in terms of volume).
- Inner Boards are not supported.
- I/O interrupt tasks and external interrupt tasks are not supported by CJ1 CPU Units. (They are supported by CJ1-H CPU Units.)
- C200H Special I/O Units are not supported (e.g., SYSMAC BUS Remote I/O Units).
- It is not necessary to create I/O tables unless desired, i.e., I/O tables can be created automatically when power is turned ON.
- The startup mode when a Programming Console is not connected is RUN mode (rather than PROGRAM mode, as it is for CS1 CPU Units).
- Only version 2.04 or later versions of CX-Programmer can be connected (version 2.1 or later for the CJ1-H CPU Units).

1-2 CJ-series Features

1-2-1 Special Features

Improvements in Basic Performance

The CJ Series provides high speed, high capacity, and more functions in micro-size PCs.

Only 30% to 35% of the Volume of CS-series PCs

At 90 x 65 mm (height x depth), the CJ-series Units have on 70% the height and half the depth of CS-series Units, contributing to machine downsizing.

Mount to DIN Track

The CJ-series PCs can be mounted to DIN Track along with power supplies and other components when there is limited installation space in a machine (e.g., limited space between top and bottom ducts).

Faster Instruction Execution and Peripheral Servicing

The cycle time has been greatly reduced as a result of faster instruction execution (basic instructions: 0.02 or 0.08 μs min., special instructions: 0.06 or 0.12 μs, and floating-point instructions: 8.0 or 10.2 μs min. for CJ1 or CJ1-H CPU Units) and faster processing for overhead, I/O refreshes, and peripheral servicing.

Ample Programming Capacity

With up to 120 Ksteps of program capacity, 256 Kwords of DM Memory, and 2,560 I/O points, there is sufficient capacity for added-value programs including machine interfaces, communications, data processing, etc.

Program and PC Setup Compatibility with CS-series CPU Units

There is almost 100% compatibility with CS-series CPU Units for programming and internal settings (PC Setup).

Note Because of physical differences in the CJ-series PCs, they do not support all of the features of the CS-series PC.

No Backplanes for Greater Space Efficiency

A flexible system configuration that requires less space is made possible because Backplanes are not required for CJ-series PCs.

Up to 3 Expansion Racks and 40 Units

By connecting an I/O Control Unit to the CPU Rack and I/O Interface Units to Expansion Racks, up to 3 Expansion Racks can be connected. The CPU

Rack can contain up to 10 Units, as can each of the 3 Expansion Racks, enabling a total of up to 40 Units.

Two I/O Allocation Methods

The need for Backplanes was eliminated, enabling the following two methods for allocating I/O.

1. Automatic I/O Allocation at Startup
   I/O is allocated to the connected Units each time the power is turned ON (same as CQM1H PCs).
2. User-set I/O Allocation
   If desired, the user can set I/O tables in the same way as for the CS-series PCs.

The default setting is for automatic I/O allocation at startup, but the user can set the PC to automatically use I/O tables to enable checking for Unit connection errors or to allocate unused words.

Allocate Unused Words

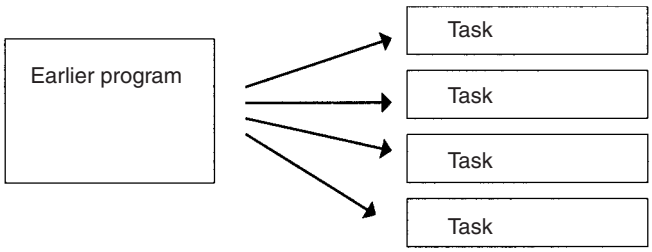
The CX-Programmer can be used to allocate unused words in I/O tables for transfer to the CPU Unit. This enables keeping words unallocated for future use or to enable system standardization/modularization.

Structured Programming

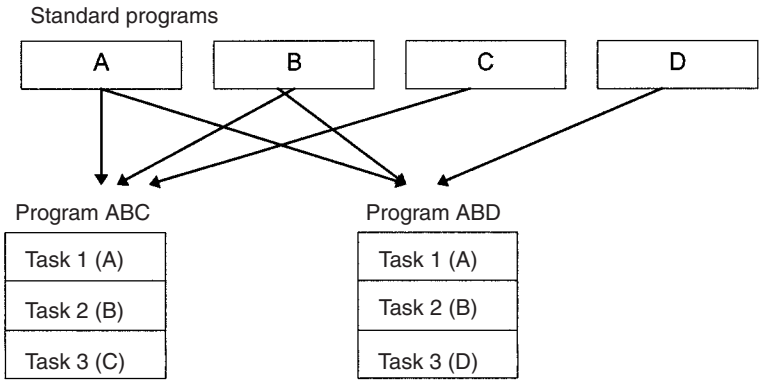
Division of the Program into Tasks

When the program is divided into tasks that handle separate functions, control systems, or processes, several programmers can develop these separate tasks simultaneously.

There can be up to 32 regular (cyclically executed) tasks and 256 interrupt tasks. There are two types of interrupts: Power OFF Interrupts and Scheduled Interrupts.



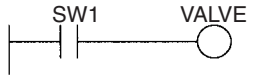
When a new program is being created, standard programs can be combined as tasks to create an entire program.



Using Symbols

Arbitrary symbols (names up to 32 characters) that are independent of I/O terminal allocations can be used in programming. Standard programs created with symbols are more general and easier to reuse as tasks in different programs.

Symbols specified for bit address:



Global and Local Symbols Supported

I/O names are handled as symbols which can be defined as global symbols, which apply to all of the programs in all tasks, or as local symbols, which apply to just the local task.

When the symbols are defined, you can choose to have the local symbols allocated to addresses automatically.

Improve Overall System Response Performance

The response performance of the system can be improved by dividing the program into a system-management task and tasks used for control and executing only those control tasks that need to be executed.

Simplify Program Modification

- Debugging is more efficient when the job of modifying and debugging the tasks can be divided among several individuals.
- Program maintenance is easier because only the tasks affected by changes have to be modified when there are changes (such as changes in specifications).
- Several consecutive program lines can be modified with online editing.
- The amount the cycle time is extended during online editing has been reduced.

Change Program Arrangement Easily

When separate tasks have been programmed for different production models, the task control instructions can be used to switch the program quickly from production of one model to another.

Step Control and Block Programming

The step control and block programming instructions can be used to control repetitive processes that are difficult to program with ladder programming alone.

Comments

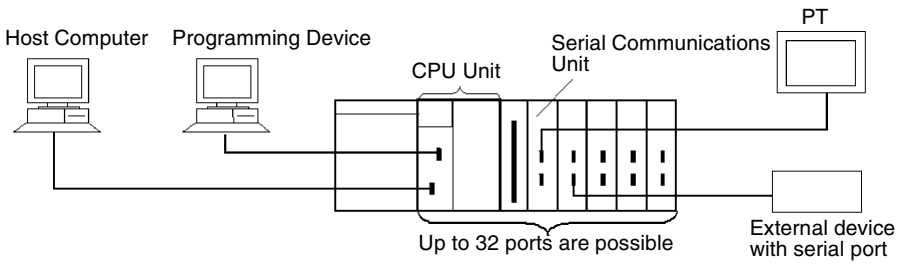
Several types of comments can be added to the program to make it easier to understand, including Rung comments, and I/O comments.

Port-specific Protocol Macros

Create Protocol Macros for All Ports

Protocol macros can be used to create versatile communications functions for any of the PC's communications ports. The communications functions can have host link, NT Link, or protocol macro configurations and can be directed to RS-232C and RS-422/485 ports on any of the Units.

All together, a CPU Unit can support a maximum of 32 ports. In addition, up to 16 ASCII Units can be connected. The ASCII Units can be used to create protocol functions with BASIC programs.



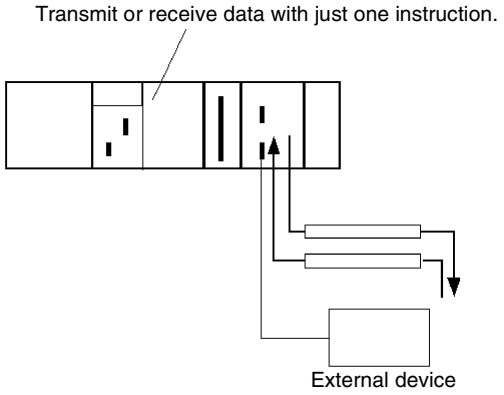
Standard Serial Communications with External Devices

Messages can be transferred to and from standard serial devices with the protocol macro function (according to preset parameter settings). The protocol macro function supports processing options such as retries, timeout monitoring, and error checks.

Symbols that read and write data to the CPU Unit can be included in the communications frames, so data can be exchanged with the CPU Unit very easily.

OMRON components (such as Temperature Controllers, ID System Devices, Bar Code Readers, and Modems) can be connected to a Serial Communications Unit with the standard system protocol. It is also possible to change the settings if necessary.

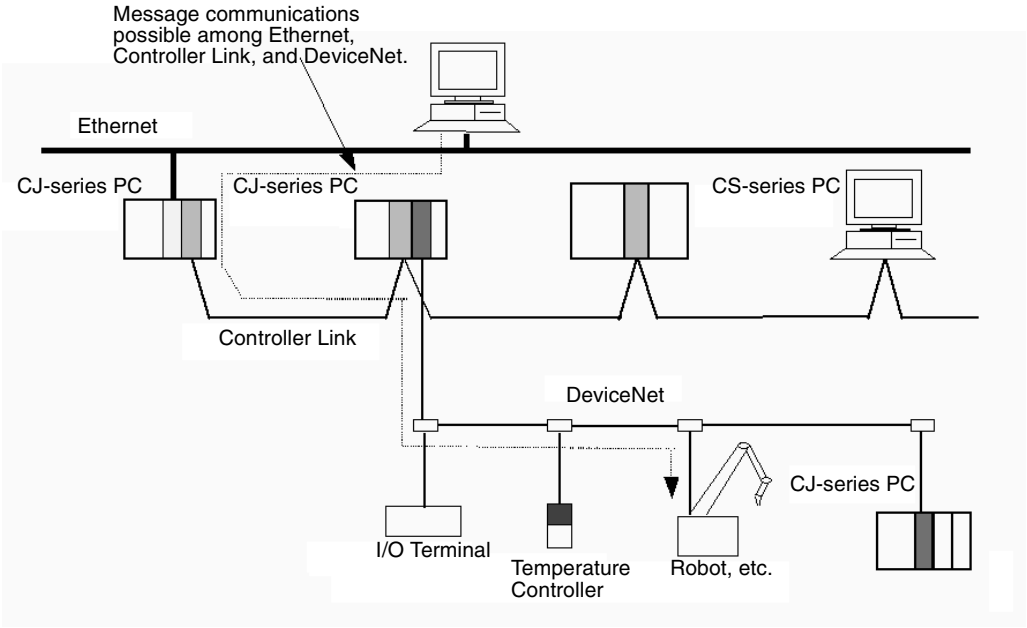
Note The Serial Communications Unit must be purchased separately to take advantage of this function.



Multilevel Network Configurations

Different network levels can be connected as shown in the following diagram. The multilevel configuration provides more flexibility in networking from the manufacturing site to production management.

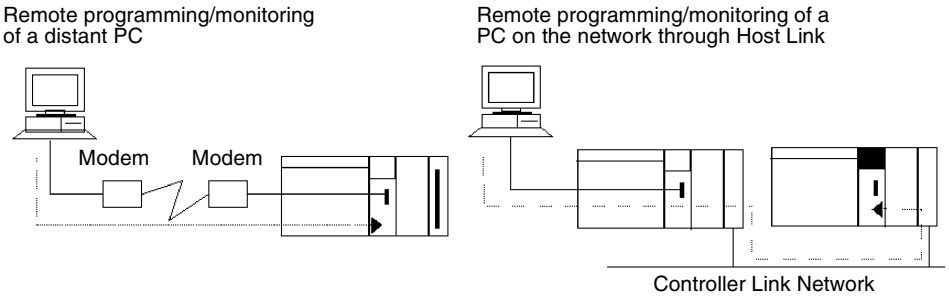
OA network:	Ethernet
FA network:	Controller Link
Open network:	DeviceNet (CompoBus/D)



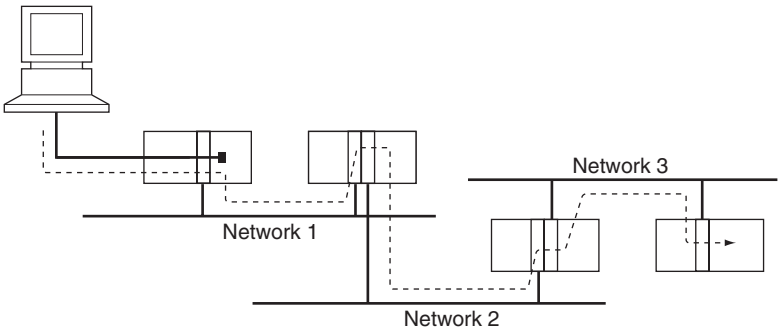
Remote Monitoring and Programming

1,2,3...

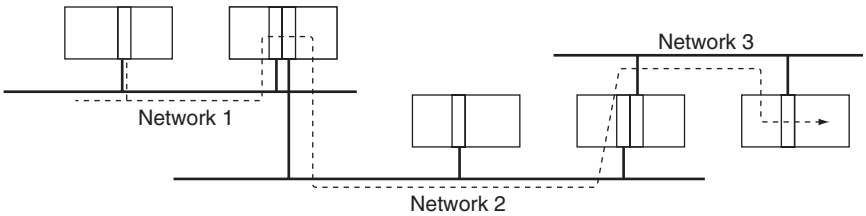
1. The host link function can operate through a modem, which allows monitoring of a distant PC's operation, data transfers, or even online editing of a distant PC's program by phone.
2. PCs in a network can be programmed and monitored through the Host Link.
3. It is possible to communicate through 3 network levels even with different types of networks.



Remote programming/monitoring of a PC on a network up to 3 levels away (including the local network) for the same or different types of networks is possible through Host Link.



Message transfer between PCs on a network 3 levels away (including the local network) for the same or different types of networks.



Seamless message communications are possible across Ethernet, Controller Link, and DeviceNet networks, enabling easy information integration on machine, machine-to-machine, and machine-to-host levels.

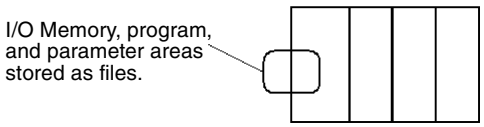
Note NT Link communications between an NT31/NT631-V2 PT and a CJ-series PC are now possible at high speed.

1-2-2 Versatile Functions

Memory Card and File Management Functions

Transfer Data to and from Memory Cards

Data area data, program data, and PC Setup data can be transferred as files between the Memory Card (compact flash memory) and a Programming Device, program instructions, a host computer, or via FINS commands. Memory Cards are available with capacities 8, 15, 30, and 48 Mbytes.



Convert EM Area Banks to File Memory

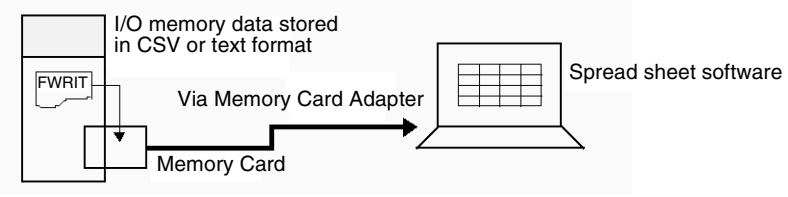
Part of the EM Area can be converted to file memory to provide file management capabilities without a Memory Card and with much faster access time than a Memory Card. (The EM Area can be very useful for storing data such as trend data as files.)

Automatic File Transfer at Start-up

The PC can be set up to transfer the program and/or PC Setup files from the Memory Card when the PC is turned ON. With this function, the Memory Card provides a flash-ROM transfer. This function can also be used to store and change PC configurations quickly and easily.

I/O Memory Files in CSV and Text Format

It is now possible to save production results and other data (hexadecimal) from the CPU Unit I/O memory in a Memory Card in CSV or text format. The data can then be read and edited using personal computer spreadsheet software by means of a Memory Card Adapter.

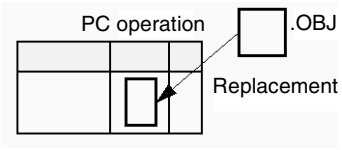


File Operations (Format, Delete, etc.) from Ladder Programs

It is possible to format files, delete, copy, change file names, create new directories, and perform similar operations on a Memory Card from the ladder program during PC operation.

Program Replacement During Operation

It is now possible to replace the entire user program in the CPU Unit from the Memory Card during operation. In this way, it is possible to switch PC operation without stopping the PC.



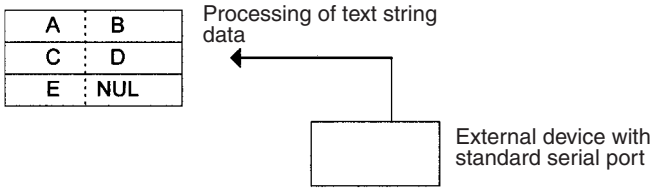
Easy Backups

It is now possible to back up all data (user programs, parameters, and I/O memory) to the Memory Card by pressing the Memory Card power supply switch. In this way, if a malfunction arises, it is possible to back up all data in the CPU Unit at the time without using a Programming Device.

Specialized Instructions Simplify Programming

Text String Instructions

The text string instructions allow text processing to be performed easily from the ladder program. These instructions simplify the processing required when creating messages for transmission or processing messages received from external devices with the protocol macro function.



Loop Instructions

The FOR(512), NEXT(513), and BREAK(514) instructions provide a very powerful programming tool that takes up little program capacity.

Index Registers

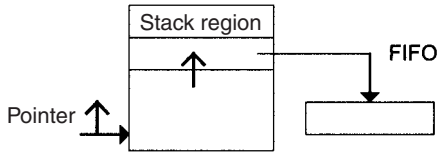
Sixteen Index Registers are provided for use as pointers in instructions. An Index Register can be used to indirectly address any word in I/O memory. The CJ-series PCs also support the auto-increment, auto-decrement, and offset functions.

The Index Registers can be a powerful tool for repetitive processing (loops) when combined with the auto-increment, auto-decrement, and offset functions. Index Registers can also be useful for table processing operations such as changing the order of characters in text strings.

Table Data Processing Instructions

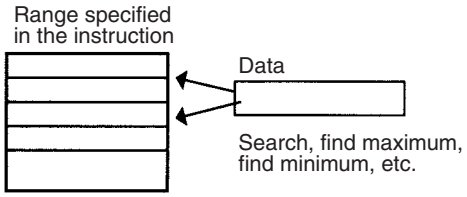
Stack Instructions

A region of I/O memory can be defined as a stack region. Words in the stack are specified by a stack pointer for easy FIFO (first-in first-out) or LIFO (last-in first-out) data processing.



Range Instructions

These instructions operate on a specified range of words to find the maximum value or minimum value, search for a particular value, calculate the sum or FCS, or swap the contents of the leftmost and rightmost bytes in the words.

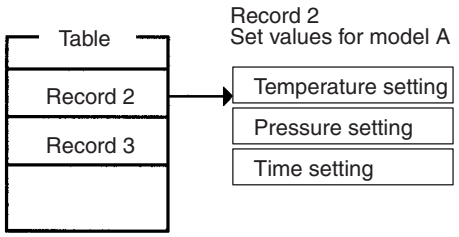


Record-table Instructions

Record-table instructions operate on specially defined data tables. The record table must be defined in advance with DIM(631), which declares the number of words in a record and the number of records in the table. Up to 16 record tables can be defined.

Record tables are useful when data is organized in records. As an example, if temperatures, pressures, or other set values for various models have been combined into a table, the record-table format makes it easy to store and read the set values for each model.

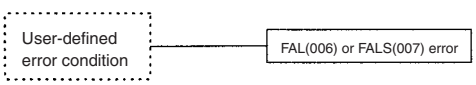
The SETR(635) can be used to store the first address of the desired record in an Index Register. Index Registers can then be used to simplify complicated processes such as changing the order of records in the record table, searching for data, or comparing data.



Troubleshooting Functions

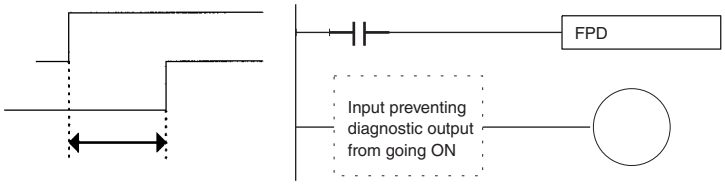
Failure Diagnosis: FAL(006) and FALS(007)

The FAL(006) and FALS(007) can be used to generate a non-fatal or fatal error when the user-defined conditions are met. Records of these errors are stored in the error log just like system-generated errors.



Failure Point Detection: FPD(269)

Diagnoses a failure in an instruction block by monitoring the time between execution of FPD(269) and execution of a diagnostic output and finding which input is preventing an output from being turned ON.



Error Log Functions

The error log contains the error code and time of occurrence for the most recent 20 errors (user-defined or system-generated errors).

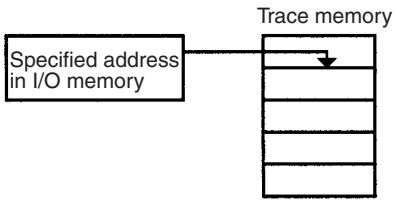
Maintenance Functions

The CJ-series PCs record information useful for maintenance, such as the number of power interruptions and the total PC ON time.

Other Functions

Data Trace Function

The content of the specified word or bit in I/O memory can be stored in trace memory by one of the following methods: scheduled sampling, cyclic sampling, or sampling at execution of TRSM(045).



Fixed Cycle Time Function

A fixed (minimum) cycle time can be set to minimize variations in I/O response times.

I/O Refreshing Methods

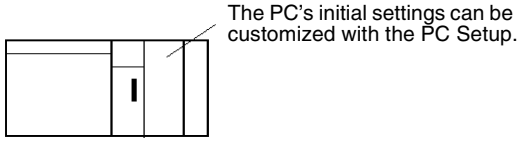
I/O refreshing can be performed cyclically and immediately by programming the immediate-refreshing variation of the instruction.

Peripheral Servicing Priority Mode

The CPU Unit can be set to execute peripheral servicing periodically and more than once in each cycle. Up to five items can be set for priority servicing, including the RS-232C port, peripheral port, CPU Bus Units, and Special I/O Units. This feature supports applications that require giving priority to servicing peripheral devices over program execution, such as for host monitoring systems for process control where response speed is important.

PC Setup Functions

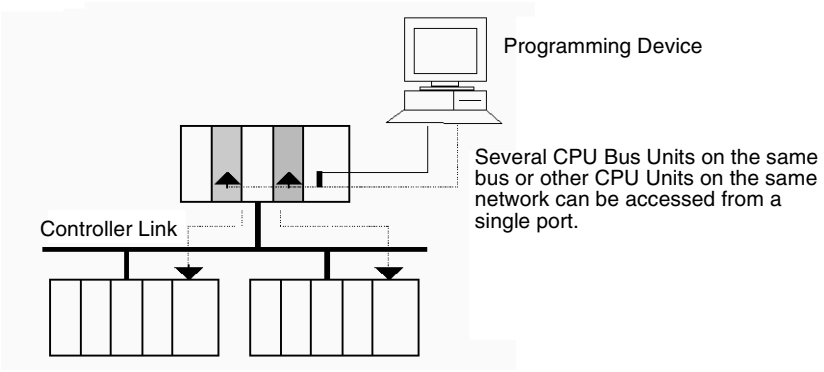
PC operation can be customized with PC Setup settings, such as the maximum cycle time setting (watch cycle time) and the instruction error operation setting, which determines whether instruction processing errors and access errors are treated as non-fatal or fatal errors.



Windows-based Support Software

The single-port multiple-access (SPMA) function can be used to program and monitor other CPU Bus Units on the same bus (CPU Rack or Expansion

Racks) or other CPU Units on the same network from a serial port on the CPU Unit.



1-3 CJ1-H CPU Unit Features

1-3-1 High-speed Performance

Ultra High-speed Cycle Time

The CJ1-H CPU Units provide a cycle time that is three to four times faster than that of the CJ1 CPU Units.

For example, a program consisting of 38 Ksteps of only basic instructions with 128 inputs and 128 outputs executes in 1 ms (4.9 ms for the CJ1 CPU Units); a program consisting of 20 Ksteps of basic and special instructions in a 1:1 ratio with 128 inputs and 128 outputs executes in 1 ms (2.7 ms for the CJ1 CPU Units); and a program consisting of 8 Ksteps of basic and special instructions in a 1:2 ratio with 64 inputs and 64 outputs executes in 0.5 ms (1.4 ms for the CJ1 CPU Units).

The following factors give the CJ1-H CPU Units their high speed.

1,2,3...

1. Instruction execution times: Only about 1/2 the time required for basic instructions, and only about 1/3 the time required for special instructions.
2. Better bus performance: Data transfers between the CPU Unit and Special I/O or Communications Units is about twice as fast, providing greater overall system performance.
3. Instruction execution is performed in parallel with peripheral servicing.
4. Other factors, including background execution of text string processing and table data processing instructions.

Faster Execution of Common Instructions

Extensive research on applications of CJ1 CPU Units was used to identify the 20 most commonly used instructions of the more than 400 supported instructions (see below), and execution speed for these instructions was increased by 10 to 20 times previous performance.

CPS (SIGNED BINARY COMPARE)
JMP (JUMP)
CPSL (DOUBLE SIGNED BINARY COMPARE)
CJP (CONDITIONAL JUMP)
XFER (BLOCK TRANSFER)
BCNT (BIT COUNTER)
MOVB (MOVE BIT)
MLPX (DATA DECODER)
MOVD (MOVE DIGITS)
BCD (BINARY-TO-BCD)
BSET (BLOCK SET)
SBS/RET (SUBROUTINE CALL/RETURN)

System Bus Speed Doubled

The speed of transferring data between the CPU Unit and CPU Bus Units has been doubled to increase overall system performance.

Parallel Processing of Instructions and Peripheral Servicing

A special mode is supported that enables parallel processing of instruction execution and peripheral device servicing to support the following types of application.

- Extensive data exchange with a host not restricted by the program capacity in the CJ1-H CPU Unit
- Consistently timed data exchange with SCADA software
- Eliminating the effects on cycle time of future system expansion or increases in communications

Less Cycle Time Fluctuation for Data Processing

Table data processing and text string processing, which often require time, can be separated over several cycles to minimize fluctuations in the cycle time and achieve stable I/O response.

Better Data Link and Remote I/O Refreshing

CPU Bus Unit refresh response has been increased both by reductions in the cycle time itself and by the addition of an immediate I/O refresh instruction for CPU Bus Units (DLNK(226)). This instruction will refresh data links, DeviceNet remote I/O, protocol macros, and other special data for CPU Bus Units.

The response of a CJ1-H CPU Unit is approximately 2.4 times that of a CJ1 CPU Unit. And, for a cycle time of approximately 100 ms or higher, the increase in the data link response is comparable to that for the cycle time.

Immediate Refreshing for CPU Bus Units

Although previously, I/O refreshing for CPU Bus Units was possible only after program executions, a CPU BUS I/O REFRESH instruction (DLNK(226)) has been added to enable immediate I/O refreshing for CPU Bus Units. Data links, DeviceNet remote I/O, an other unique CPU Bus Unit refreshing can be refreshed along with words allocated to the CPU Bus Unit in the CIO and DM Areas whenever DLNK(226) is executed. This is particularly effective for longer cycle times (e.g., 100 ms or longer). (Data exchange for data links, DeviceNet remote I/O, and other network communications are also affected by the communications cycle time, i.e., DLNK(226) refreshes data only between the CPU Bus Units and the CPU Unit, not the data on the individual networks.)

1-3-2 High-speed Structured Programming

To further aid standardized programming, program structuring functions have been improved, as has program execution speed.

More Cyclic Tasks

Tasks provide better efficiency by enabling programs to be separated by function or for development by different engineers. The CJ1-H CPU Units support up to 288 cyclic tasks, an incredible increase over the previous maximum of 32 tasks.

Common Processing from Multiple Tasks

Global subroutines that can be called by any task are now supported. These can be used for common processing from more than one task, for greater standardization.

Faster Subroutine Instructions

Subroutine instruction are executed approximately 9 or 17 times faster to enable greater program modularization without having to be concerned about increasing the cycle time.

Shared Index and Data Registers between Tasks

Although separate index and data registers can still be used in each task, they have been joined by shared index and data registers that can be used between tasks to reduce the time required to switch between tasks.

1-3-3 More Instructions for Specific Applications

Very specific control can be easily programmed for a much wider range of applications with the many new special instructions added to the CJ1-H CPU Units.

High-speed Positioning for XY Tables

Double-precision floating-point calculations are supported for the CJ1-H CPU Units to provide even better precision for position control operations.

Convert between Floating Point and Text String Data

To display floating-point data on PTs, the CJ1-H CPU Units provide conversion instructions from floating-point data to text strings (ASCII). Conversion between ASCII and floating-point data is also possible so that ASCII data from serial communications with measurement devices can be used in calculations.

Accurate Line Approximations

Unsigned 16-bit binary/BCD data, signed 16/32-bit binary data, or floating-point data can be used for line data, enabling precise (high data resolution) conversions, such as from a level meter (mm) to tank capacity (l) based on the shape of the tank.

Realtime Workpiece Data Management

When loading and unloading workpieces from conveyor lines, workpiece information can be managed in realtime in table format.

PID Autotuning

Autotuning is now supported for PID constants with the PID CONTROL instruction. The limit cycle method is used to ensure rapid autotuning. Very effective for multiloop PID control.

System Debugging through Error Simulation

A specified error status can be created with the FAL/FALS instructions. This can be used effectively when depending systems. For example, errors can be simulated to produce corresponding displays on a PT to confirm that the correct messages are being displayed.

Program Simplification with More Specific Basic Instructions

Programs that use a high quantity of basic instructions can be simplified though the use of differentiated forms of the LD NOT, AND NOT and OR NOT instructions, and through the use of OUT, SET, and RSET instructions that can manipulate individual bits in the DM or EM Area.

Delayed Power OFF Processing for Specified Program Areas

The DI and EI instructions can be used to disable interrupts during specific portions of the program, for example, to prevent the power OFF interrupt from being executed until a specific instruction has been executed.

1-3-4 Battery-free Operation with Flash Memory

Any user program or parameter area data transferred to the CPU Unit is automatically backed up in flash memory in the CPU Unit to enable battery-free operation without using a Memory Card.

Note Refer to information on flash memory in the *CS/CJ Series Programming Manual* (W394) for precautions on this function.

1-3-5 Better Compatibility with Other SYSMAC PCs

C200HE/HG/HX PCs

The AREA RANGE COMPARE (ZCP) and DOUBLE AREA RANGE COMPARE (ZCPl) instructions are supported in the CJ1-H CPU Units to provide better compatibility with the C200HE/HG/HX PCs.

CVM1/CV-series PCs

The CONVERT ADDRESS FROM CV instruction allows real I/O memory addresses for the CVM1/CV-series PCs to be converted to addresses for the CJ-series PCs, enabling programs with CVM1/CV-series addresses to be quickly converted for use with a CJ-series CPU Unit.

1-4 CJ1 and CJ1-H CPU Unit Comparison

Item			CJ1-H CPU Unit (CJ1H-CPU6□H)	CJ1 CPU Unit (CJ1G-CPU4□)
Instruction executions times	Basic instructions		LD: 0.02 μs	0.08 μs
			OUT: 0.02 μs	0.21 μs
	Special instructions		Examples	
			XFER: 300 μs (for 1,000 words)	633 μs (for 1,000 words)
			BSET: 200 μs (for 1,000 words)	278 μs (for 1,000 words)
			BCD arithmetic: 8.2 μs min.	14 μs min.
			Binary arithmetic: 0.18 μs min.	0.25 μs min.
			Floating-point math: 8 μs min.	10 μs min.
			SBS/RET: 2.1 μs	37 μs
Overseeing processing time			Normal mode: 0.3 ms Parallel mode: 0.2 ms	0.5 ms
Execution timing	CPU execution processing modes		Any of the following 4 modes: Normal (instructions and peripheral servicing perform consecutively) Peripheral Servicing Priority Mode (instruction execution interrupted to service peripherals at a specific cycle and time; consecutive refreshing also performed) Parallel Processing Mode with Synchronous Memory Access (instruction executed and peripheral services in parallel while synchronizing access to I/O memory) Parallel Processing Mode with Asynchronous Memory Access (instruction executed and peripheral services in parallel without synchronizing access to I/O memory)	Either of following 2 modes: Normal (instructions and peripheral servicing perform consecutively) Peripheral Servicing Priority Mode (instruction execution interrupted to service peripherals at a specific cycle and time; consecutive refreshing also performed) (Add for CPU Units with lot number No. 001201□□□□ or later.)
	CPU Bus Unit special refreshing	Data links	During I/O refresh period or via special CPU BUS UNIT I/O REFRESH instruction (DLNK(226))	During I/O refresh period
		DeviceNet remote I/O		
		Protocol macro send/receive data		
	Refreshing of CIO and DM Areas words allocated to CPU Bus Unit			

Item			CJ1-H CPU Unit (CJ1H-CPU6□H)	CJ1 CPU Unit (CJ1G-CPU4□)
Tasks	Cyclic execution of interrupt tasks via TKON instruction (called “extra cyclic tasks”)		Supported (Up to 255 extra cyclic tasks, increasing the total number of cyclic tasks to 288 max.)	Not supported (No extra cyclic tasks; 32 cyclic tasks max.)
	Independent/shared specifications for index and data registers		Supported The time to switch between tasks can be reduces if shared registers are used.	Not supported (only independent registers for each task)
	Initialization when tasks are started		Supported Task Startup Flags supported.	Only Task Flag for first execution
	Starting subroutines from multiple tasks		Global subroutines can be defined that can be called from more than one task.	Not supported
	Interrupt task execution timing during instruction execution	For instructions other than the following ones	Any instruction that is being executed is interrupted when interrupt task conditions are met to start the interrupt task. If the cyclic task (including extra cyclic tasks) access the same data area words as the instruction that was interrupted, data may not be concurrent. To ensure data concurrency, the DI and EI instructions must be used to disable and enable interrupts during a specific part of the program.	
		For BIT COUNTER (BCNT) or BLOCK TRANSFER (XFER) instructions	Interrupt tasks are started only after execution of the instruction has been completed, ensuring data concurrency even when the same data area words are accessed from the instruction and the interrupt task.	
Debugging	Backup to Memory Cards (simple backup function)		In addition to the data listed at the right, data from Units mounted to the CPU Rack or Expansion Racks can also be backed up to the Memory Card (via pushbutton on front panel). This is very effective when replacing Units. Backup data includes scan lists for DeviceNet Units, protocol macros for Serial Communications Units, etc.	Only the user program parameters, and I/O memory in the CPU Unit
	Automatic user program and parameter area backup to flash memory		Supported (enabling battery-free operation without a Memory Card) The user program and parameter area data are automatically backed up the flash memory whenever they are transferred to the CPU Unit from the CX-Programmer, file memory, etc.	Not supported
I/O tables	Detailed information on I/O table creation errors		Detailed I/O table error information is stored in A261 whenever the I/O tables cannot be created for any reason.	Not supported
	Displaying presence of first rack word setting on Programming Console		It’s possible to confirm if the first rack word has been specified for the system on the Programming Console display. The first rack word is specified from the CX-Programmer, making it previously impossible to confirm the setting from the Programming Console.	Not supported

Item		CJ1-H CPU Unit (CJ1H-CPU6□H)	CJ1 CPU Unit (CJ1G-CPU4□)
Sequence instructions	Differentiated LD NOT, AND NOT, and OR NOT instructions	Supported	Not supported (The same results can be achieved by combining differentiated LD, AND, and OR instructions with the NOT instruction.)
	OUTB, SETB, and RSTB instructions to manipulate individual bits in DM and EM Area words	Supported	Not supported
Special math instructions	32-bit signed data line coordinates and X axis starting point specification for APR instruction	Supported	Not supported
Floating-point decimal instructions	Single-precision calculations and conversions	Supported (enabling standard deviation calculations)	Not supported
	Conversions between single-precision floating point and ASCII	Supported Floating point can be converted to ASCII for display on PTs ASCII text strings from measurement devices can be converted to floating-point decimal for use in calculations.	Not supported
	Double-precision calculations and conversions	Supported (enabling high-precision positioning)	Not supported
Text string, table data, and data shift instructions	Text string and table data processing instruction execution	Data processing can be performed normally or in the background (specified for each instruction) (Using time slices to process instruction over several cycles reduces the effect of these instructions on the cycle time.)	Normal processing only
	Stack insertions/deletions/ replacements and stack counts with table processing instructions	Supported Effective for tracking workpieces on conveyor lines.	Not supported
Data control instructions	PID with autotuning	Supported (eliminating the need to turn PID constants)	Not supported
Subroutine instructions	Global subroutines	Supported (GSBS, GSBN, and GRET instructions) Enables easier structuring of subroutines.	Not supported
Failure diagnosis instructions	Error log storage for FAL	Supported FAL can be executed without placing an entry in the error log. (Only system FAL errors will be placed in the error log.)	Not supported
	Error simulation with FAL/FALS	Supported Fatal and nonfatal errors can be simulated in the system to aid in debugging.	Not supported
Data comparison instructions	AREA RANGE COMPARE (ZCP) and DOUBLE RANGE COMPARE (ZCPL)	Supported	Not supported
Index register real I/O address conversion for CVM1/CV	Program and real I/O memory address compatibility with CVM1/CV-series PCs	CVM1/CV-series real I/O memory addresses can be converted to CJ-series addresses and placed in index registers or CJ-series real I/O memory addresses in index registers can be converted to CVM1/CV-series addresses.	Not supported

Item		CJ1-H CPU Unit (CJ1H-CPU6□H)	CJ1 CPU Unit (CJ1G-CPU4□)
Condition Flag saving and loading	Compatibility with CVM1/CV-series PCs	Condition Flag status can be saved or loading using the SAVE CONDITION FLAGS (CCS) and LOAD CONDITION FLAGS (CCL) instructions, enabling applications where Condition Flag status must be passed between different program locations, tasks, or cycles.	Not supported
Operation after Unit startup processing	CPU Unit startup	Starting or not starting (standby) the CPU Unit in MONITOR or RUN mode even if a Unit has not completed startup processing can be specified in the PC Setup.	CPU Unit standby (fixed)
Disabling power interruptions in program sections		Supported Instructions between DI and EI are executed without performing power OFF processing even if a power interruption has been detected and confirmed.	Not supported
Condition Flag operation		The statuses of the Equals, Negative, and Error Flags are maintained for execution of the following instructions. TIM, TIMH, TMHH, CNT, IL, ILC, JMP0, JME0, XCHG, XCGL, MOVR, input comparison instructions, CMP, CMPL, CPS, CPSL, TST, TSTN, STC, and CLC	The Equals, Negative, and Error Flags are turned OFF after executing the following instructions. TIM, TIMH, TMHH, CNT, IL, ILC, JMP0, JME0, XCHG, XCGL, MOVR, input comparison instructions, CMP, CMPL, CPS, CPSL, TST, TSTN, STC, and CLC

1-5 Function Tables

The following tables list functions for the CJ-series CPU Units (including both the CJ1 CPU Units and the CJ1-H CPU Units).

1-5-1 Functions Arranged by Purpose

Purpose		Function	Manual	Reference
Basic Operation and System Design	Studying system configuration	---> ---	*Operation Manual*	*SECTION 2 Specifications and System Configuration*
	Studying I/O allocations	---> ---		*SECTION 8 I/O Allocations and Data Exchange*
	Installation size	---> ---		*5-2-3 Assembled Appearance and Dimensions*
	Installation methods	---> ---		*5-2 Installation*
	Setting DIP switches	---> ---		*3-1-2 Components*
	Setting the PC Setup	---> ---		*7-1 PC Setup*
	Using Auxiliary Bits	---> ---		*Appendix B Auxiliary Area* and *9-10 Auxiliary Area*
	Studying the cycle time	---> ---		*Parallel Processing Mode*
	Troubleshooting	---> ---		*11-2-5 Error Messages*
Structured Programming	Standardizing programs as modules. Developing a program with several programmers working in parallel. Making the program easier to understand.	---> Program with tasks to divide the program, specify symbols, and define local and global symbols.	*Programming Manual* (W394)	*4-1 Tasks*
	Creating step programs.	---> Use the step instructions.	*Instructions Reference Manual* (W340)	Step Programming Instructions
	Using BASIC-like mnemonic instructions to program processes that are difficult to enter in the ladder diagram format (such as conditional branches and loops).	---> Use the block programming instructions.		Block Programming Instructions

Purpose		Function	Manual	Reference
Simplifying the Program	Creating looped program sections.	Use FOR(512) and NEXT(513) or JMP(004) and JME(005).	*Instructions Reference Manual* (W340)	Sequence Control Instructions
	Indirectly addressing DM words.	All words in the DM and EM Areas can be indirectly addressed.	*Programming Manual* (W394)	*6-2 Index Registers*
	Simplifying the program by switching to PC memory address specification.	Use Index Registers as pointers to indirectly address data area addresses. The Index Registers are very useful in combination with loops, increment instructions, and table data processing instructions. The auto-increment, auto-decrement, and offset functions are also supported.		
	Consolidating instruction blocks with the same pattern but different addresses into a single instruction block.	Use MCRO(099).	*Instructions Reference Manual* (W340)	MCRO(099) in the Subroutine Instructions
Managing the Cycle Time	Reducing the cycle time.	• Use tasks to put parts of the program that don't need to be executed into "standby" status. • Use JMP(004) and JME(005) to jump parts of the task that don't need to be executed. • Convert parts of the task to subroutines if they are executed only under particular conditions. • Disable a Unit's Special I/O Unit refreshing in the PC Setup if it isn't necessary to exchange data with that Special I/O Unit every cycle.	*Programming Manual* (W394)	*6-1 Cycle Time/High-speed Processing*
	Setting a fixed (minimum) cycle time.	Set a minimum cycle time in the PC Setup.		
	Setting a maximum cycle time. (Generating an error for a cycle time exceeding the maximum.)	Set a maximum cycle time (watch cycle time) in the PC Setup. If the cycle time exceeds this value, the Cycle Time Too Long Flag (A40108) will be turned ON and PC operation will be stopped.	*Operation Manual*	*7-1 PC Setup*
	Reducing the I/O response time for particular I/O points.	Use immediate refreshing or IORF(097).	*Programming Manual* (W394)	*6-1 Cycle Time/High-speed Processing*
	Finding I/O refresh times for individual Units	---	*Operation Manual*	*Parallel Processing Mode*
	Studying the I/O response time	---		*10-4-6 I/O Response Time*
	Finding the increase in the cycle time for online editing	---		*10-4-5 Online Editing Cycle Time Extension*
	Giving peripheral servicing priority over instruction execution	Use the Peripheral Servicing Priority Mode	*Programming Manual* (W394)	*6-6 Peripheral Servicing Priority Mode*

Purpose		Function	Manual	Reference
Using Interrupt Tasks	Monitoring operating status at regular intervals.	Use a scheduled interrupt task.	*Programming Manual* (W394)	*4-3 Interrupt Tasks*
	Issuing an interrupt to the CPU when data is received through serial communications.	Use a Serial Communications Units and external interrupt task.		
	Performing interrupt processing when an input goes ON.	Use an I/O interrupt task.		
	Executing an emergency interrupt program when the power supply fails.	Use a power OFF interrupt task. Enable the power OFF interrupt task in the PC Setup.		
	Studying the interrupt response time	---	*Operation Manual*	*10-4-7 Interrupt Response Times*
	Knowing the priority of interrupt tasks	---	*Programming Manual* (W394)	*4-3-2 Interrupt Task Priority*
Data Processing	Operating a FIFO or LIFO stack.	Use the stack instructions (FIFO(633) and LIFO(634)).	*Instructions Reference Manual* (W340)	Table Processing Instructions
	Performing basic operations on tables made up of 1-word records.	Use range instructions such as MAX(182), MIN(183), and SRCH(181).		
	Performing complex operations on tables made up of 1-word records.	Use Index Registers as pointers in special instructions.		
	Performing operations on tables made up of records longer than 1 word. (For example, the temperature, pressure, and other manufacturing settings for different models of a product could be stored in separate records.)	Use Index Registers and the record-table instructions.	*Programming Manual (W394)*	*6-2 Index Registers*
System Configuration and Serial Communications	Monitoring several different kinds of devices through the RS-232C port.	Multiple serial ports can be installed with Serial Communications Units (protocol macros).	*Operation Manual*	*2-5 Expanded System Configuration*
	Changing protocol during operation (from a modem connection to host link, for example).	Use STUP(237), the CHANGE SERIAL PORT SETUP instruction.	*Instructions Reference Manual* (W340)	Serial Communications Instructions

Purpose		Function	Manual	Reference
Connecting Programming Devices	Connecting a Programming Console.	Connect to the peripheral port with pin 4 of the CPU Unit's DIP switch OFF.	*Operation Manual*	*3-3 Programming Devices*
	Connecting a Programming Device (e.g., the CX-Programmer).	Connect to the peripheral port with pin 4 of the CPU Unit's DIP switch OFF or with pin 4 ON and the communications mode set to "peripheral bus" under Peripheral Port settings in the PC Setup. Connect to the RS-232C port with pin 5 of the CPU Unit's DIP switch ON or with pin 5 OFF and the communications mode set to "peripheral bus" under RS-232C Port settings in the PC Setup.		
	Connecting a host computer.	Connect to the RS-232C port or peripheral port. (Set the communications mode to "host link" in the PC Setup.)		*2-5 Expanded System Configuration*
	Connecting a PT.	Connect to the RS-232C port or peripheral port. (Set the communications mode to "NT Link" in the PC Setup.) Set the PT communications settings for a 1:N NT Link.		
	Connecting a standard serial device to the CPU Unit (no-protocol mode).	Connect to the RS-232C port. (Set the communications mode to "no-protocol" in the PC Setup.)		
Controlling Outputs	Turning OFF all outputs on basic Output Units and High-density Output Units (a type of Special I/O Unit).	Turn ON the Output OFF Bit (A50015).	*Programming Manual* (W394)	*6-4-2 Load OFF Functions*
	Maintaining the status of all outputs on Output Units when PC operation stops (hot start).	Turn ON the IOM Hold BIt (A50012).		*6-4-1 Hot Start/Hot Stop Functions*
Controlling I/O Memory	Maintaining the previous contents of all I/O Memory at the start of PC operation (hot start).	Turn ON the IOM Hold BIt (A50012).	*Programming Manual* (W394)	*6-4-1 Hot Start/Hot Stop Functions*
	Maintaining the previous contents of all I/O Memory when the PC is turned on.	Turn ON the IOM Hold BIt (A50012) and set the PC Setup to maintain the status of the IOM Hold Bit at start-up. (IOM Hold Bit Status at Startup)		

	Purpose		Function	Manual	Reference
File Memory	Automatically transferring the program, I/O Memory, and PC Setup from the Memory Card when the PC is turned on.	→	Enable the "automatic transfer at start-up" function by turning ON pin 2 of the CPU Unit's DIP switch and create an AUTOEXEC file.	*Programming Manual* (W394)	*SECTION 5 File Memory Functions*
	Creating a library of programs for different program arrangements.	→	Memory Card functions (Program Files)		
	Creating a library of parameter settings for various PC Racks and models.	→	Memory Card functions (Parameter Files)		
	Creating a library of data files with settings for various PC Racks and CPU Bus Units.	→	Memory Card functions (Data Files)		
	Storing I/O Comment data within the Memory Card.	→	Memory Card functions (Symbol Table Files)		
	Storing operating data (trend and quality data) within the CPU Unit during program execution.	→	EM File Memory Functions and the FREAD(700)/FWRIT(701) instructions		
	Switching PC operation.	→	Memory Card functions (Program Replacement during PC Operation)		
	Reading and writing I/O memory data with a spreadsheet.	→	Read/write data files using instructions in CSV or text format.		
Text string processing	Performing string processing at the PC which was performed at the host computer previously and reducing the program load at the host computer (operations such as read, insert, search, replace, and exchange).	→	Combine the Host Link function with the text string processing instructions.	*Instructions Reference Manual* (W340)	Text String Processing Instructions
	Performing string processing operations such as rearranging text strings.	→	Use the string comparison instructions and index registers.		
	Receiving data from external devices (such as bar code readers) through serial communications, storing the data in DM, and reading just the required string when it is needed.	→	Combine the protocol macro function with the text string processing instructions.		

Purpose		Function	Manual	Reference
Maintenance and Debugging	Changing the program while it is being executed.	Use the online editing function from a Programming Device. (Several instruction blocks can be changed with CX-Programmer.)	*Programming Manual* (W394)	*7-2-3 Online Editing*
	Sampling I/O Memory data. • Periodic sampling • Sampling at the end of each cycle • Sampling at execution of TRSM(045)	 → Data trace at regular intervals → Data trace at the end of each cycle → Data trace each time that TRSM(045) is executed		*7-2-4 Data Tracing*
	Specifying the start-up operating mode.	→ Set the PC Setup to specify the desired operating mode at start-up. (Startup Mode)		*6-4 Startup Settings and Maintenance*
	Recording the time that power was turned on, the last time that power was interrupted, the number of power interruptions, and the total PC on time.	→ These items are recorded automatically in the Auxiliary Area.		*6-4-5 Clock Functions*
	Stopping the program for instruction execution errors.	→ Set the PC Setup so that instruction errors are treated as fatal errors. (Instruction Error Operation)		*2-3-3 Checking Programs*
	Programming/monitoring the PC remotely. • Programming or monitoring a PC on the network through Host Link. • Programming or monitoring a PC through modems.	 → Host Link → Network Gateway function → Host Link through modems	*Operation Manual*	*2-5 Expanded System Configuration*
	Programming/monitoring PCs in other networks	→ Communicate with PCs up to 2 network levels away through Controller Link or Ethernet.		
Error Processing and Troubleshooting	Generating a non-fatal or fatal error for user-defined conditions. • Non-fatal errors (Operation continues.) • Fatal errors (PC operation stops.)	 → FAILURE ALARM: FAL(006) → SEVERE FAILURE ALARM: FALS(007)	*Programming Manual* (W394)	*6-5 Diagnostic and Debugging Functions*
	Analyzing time and logic in execution of an instruction block.	→ FAILURE POINT DETECTION: FPD(269)		
	Record information about errors, including user-defined errors, in the error log.	→ Use the error log function. Up to 20 error records can be stored.		

Purpose			Function	Manual	Reference
Other Functions	Protecting the program.	→	Write-protect the user program memory.	*Programming Manual* (W394)	6-4 Startup Settings and Maintenance
	Allocating words in the I/O Area by specifying the first word allocated to each Rack.	→	Set the first word allocated to each Rack by registering the I/O table from the CX-Programmer. (Words must be allocated to Racks in the order that the Racks are connected.)		*6-7 Other Functions*
	Reducing input chattering and the effects of noise.	→	Specify the input response times for Basic I/O Units in the PC Setup. (Basic I/O Unit Input Response Time)		

1-5-2 Communications Functions (Serial/Network)

Purpose			Protocol: Required Equipment	Reference
Monitoring from the Host Computer	RS-232C or RS-422/485	→	Host Link: Port in the CPU Unit or Serial Communications Unit	*2-5 Expanded System Configuration*
	Host Link communications from the PC	→	Enclose a FINS command with a Host Link header and terminator and issue it from the PC as a network communications instruction.	
	Network communications through RS-232C or RS-422/485	→	Controller Link and Ethernet communications are possible through the Host Link. (Enclose a FINS command with a Host Link header and terminator and issue it from the PC as a network communications instruction.)	
	Network: Control system	→	Controller Link: Controller Link Unit	
	Network: Information system	→	Ethernet: Ethernet Unit	
Connecting to a Standard Serial Device	Creating a simple protocol	→	Protocol Macros: Serial Communications Unit	
	High-speed data exchange	→		
	No protocol	→	No protocol: CPU Unit's RS-232C port, or Protocol Macro	
Communicating with a PT	Direct access	→	NT Link: Port in the CPU Unit or Serial Communications Unit	
Data Link between PCs	High capacity or free word allocation	→	Controller Link: Controller Link Unit	
Data Link between PC and computer		→	Controller Link: Controller Link Unit	
Message communications between PCs	Normal or high capacity	→	Controller Link: Controller Link Unit	
	Information system	→	Ethernet: Ethernet Unit	
Message communications between PC and computer	Control system	→	Controller Link: Controller Link Unit	
	Information system	→	Ethernet: Ethernet Unit	

Purpose			Protocol: Required Equipment	Reference
Remote I/O between PC and Slaves	High-density I/O	→	DeviceNet: DeviceNet Master Unit and required Slave Units	*2-5-3 Communications Network System*
	Free word allocation	→		
	Multi-vendor capability	→		
	Analog I/O capability	→		
	Multi-level architecture	→		
	High-speed Remote I/O	→	CompoBus/S: CompoBus/S Master Unit and required Slave Units	

1-6 CJ1-H Functions Arranged by Purpose

Purpose		Function
Increasing speed	Increasing the speed of both the instruction execution cycle and peripheral servicing. • Fast large-scale data exchange with the host are needed even though the PC program is very large. • Consistently timed data exchange with SCADA software is needed. • It is necessary to minimize the effects on the cycle time of future system expansion or increases in communications.	Use the Parallel Processing Mode with Synchronous Memory Access or Parallel Processing Mode with Asynchronous Memory Access. Using parallel processing enables the following savings. For example, if the program consists of basic instructions with a cycle time of approximately 10 ms and one Ethernet Unit is being used, the cycle time will be reduced to approximately 90% of the time for the normal mode. and the peripheral servicing time will be reduced to approximately 40% of the time for the normal mode.
	Maintaining concurrency in the I/O memory data accessed for instruction execution and for peripheral servicing (for data larger than one word).	Use the Parallel Processing Mode with Synchronous Memory Access.
	Not necessarily maintaining concurrency in the I/O memory data accessed for instruction execution and for peripheral servicing (for data larger than one word).	Use the Parallel Processing Mode with Asynchronous Memory Access.
	Giving priority to peripheral servicing over the instruction execution cycle (For example, to give priority to the read/write response of CPU Unit data from SCADA software for process control)	The response of peripheral servicing can be adjusted by using the following modes (listed in order from highest response): Parallel Processing Mode with Asynchronous Memory Access, Peripheral Servicing Priority Mode (with a long instruction execution cycle), Parallel Processing Mode with Synchronous Memory Access, Normal Mode
	Specifying where index and data registers are used independently by task for shared by tasks	Set the program properties from the CX-Programmer to independent (default) or shared registers.
	Minimizing cycle time fluctuations and maintaining consistent I/O response even when extensive table data and text string data is being processed	Table data processing and text string processing, which often require time, can be set in the PC Setup so that they are processed in the background. The default is for no background execution. (For background execution, time slicing is used to separate processing over several cycles.) If background execution is used, the effect on the cycle time can be limited to 4% or less (PC Setup default setting).
	Improving data link response with a long cycle time	The CPU BUS UNIT I/O REFRESH instruction (DLNK(226)) can be used at one or more locations in the ladder program. This enables refreshing data links for specified Controller Link or SYSMAC LINK Units, whenever necessary, as well as during the I/O refresh period. (The actual data that is refreshed depends on the communications cycle time.)
	Improving DeviceNet remote I/O response	The CPU BUS UNIT I/O REFRESH instruction (DLNK(226)) can be used at one or more locations in the ladder program. This enables refreshing remote I/O for DeviceNet Units, whenever necessary, as well as during the I/O refresh period. (The actual data that is refreshed depends on the communications cycle time.)
	Improving the response of protocol macro data transfers for Serial Communications Units	The CPU BUS UNIT I/O REFRESH instruction (DLNK(226)) can be used at one or more locations in the ladder program. This enables refreshing data transferred for protocol macros executed by Serial Communications Units, whenever necessary, as well as during the I/O refresh period. (The actual data that is refreshed depends on the communications cycle time.)
	Immediately refreshing status data and other words allocated to CPU Bus Units in the CIO Area whenever necessary (including Ethernet Units, Serial Communications Units, Controller Link Units, etc.)	The CPU BUS UNIT I/O REFRESH instruction (DLNK(226)) can be used at one or more locations in the ladder program. This enables refreshing words allocated to CPU Bus Units in the CIO Area (25 words) whenever necessary, in the same way that the IORF instruction is used for other Units.

Purpose		Function
Increasing structure	Using more tasks	Define interrupt tasks as cyclic tasks (called “extra cyclic tasks”).
	Reducing the cycle time even with structured programs using many tasks	Use shared index and data registers.
	Using the same index or data registers in different tasks without saving and loading register contents	
	Initializing processing when a task is started	Use the Task Start Flags.
	Using standard processing shared by more than one task	Use a global subroutine (GSBN to GRET) in interrupt task number 0.
	Standardization and program structure based on subroutines	Increase speed using subroutine instructions (SBS, SBN, and RET) and global subroutine instructions (GSBS, GSBN, and GRET)
Special applications	Displaying floating-point decimal data on a PT	Use the FLOATING- POINT TO ASCII instruction.
	Using text string data from measurement devices in calculations	Use the ASCII TO FLOATING-POINT instruction.
	Performing high-precision positioning, e.g., for XY tables	Use the Double-precision Floating-point instructions.
	Managing information on workpieces flowing on a conveyer in realtime in table form, e.g., when workpieces are added or removed from the conveyor during processing	Use the stack instructions. STACK DATA READ, STACK DATA OVERWRITE, STACK DATA INSERT, and STACK DATA DELETE (Operate on a specified element in the stack.) STACK SIZE READ (Counts the number of elements in the stack.)
	Performing high-precision linear approximations, e.g., converting a level meter reading in mm to a capacity value in liters according to the shape of a tank	Use the ARITHMETIC PROCESS instruction (unsigned 16-bit binary/BCD data, signed 16/32-bit binary data, or single-precision floating-point data can be used for line data).
	Autotuning PID constants (particularly to automatically tune PID constants and start the system faster when using multiloop PID)	Use the PID CONTROL WITH AUTO TUNING instruction.
	Saving and loading execution results (e.g., from comparison instructions) at different locations in a task or in different tasks	Use the SAVE CONDITION FLAGS (CCS) and LOAD CONDITION FLAGS (CCL) instructions to save the current status of the Condition Flags or load the previous status.
	Using a CVM1/CV-series program containing real I/O memory addresses in a CJ-series CPU Unit	Use the CONVERT ADDRESS FROM CV (FRMCV) instruction.
	Using I/O memory tables containing CVM1/CV-series real I/O memory addresses (e.g., to return the data to a CVM1/CV-series CPU Unit after processing by the CJ-series CPU Unit).	Use the CONVERT ADDRESS TO CV (TOCV) instruction.
	Disabling power interruptions during specific regions of the program	Create program sections for which power interrupts have been disabled with the DI and EI instructions (set A530 to A5A5 Hex).

Purpose		Function
Debugging and maintenance	Not including user-defined FAL errors in the error log, e.g., when monitoring errors on a PT (System FAL errors will be included.)	Set the PC Setup to not include user-defined FAL errors in the error log.
	Simulating errors in the CPU Unit when debugging the system, e.g., to check error messages displayed on a PT	Use FAL/FALS to simulate fatal and nonfatal system errors.
	Backing up data from Units other than the CPU Unit, e.g., DeviceNet Units, Serial Communications Units, etc.	Use the simple backup operation, which includes data from specific Units (including device parameters from DeviceNet Units, protocol macro data from Serial Communications Units, etc.).
	Finding errors occurring when creating I/O tables	Use the detailed error information for I/O table creation stored in the AR Area.
	Using battery-free operation (ROM operation) without a Memory Card	Use the automatic program/parameter area backup function to flash memory in the CPU Unit.
	Starting CPU Unit operation without waiting for Units with long startup times to complete startup processing	Use the startup condition settings (allowing the CPU Unit to startup immediately in RUN or MONITOR mode even when startup processing has not been completed for other Units).

1-7 Comparison to CS-series PCs

The CS-series and CJ-series PCs use the same architecture and are basically the same in terms of program structure (tasks), instruction system, I/O memory, and other functionality. They do differ, however in that the CJ-series PCs have a different Unit structure, support different Units, do not support Inner Boards, have different Expansion Racks, have a different I/O allocation method, etc. These differences are outlined in the following table.

Item		CJ-series PCs, CJ1-H CPU Units	CS-series PCs, CS1-H CPU Units
Dimensions: Height x width		90 x 65 mm	130 x 123 mm
Unit connections		Connected to each other via connectors. End Cover connected to right end to indicate end of Rack.	Mounted to Backplanes.
Maximum I/O capacity		2,560 I/O points	5,120 I/O points
Maximum program capacity		120 Ksteps	250 Ksteps
Maximum data memory (DM and EM Areas combined)		256 Kwords	448 Kwords
Instructions system		Same	
I/O memory		Same	
PC Setup		Same	
Cyclic task functionality		Same	
Interrupt tasks		Same (Power OFF interrupt task, schedule interrupt tasks, I/O interrupt, and external interrupt tasks)	
Programming Devices		CX-Programmer (versions 2.1 or later) and Programming Consoles	
Instruction execution time	Basic instructions	0.02 μs min.	
	Special instructions	0.06 μs min	
Overhead time		0.3 ms	
Mounting		DIN Track (not mountable with screws)	DIN Track or screws
Inner Boards		Not supported.	Supported.
Special I/O Units and CPU Bus Units		Structure of allocations is the same. Special I/O Units: 96 Units max. (restrictions on mounting positions) CPU Bus Units: 16 Units max.	
CPU Rack mounting positions		10 Units max. (11 Units or more will cause an error)	3, 5, 8, or 10 slots
Expansion Rack mounting positions		10 Units max. (11 Units or more will cause an error)	2, 3, 5, 8, or 10 slots
Expansion Racks		One I/O Control Unit required on CPU Rack and one I/O Interface Unit required on each Expansion Rack.	Either C200H or CS-series Expansion Racks can be connected without an I/O Control Unit or I/O Interface Units.
Maximum number of Expansion Racks		3	7
Maximum total cable length to Expansion Racks		12 m	
Maximum number of Units		40	80
SYSMAC BUS Remote I/O		Not supported.	Supported.
File Memory (Memory Cards or EM Area)		Same	
Trace Memory		Same	
I/O allocation		Automatic allocation from right to left starting at Unit closest to CPU Unit and then right to left on Expansion Racks.	Automatic allocation from right to left starting at Unit closest to CPU Unit and then right to left on Expansion Racks.

Item		CJ-series PCs, CJ1-H CPU Units	CS-series PCs, CS1-H CPU Units
Registered I/O tables	Support	Supported (but operation is possible without creating I/O tables from a Programming Device).	Supported (must be created from Programming Device).
	Modes	Either user-set I/O tables or automatic I/O allocation at startup (no I/O table verification). The default setting is for Automatic I/O Allocation at Startup. User-set I/O tables can be automatically used by setting and transferring I/O tables (or parameter file). If the I/O tables are deleted from a CPU Unit from the CX-Programmer, Automatic I/O Allocation at Startup will be used again.	Only user-specified I/O tables (I/O tables can be verified against actual I/O)
	Allocating unused words	Possible only by using user-set I/O tables (set by editing I/O tables on the CX-Programmer and transferring them to the CPU Unit).	Always possible. (Set by editing I/O tables on the CX-Programmer and transferring them to the CPU Unit.)
Discrepancies between registered I/O tables and actual I/O		I/O setting error occurs (fatal error). (Without Backplanes and due to the physical connection method, it is essentially impossible for a Unit to fall off or for an empty position to be created. Discrepancies between the registered I/O tables and actual I/O are thus considered to be far more serious.)	I/O verify error occurs (non-fatal error).
Setting first word on each Rack		Supported.	Supported.
Startup Mode when a Programming Console is not mounted and the PC Setup is set to use operating mode specified on the Programming Console		RUN mode	
Serial communications ports		One peripheral port and one RS-232C port.	
Serial communications modes	Peripheral port	Same: Peripheral bus, Programming Console, Host Link, 1:N NT Link	
	RS-232C port	Same: Peripheral bus, Host Link, 1:N NT Link, no protocol	
Communications commands		FINS commands, Host Link commands	
Index registers		Same	
Diagnostic functions		Same	
Error log function		Same	
Debugging functions		Same (Force-set/reset, differential monitor, data traces, instruction error traces)	
I/O response time setting functions		Same	
Battery		CPM2A-BAT01	CS1W-BAT01

SECTION 2
Specifications and System Configuration

This section provides tables of standard models, Unit specifications, system configurations, and a comparison between different Units.

2-1 Specifications

2-1-1 Performance Specifications

CJ1-H CPU Units

CPU	CJ1H-CPU66H	CJ1H-CPU65H	CJ1G-CPU45H	CJ1G-CPU44H	CJ1G-CPU43H	CJ1G-CPU42H
I/O bits	2,560		1,280		960	
User program memory (See note.)	120 Ksteps	60 Ksteps	60 Ksteps	30 Ksteps	20 Ksteps	10 Ksteps
Data memory	32 Kwords					
Extended data memory	32Kwords x 7 banks E0_00000 to E6_32767	32Kwords x 3 banks E0_00000 to E2_32767	32Kwords x 3 banks E0_00000 to E2_32767	32Kwords x 1 banks E0_00000 to E0_32767		
Current consumption	0.82 A at 5 VDC		0.78 A at 5 VDC			

CJ1 CPU Units

CPU	CJ1G-CPU45	CJ1G-CPU44
I/O bits	1,280	
User program memory (See note.)	60 Ksteps	30 Ksteps
Data memory	32 Kwords	
Extended data memory	32 Kwords x 3 banks E0_00000 to E2_32767	32 Kwords x 1 bank E0_00000 to E0_32767
Current consumption	0.91 A at 5 V DC	

Note The number of steps in a program is not the same as the number of instructions. For example, LD and OUT require 1 step each, but MOV(021) requires 3 steps. The program capacity indicates the total number of steps for all instructions in the program. Refer to *10-5 Instruction Execution Times and Number of Steps* for the number of steps required for each instruction.

Common Specifications

Item	Specification	Reference
Control method	Stored program	---
I/O control method	Cyclic scan and immediate processing are both possible.	---
Programming	Ladder diagram	---
CPU processing mode	CJ1-H CPU Units: Normal Mode, Parallel Processing Mode with Asynchronous Memory Access, Parallel Processing Mode with Asynchronous Memory Access, or Peripheral Servicing Priority Mode CJ1 CPU Units: Normal Mode or Peripheral Servicing Priority Mode	---
Instruction length	1 to 7 steps per instruction	*10-5 Instruction Execution Times and Number of Steps*
Ladder instructions	Approx. 400 (3-digit function codes)	---
Execution time	CJ1-H CPU Units: Basic instructions: 0.02 μs min. Special instructions: 0.06 μs min. CJ1 CPU Units: Basic instructions: 0.08 μs min. Special instructions: 0.12 μs min.	*10-5 Instruction Execution Times and Number of Steps*
Overhead time	CJ1-H CPU Units: Normal mode: 0.3 ms min. Parallel processing: 0.3 ms min. CJ1 CPU Units: 0.5 ms min.	---

Item	Specification	Reference
Unit connection method	No Backplane: Units connected directly to each other.	---
Mounting method	DIN Track (screw mounting not possible)	*5-2-6 DIN Track Installation*
Maximum number of connectable Units	Per CPU or Expansion Rack: 10 Units including Basic I/O Units, Special I/O Units, and CPU Bus Units. Total per PC: 10 Units on CPU Rack and 10 Units each on 3 Expansion Racks = 40 Units total	---
Maximum number of Expansion Racks	3 total (An I/O Control Unit is required on the CPU Rack and an I/O Interface Unit is required on each Expansion Rack.)	*2-3-2 CJ-series Expansion Racks*
Number of tasks	288 (cyclic tasks: 32, interrupt tasks: 256) With CJ1-H CPU Units, interrupt tasks can be defined as cyclic tasks called “extra cyclic tasks.” Including these, up to 288 cyclic tasks can be used. **Note** Cyclic tasks are executed each cycle and are controlled with TKON(820) and TKOF(821) instructions. **Note** The following 2 types of interrupt tasks are supported. The following 4 types of interrupt tasks are supported. Power OFF interrupt tasks: 1 max. Scheduled interrupt tasks: 2 max. I/O interrupt tasks: 32 max. External interrupt tasks: 256 max.	*Programming Manual: 1-3 Programs and Tasks* *Programming Manual: SECTION 4: Tasks*
Interrupt types	Scheduled Interrupts: Interrupts generated at a time scheduled by the CPU Unit’s built-in timer. I/O Interrupts: Interrupts from Interrupt Input Units. Power OFF Interrupts: Interrupts executed when the CPU Unit’s power is turned OFF. External I/O Interrupts: Interrupts from the Special I/O Units or CPU Bus Units.	*Programming Manual: 4-3 Interrupt Tasks*
Calling subroutines from more than one task	CJ1-H CPU Units: Supported (called “global subroutines). CJ1 CPU Units: Not supported.	Tasks: *Programming Manual* (W394)

<table>
<tr><th colspan="2">Item</th><th colspan="2">Specification</th><th>Reference</th></tr>
<tr><td rowspan="5">CIO (Core I/O) Area</td><td>I/O Area</td><td>1,280: CIO 000000 to CIO 007915 (80 words from CIO 0000 to CIO 0079)
The setting of the first word can be changed from the default (CIO 0000) so that CIO 0000 to CIO 0999 can be used.
I/O bits are allocated to Basic I/O Units.</td><td rowspan="4">The CIO Area can be used as work bits if the the bits are not used as shown here.</td><td>9-3 I/O Area</td></tr>
<tr><td>Link Area</td><td>3,200 (200 words): CIO 10000 to CIO 119915 (words CIO 1000 to CIO 1199)
Link bits are used for data links and are allocated to Units in Controller Link Systems.</td><td>9-4 Data Link Area
2-5-3 Communications Network System
Controller Link Unit Operation Manual (W309)</td></tr>
<tr><td>CPU Bus Unit Area</td><td>6,400 (400 words): CIO 150000 to CIO 189915 (words CIO 1500 to CIO 1899)
CPU Bus Unit bits store the operating status of CPU Bus Units.
(25 words per Unit, 16 Units max.)</td><td>9-5 CPU Bus Unit Area
Operation Manual for each CPU Bus Unit</td></tr>
<tr><td>Special I/O Unit Area</td><td>15,360 (960 words): CIO 200000 to CIO 295915 (words CIO 2000 to CIO 2959)
Special I/O Unit bits are allocated to Special I/O Units.
(10 words per Unit, 96 Units max.)
Note Special I/O Units are I/O Units that belong to a special group called “Special I/O Units.” Examples: CJ1W-AD081 Analog Input Unit</td><td>9-6 Special I/O Unit Area
Operation Manual for each Special I/O Unit</td></tr>
<tr><td>DeviceNet Area</td><td>9,600 (600 words): CIO 320000 to CIO 379915 (words CIO 3200 to CIO 3799)
DeviceNet bits are allocated to Slaves for DeviceNet Unit remote I/O communications when the master function is used with fixed allocations.
<table><tr><td>Fixed allocation setting 1</td><td>Outputs: CIO 3200 to CIO 3263
Inputs: CIO 3300 to CIO 3363</td></tr><tr><td>Fixed allocation setting 2</td><td>Outputs: CIO 3400 to CIO 3463
Inputs: CIO 3500 to CIO 3563</td></tr><tr><td>Fixed allocation setting 3</td><td>Outputs: CIO 3600 to CIO 3663
Inputs: CIO 3700 to CIO 3763</td></tr></table>The following words are allocated to the master function even when the DeviceNet Unit is used as a slave.
<table><tr><td>Fixed allocation setting 1</td><td>Outputs: CIO 3370 (slave to master)
Inputs: CIO 3270 (master to slave)</td></tr><tr><td>Fixed allocation setting 2</td><td>Outputs: CIO 3570 (slave to master)
Inputs: CIO 3470 (master to slave)</td></tr><tr><td>Fixed allocation setting 3</td><td>Outputs: CIO 3770 (slave to master)
Inputs: CIO 3670 (master to slave)</td></tr></table></td><td>DeviceNet Unit Operation Manual (W380)</td></tr>
<tr><td>Internal I/O Area</td><td colspan="2">4,800 (300 words): CIO 120000 to CIO 149915 (words CIO 1200 to CIO 1499)
37,504 (2,344 words): CIO 380000 to CIO 614315 (words CIO 3800 to CIO 6143)
These bits in the CIO Area are used as work bits in programming to control program execution. They cannot be used for external I/O.</td><td>9-2-2 Overview of the Data Areas</td></tr>
</table>

Item	Specification	Reference
Work Area	8,192 bits (512 words): W00000 to W51115 (W000 to W511) Controls the programs only. (I/O from external I/O terminals is not possible.) **Note** When using work bits in programming, use the bits in the Work Area first before using bits from other areas.	*9-2-2 Overview of the Data Areas* *9-7 DeviceNet Area*
Holding Area	8,192 bits (512 words): H00000 to H51115 (H000 to H511) Holding bits are used to control the execution of the program, and maintain their ON/OFF status when the PC is turned OFF or the operating mode is changed.	*9-2-2 Overview of the Data Areas* *9-9 Holding Area*
Auxiliary Area	Read only: 7,168 bits (448 words): A00000 to A44715 (words A000 to A447) Read/write: 8,192 bits (512 words): A44800 to A95915 (words A448 to A959) Auxiliary bits are allocated specific functions.	*9-2-2 Overview of the Data Areas* *9-10 Auxiliary Area*
Temporary Area	16 bits (TR0 to TR15) Temporary bits are used to temporarily store the ON/OFF execution conditions at program branches.	*9-2-2 Overview of the Data Areas* *9-11 TR (Temporary Relay) Area*
Timer Area	4,096: T0000 to T4095 (used for timers only)	*9-2-2 Overview of the Data Areas* *9-12 Timer Area*
Counter Area	4,096: C0000 to C4095 (used for counters only)	*9-2-2 Overview of the Data Areas* *9-13 Counter Area*
DM Area	32K words: D00000 to D32767 Used as a general-purpose data area for reading and writing data in word units (16 bits). Words in the DM Area maintain their status when the PC is turned OFF or the operating mode is changed. Internal Special I/O Unit DM Area: D20000 to D29599 (100 words × 96 Units) Used to set parameters for Special I/O Units. CPU Bus Unit DM Area: D30000 to D31599 (100 words × 16 Units) Used to set parameters for CPU Bus Units.	*9-2-2 Overview of the Data Areas* *9-14 Data Memory (DM) Area*
EM Area	32K words per bank, 3 banks max.: E0_00000 to E2_32767 max. (depending on model of CPU Unit) Used as a general-purpose data area for reading and writing data in word units (16 bits). Words in the EM Area maintain their status when the PC is turned OFF or the operating mode is changed. The EM Area is divided into banks, and the addresses can be set by either of the following methods. Changing the current bank using the EMBC(281) instruction and setting addresses for the current bank. Setting bank numbers and addresses directly. EM data can be stored in files by specifying the number of the first bank.	*9-2-2 Overview of the Data Areas* *9-15 Extended Data Memory (EM) Area*
Index Registers	IR0 to IR15 Store PC memory addresses for indirect addressing. Index registers can be used independently in each task. One register is 32 bits (2 words). CJ1 CPU Units: Index registers used independently in each task. CJ1-H CPU Units: Setting to use index registers either independently in each task or to share them between tasks.	*9-16 Index Registers* *Programming Manual: 6-2 Index Registers*
Task Flag Area	32 (TK0000 to TK0031) Task Flags are read-only flags that are ON when the corresponding cyclic task is executable and OFF when the corresponding task is not executable or in standby status.	*9-18 Task Flags* *Programming Manual: 4-2-3 Flags Related to Cyclic Tasks*

Item	Specification	Reference
Trace Memory	4,000 words (trace data: 31 bits, 6 words)	*Programming Manual: 7-2-4 Tracing Data*
File Memory	Memory Cards: Compact flash memory cards can be used (MS-DOS format). EM file memory: Part of the EM Area can be converted to file memory (MS-DOS format). OMRON Memory Cards can be used.	*Programming Manual: SECTION 5: File Memory Functions*

Function Specifications

Item	Specification	Reference
Constant cycle time	1 to 32,000 ms (Unit: 1 ms) When a Parallel Processing Mode is used for a CJ1-H CPU Unit, the cycle time for executing instructions is constant.	*10-4 Computing the Cycle Time* *Programming Manual: 6-1-1 Minimum Cycle Time*
Cycle time monitoring	Possible (Unit stops operating if the cycle is too long): 10 to 40,000 ms (Unit: 10 ms) When a Parallel Processing Mode is used for a CJ1-H CPU Unit, the instruction execution cycle is monitored. CPU Unit operation will stop if the peripheral servicing cycle time exceeds 2 s (fixed).	*10-4 Computing the Cycle Time* *Programming Manual: 6-1-2* Maximum Cycle Time (Watch Cycle Time) and *6-1-3 Cycle Time Monitoring*
I/O refreshing	Cyclic refreshing, immediate refreshing, refreshing by IORF(097). IORF(097) refreshes I/O bits allocated to Basic I/O Units and Special I/O Units. With the CJ1-H CPU Units, the CPU BUS UNIT I/O REFRESH (DLNK(226)) instruction can be used to refresh bits allocated to CPU Bus Units in the CIO and DM Areas.	*10-4 Computing the Cycle Time* *Programming Manual: 6-1-6 I/O Refresh Methods*
Timing of special refreshing for CPU Bus Units	Data links for Controller Link Units and SYSMAC LINK Units, remote I/O for DeviceNet Units, and other special refreshing for CPU Bus Units is performed at the following times: CJ1 CPU Units: I/O refresh period CJ1-H CPU Units: I/O refresh period and when the CPU BUS UNIT I/O REFRESH (DLNK(226)) instruction is executed.	*10-4 Computing the Cycle Time*
I/O memory holding when changing operating modes	Depends on the ON/OFF status of the IOM Hold Bit in the Auxiliary Area.	*SECTION 9 Memory Areas* *9-2-3 Data Area Properties* *Programming Manual: 6-4-1 Hot Start/Cold Start Function*
Load OFF	All outputs on Output Units can be turned OFF when the CPU Unit is operating in RUN, MONITOR, or PROGRAM mode.	*Programming Manual: 6-5-2 Load OFF Function* and *7-2-3 Online Editing*
Input response time setting	Time constants can be set for inputs from Basic I/O Units. The time constant can be increased to reduce the influence of noise and chattering or it can be decreased to detect shorter pulses on the inputs.	*10-4-6 I/O Response Time* *Programming Manual: 6-6-1 I/O Response Time Settings*
Mode setting at power-up	Possible (By default, the CPU Unit will start in RUN mode if a Programming Console is not connected.)	*7-1-2 PC Setup Settings* *Programming Manual: 1-2 Operating Modes* and *1-2-3 Startup Mode*

Item	Specification		Reference
Flash memory (CJ1-H CPU Units only)	The user program and parameter area data (e.g., PC Setup) are always backed up automatically in flash memory. (automatic backup and restore.)		---
Memory Card functions	Automatically reading programs (autoboot) from the Memory Card when the power is turned ON.	Possible	*3-2 File Memory* *Programming Manual: SECTION 5 File Memory Functions, 5-1-3 Files*, and *5-2-2 CMND Instruction*
	Program replacement during PC operation	Possible	*Programming Manual: 5-2-3 Using Instruction in User Program*
	Format in which data is stored in Memory Card	User program: Program file format PC Setup and other parameters: Data file format I/O memory: Data file format (binary format), text format, or CSV format	*Programming Manual: 5-1 File Memory*
	Functions for which Memory Card read/write is supported	User program instructions, Programming Devices (including CX-Programmer and Programming Consoles), Host Link computers, AR Area control bits, easy backup operation	*Programming Manual:* 5-2 File Memory Operations
Filing	Memory Card data and the EM (Extended Data Memory) Area can be handled as files.		*Programming Manual: SECTION 5 File Memory Functions*
Debugging	Control set/reset, differential monitoring, data tracing (scheduled, each cycle, or when instruction is executed), instruction error tracing, storing location generating error when a program error occurs.		*Programming Manual: 7-2 Trial Operation and Debugging*
Online editing	User programs can be overwritten in program-block units when the CPU Unit is in MONITOR or PROGRAM mode. This function is not available for block programming areas. With the CX-Programmer, more than one program block can be edited at the same time.		*Programming Manual: 1-2 Operating Modes* and *7-2-3 Online Editing*
Program protection	Overwrite protection: Set using DIP switch. Copy protection: Password set using CX-Programmer or Programming Consoles.		*Programming Manual: 6-4-6 Program Protection*
Error check	User-defined errors (i.e., user can define fatal errors and non-fatal errors) The FPD(269) instruction can be used to check the execution time and logic of each programming block. FAL and FALS instructions can be used with the CJ1-H CPU Units to simulate errors.		*11-2-5 Error Messages* *Programming Manual: 6-5 Diagnostic Functions* and *6-5-3 Failure Alarm Functions*
Error log	Up to 20 errors are stored in the error log. Information includes the error code, error details, and the time the error occurred. A CJ1-H CPU Unit can be set so that user-defined FAL errors are not stored in the error log.		*Programming Manual: 6-4-1 Error Log*
Serial communications	Built-in peripheral port: Programming Device (including Programming Console) connections, Host Links, NT Links Built-in RS-232C port: Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links		*2-5-1 Serial Communications System* *Programming Manual: 6-3 Serial Communications Functions*
	Serial Communications Unit (sold separately): Protocol macros, Host Links, NT Links		

Item	Specification	Reference
Clock	Provided on all models. Accuracy: Ambient temperature — Monthly error 55°C: −3.5 min to +0.5 min 25°C: −1.5 min to +1.5 min 0°C: −3 min to +1 min **Note** Used to store the time when power is turned ON and when errors occur.	*Programming Manual: 6-4-5 Clock Functions*
Power OFF detection time	10 to 25 ms (not fixed)	*10-3 Power OFF Operation*
Power OFF detection delay time	0 to 10 ms (user-defined, default: 0 ms)	*Programming Manual: 6-4-4 Power OFF Detection Delay Time*
Memory protection	Held Areas: Holding bits, contents of Data Memory and Extended Data Memory, and status of the counter Completion Flags and present values. **Note** If the IOM Hold Bit in the Auxiliary Area is turned ON, and the PC Setup is set to maintain the IOM Hold Bit status when power to the PC is turned ON, the contents of the CIO Area, the Work Area, part of the Auxiliary Area, timer Completion Flag and PVs, Index Registers, and the Data Registers will be saved for up to 20 days.	*9-2-3 Data Area Properties*
Sending commands to a Host Link computer	FINS commands can be sent to a computer connected via the Host Link System by executing Network Communications Instructions from the PC.	*2-5-2 Systems*
Remote programming and monitoring	Host Link communications can be used for remote programming and remote monitoring through a Controller Link System or Ethernet network.	*2-5-3 Communications Network System* *Programming Manual: 6-4-7 Remote Programming and Monitoring*
Three-level communications	Host Link communications can be used for remote programming and remote monitoring from devices on networks up to two levels away (Controller Link Network, Ethernet Network, or other network).	*2-5-2 Systems*
Storing comments in CPU Unit	I/O comments can be stored in the CPU Unit in Memory Cards or EM file memory.	*Programming Manual: 5-1-5 Applications* *CX-Programmer User Manual: I/O Comments*
Program check	Program checks are performed at the beginning of operation for items such as no END instruction and instruction errors. CX-Programmer can also be used to check programs.	*Programming Manual: 2-3 Checking Programs*
Control output signals	RUN output: The internal contacts will turn ON (close) while the CPU Unit is operating (CJ1W-PA205R).	*Programming Manual: 6-4-3 RUN Output*
Battery life	Refer to *12-2 Replacing User-serviceable Parts.* Battery Set: CPM2A-BAT01	*12-1-2 Unit Replacement Precautions*
Self-diagnostics	CPU errors (watchdog timer), I/O bus errors, memory errors, and battery errors.	*11-2-5 Error Messages*
Other functions	Storage of number of times power has been interrupted. (Stored in A514.)	*10-3 Power OFF Operation*

2-1-2 General Specifications

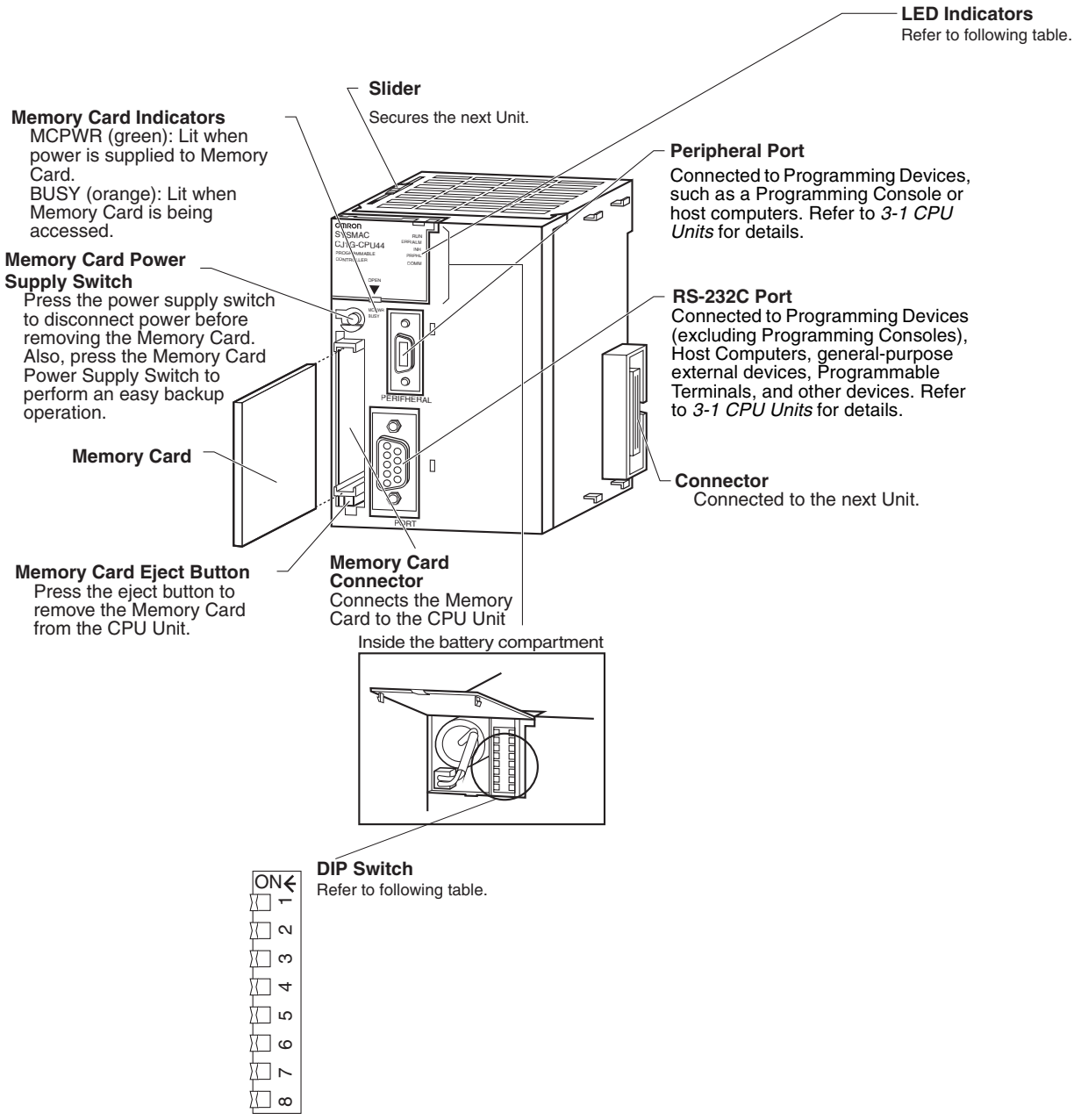
Item	Specifications		
Power Supply Unit	CJ1W-PA205R	CJ1W-PA202	CJ1W-PD025
Supply voltage	100 to 240 V AC (wide-range), 50/60 Hz		24 V DC
Operating voltage and frequency ranges	85 to 264 V AC, 47 to 63 Hz		19.2 to 28.8 V DC
Power consumption	100 VA max.	50 VA max.	50 W max.
Inrush current (See note 3.)	At 100 to 120 V AC: 15 A/8 ms max. for cold start at room temperature At 200 to 240 V AC: 30 A/8 ms max. for cold start at room temperature	At 100 to 120 V AC: 20 A/8 ms max. for cold start at room temperature At 200 to 240 V AC: 40 A/8 ms max. for cold start at room temperature	At 24 V DC: 30 A/2 ms max. for cold start at room temperature
Output capacity	5.0 A, 5 V DC (including supply to CPU Unit)	2.8 A, 5 V DC (including supply to CPU Unit)	5.0 A, 5 V DC (including supply to CPU Unit)
	0.8 A, 24 V DC Total: 25 W max.	0.4 A, 24 V DC Total: 14 W max.	0.8 A, 24 V DC Total: 25 W max.
Output terminal (service supply)	Not provided		
RUN output (See note 2.)	Contact configuration: SPST-NO Switch capacity: 250 V AC, 2 A (resistive load) 120 V AC, 0.5 A (inductive load), 24 V DC, 2A (resistive load) 24 V DC, 2 A (inductive load)	Not provided.	
Insulation resistance	20 MΩ min. (at 500 V DC) between AC external and GR terminals (See note 1.)		20 MΩ min. (at 500 V DC) between DC external and GR terminals (See note 1.)
Dielectric strength	2,300 V AC 50/60 Hz for 1 min between AC external and GR terminals (See note 1.) Leakage current: 10 mA max.		
	1,000 V AC 50/60 Hz for 1 min between AC external and GR terminals (See note 1.) Leakage current: 10 mA max.		
Noise immunity	2 kV on power supply line (conforming to IEC61000-4-4)		
Vibration resistance	10 to 57 Hz, 0.075-mm amplitude, 57 to 150 Hz, acceleration: 9.8 m/s^2 in X, Y, and Z directions for 80 minutes (Time coefficient: 8 minutes × coefficient factor 10 = total time 80 min.) (according to JIS C0040)		
Shock resistance	147 m/s^2 3 times each in X, Y, and Z directions (Relay Output Unit: 100 m/s^2) (according to JIS C0041)		
Ambient operating temperature	0 to 55°C		
Ambient operating humidity	10% to 90% (with no condensation)		
Atmosphere	Must be free from corrosive gases.		
Ambient storage temperature	–20 to 70°C (excluding battery)		
Grounding	Less than 100 Ω		
Enclosure	Mounted in a panel.		
Weight	All models are each 5 kg max.		
CPU Rack dimensions	156.7 to 466.7 × 90 × 65 mm (W x H x D) (not including cables) The total width is given by the following: W = 156.7 + n × 20 + m × 31, where n is the number of 32-point I/O Units or I/O Control Units and m is the number of other Units.		
Safety measures	Conforms to cULus and EC Directives.		

Note

1. Disconnect the Power Supply Unit's LG terminal from the GR terminal when testing insulation and dielectric strength. Testing the insulation and dielectric strength with the LG terminal and the GR terminals connected will damage internal circuits in the CPU Unit.
2. Supported only when mounted to CPU Rack.
3. The inrush current is given for a cold start at room temperature. The inrush control circuit uses a thermistor element with a low-temperature current control characteristic. If the ambient temperature is high or the PC is hot-started, the thermistor will not be sufficiently cool, and the inrush currents given in the table may be exceeded by up to twice the given values. When selecting fuses or breakers for external circuits, allow sufficient margin in shut-off performance.

2-2 CPU Unit Components and Functions

2-2-1 CPU Unit Components



Indicators

The following table describes the LED indicators on the front panel of the CPU Unit.

Indicator	Meaning
RUN (green)	Lights when the PC is operating normally in MONITOR or RUN mode.
ERR/ALM (red)	Flashes if a non-fatal error occurs that does not stop the CPU Unit. If a non-fatal error occurs, the CPU Unit will continue operating. Lights if a fatal error occurs that stops the CPU Unit or if a hardware error occurs. If a fatal or hardware error occurs, the CPU Unit will stop operating, and the outputs from all Output Units will turn OFF.
INH (orange)	Lights when the Output OFF Bit (A50015) turns ON. If the Output OFF Bit is turned ON, the outputs from all Output Units will turn OFF.
PRPHL (orange)	Flashes when the CPU Unit is communicating via the peripheral port.
BKUP (orange; CJ1-H CPU Units only)	Lights when data is being backed up from RAM to the flash memory. Do not turn OFF the CPU Unit when this indicator is lit.
COMM (orange)	Flashes when the CPU Unit is communicating via the RS-232C port.
MCPWR (green)	Lit while power is supplied to the Memory Card.
BUSY	Lit while the Memory Card is being accessed.

DIP Switch

The CJ-series CPU Unit has an 8-pin DIP switch that is used to set basic operational parameters for the CPU Unit. The DIP switch is located under the cover of the battery compartment. The DIP switch pin settings are described in the following table.

Pin	Setting	Function
1	ON	Writing disabled for user program memory.
	OFF	Writing enabled for user program memory.
2	ON	User program automatically transferred when power is turned ON.
	OFF	User program not automatically transferred when power is turned ON.
3	ON	Not used.
4	ON	Use peripheral port parameters set in the PC Setup.
	OFF	Auto-detect Programming Console or CX-Programmer parameters at the peripheral port.
5	ON	Auto-detect CX-Programmer parameters at the RS-232C port.
	OFF	Use RS-232C port parameters set in the PC Setup.
6	ON	User-defined pin. Turns OFF the User DIP Switch Pin Flag (A39512).
	OFF	User-defined pin. Turns ON the User DIP Switch Pin Flag (A39512).
7	ON	Easy backup: Read/write to Memory Card.
	OFF	Easy backup: Verify contents of Memory Card.
8	OFF	Always OFF.

2-2-2 CPU Unit Capabilities

CJ1 CPU Units

Model	I/O bits	Program capacity	Data memory capacity (See Note.)	Ladder instruction processing speed	Internal communications ports	Optional products
CJ1G-CPU45	1,280 bits (Up to 3 Expansion Racks)	60 Ksteps	128 Kwords	0.08 μs	Peripheral port and RS-232C port (one each)	Memory Cards
CJ1G-CPU44		30 Ksteps	64 Kwords			

Note The available data memory capacity is the sum of the Data Memory (DM) and the Extended Data Memory (EM) Areas.

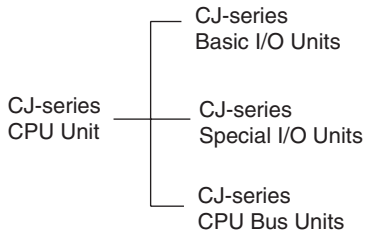
CJ1-H CPU Units

Model	I/O bits	Program capacity	Data memory capacity (See note.)	Ladder instruction processing speed	Internal communications ports	Optional products
CJ1H-CPU66H	2,560 bits (Up to 3 Expansion Racks)	120 Ksteps	256 Kwords	0.02 μs	Peripheral port and RS-232C port	Memory Cards
CJ1H-CPU65H		60 Ksteps	128 Kwords			
CJ1G-CPU45H	1280 bits (Up to 3 Expansion Racks)	60 Ksteps	128 Kwords	0.04 μs		
CJ1G-CPU44H		30 Ksteps	64 Kwords			
CJ1G-CPU43H	960 bits (Up to 2 Expansion Racks)	20 Ksteps	64 Kwords			
CJ1G-CPU42H		1 0Ksteps	64 Kwords			

Note The available data memory capacity is the sum of the Data Memory (DM) and the Extended Data Memory (EM) Areas.

2-2-3 Units Classifications

The CJ-series CPU Units can exchange data with CJ-series Basic I/O Units, CJ-series Special I/O Units, and CJ-series CPU Bus Units, as shown in the following diagram.



2-2-4 Data Communications

CPU Unit Data Communications

Unit	Data exchange during cyclic servicing (allocations)		Event service data communications (IORD/IOWR instruction)	I/O refreshing using IORF instruction
CJ-series Basic I/O Units	According to I/O allocations (Words are allocated in order according to the position the Unit is mounted.)	I/O refreshing	Not provided.	Yes
CJ-series Special I/O Units	Unit No. allocations	Special I/O Unit Area (CIO): 10 words/Unit Special I/O Unit Area (DM): 100 words/Unit	Yes (Not available for some Units.)	Yes (Not available for some Units.)
CJ-series CPU Bus Units		CJ-series CPU Bus Unit Area (CIO): 25 words/ Unit CJ-series CPU Bus Unit Area (DM): 100 words/Unit	Not provided.	No

CPU Unit Connections

Unit	Maximum number of Units on CPU Racks and Expansion Racks	Racks to which Unit can be mounted	
		CJ-series CPU Rack	CJ-series Expansion Racks
CJ-series Basic I/O Units	40 (See Note 1.)	Yes	Yes
CJ-series Special I/O Units	40 (See Note 2.)	Yes	Yes
CJ-series CPU Bus Units	16	Yes	Yes (See Note 3.)

Note
1. The maximum number of Units on CPU Rack and Expansion Racks is 40. There are other restrictions for the number of I/O points.
2. The maximum number of Units that can be connected is 40.
3. Some CPU Bus Units cannot be mounted to an Expansion Rack.

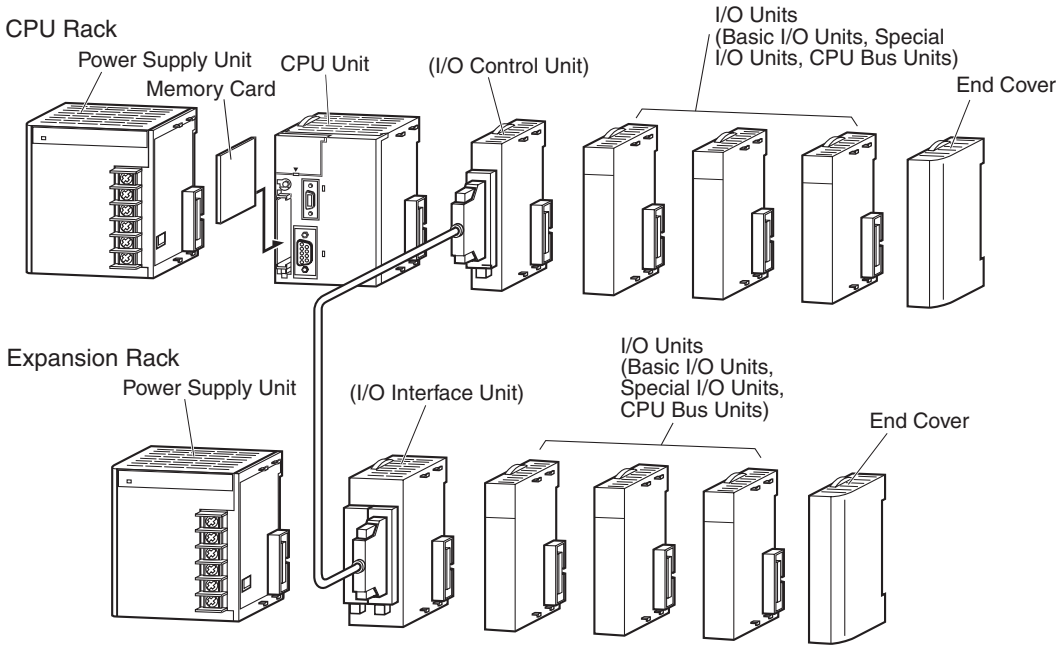
2-3 Basic System Configuration

CJ-series CPU Rack

A CJ-series CPU Rack can consist of a CPU Unit, a Power Supply Unit, Basic I/O Units, Special I/O Units, CPU Bus Units, and an End Cover. A Memory Card is optional. An I/O Control Unit is required to connect an Expansion Rack.

CJ-series Expansion Racks

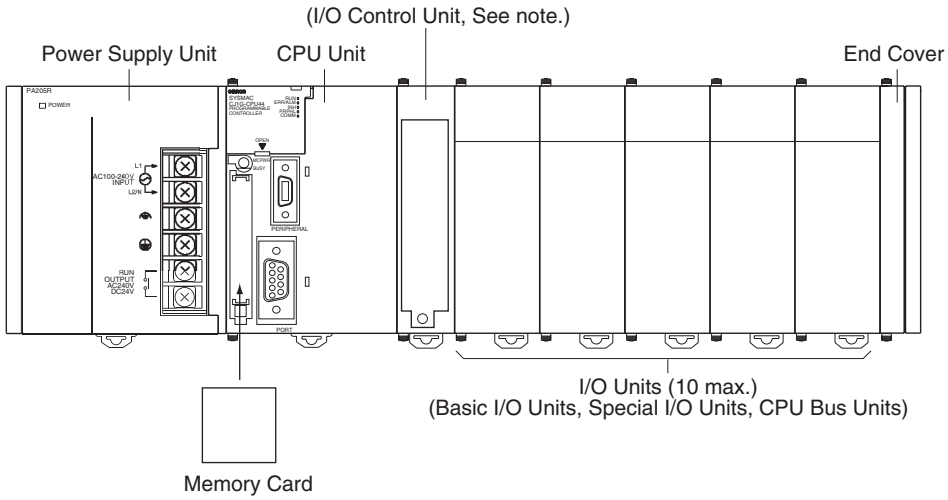
A CJ-series Expansion Rack can be connected to the CPU Rack or other CJ-series Expansion Racks. An Expansion Rack can consist of an I/O Interface Unit, a Power Supply Unit, Basic I/O Units, Special I/O Units, and CPU Bus Units, and an End Cover.



Note Although the CJ-series PCs do not require Backplanes, the term “slot” is still used to refer to the relative position of a Unit in the Racks. The slot number immediately to the left of the CPU Unit is slot 1, and slot numbers increase toward the right side of the Rack.

2-3-1 CJ-series CPU Rack

A CJ-series CPU Rack consists of a CPU Unit, a Power Supply Unit, various I/O Units, and an End Cover. Up to 10 I/O Units can be connected.



Note The I/O Control Unit is required only to connect an Expansion Rack. It must be connected next to the CPU Unit.

Name	Configuration	Remarks
CJ-series CPU Rack	CJ-series CPU Unit	One of each Unit required for every CPU Rack. Refer to the following table for details on applicable models.
	CJ-series Power Supply Unit	
	CJ-series Basic I/O Units	A total of up to 10 Units can be connected. (An error will occur if 11 or more Units are connected.)
	CJ-series Special I/O Units	
	CJ-series CPU Bus Units	
	End Cover (CJ1W-TER01)	Must be connected to the right end of the CPU Rack. One End Cover is provided with the CPU Unit. A fatal error will occur if the End Cover is not connected.
	Memory Card	Install as required. Refer to the following table for details on applicable models.
	I/O Control Unit (CJ1W-IC101)	Required to connect an Expansion Rack. Must be connected next to the CPU Unit.

Units

Name	Model	Specifications
CJ1-H CPU Units	CJ1H-CPU66H	I/O bits: 2,560, Program capacity: 120 Ksteps Data Memory: 256 Kwords (DM: 32 Kwords, EM: 32 Kwords × 7 banks)
	CJ1H-CPU65H	I/O bits: 2,560, Program capacity: 60 Ksteps Data Memory: 128 Kwords (DM: 32 Kwords, EM: 32 Kwords × 3 banks)
	CJ1G-CPU45H	I/O bits: 1,280, Program capacity: 60 Ksteps Data Memory: 128 Kwords (DM: 32 Kwords, EM: 32 Kwords × 3 banks)
	CJ1G-CPU44H	I/O bits: 1,280, Program capacity: 30 Ksteps Data Memory: 64 K words (DM: 32 Kwords, EM: 32 Kwords × 1 banks)
	CJ1G-CPU43H	I/O bits: 960, Program capacity: 20 Ksteps Data Memory: 32 Kwords (DM: 32 Kwords, EM: 32 Kwords × 1 banks)
	CJ1G-CPU42H	I/O bits: 960, Program capacity: 10 Ksteps Data Memory: 32 Kwords (DM: 32 Kwords, EM: 32 Kwords × 1 banks)
CJ1 CPU Units	CJ1G-CPU45	I/O bits: 1,280, Program capacity: 60 Ksteps Data Memory: 128 Kwords (DM: 32 Kwords, EM: 32 Kwords × 3 banks)
	CJ1G-CPU44	I/O bits: 1,280, Program capacity: 30 Ksteps Data Memory: 64 Kwords (DM: 32 Kwords, EM: 32 Kwords × 1 banks)
CJ-series Power Supply Units	CJ1W-PA205R	100 to 240 V AC (with RUN output), Output capacity: 5 A at 5 V DC
	CJ1W-PA202	100 to 240 V AC, Output capacity: 2.8A at 5 V DC
	CJ1W-PD025	24 V DC, Output capacity: 5 A at 5 V DC
Memory Cards	HMC-EF861	Flash memory, 8 MB
	HMC-EF171	Flash memory, 15 MB
	HMC-EF371	Flash memory, 30 MB
	HMC-EF571	Flash memory, 48 MB
	HMC-AP001	Memory Card Adapter
I/O Control Unit	CJ1W-IC101	Required to connect an Expansion Rack. Must be connected next to the CPU Unit. Connect to the I/O Interface Unit (CJ1W-II101) on the first Expansion Rack with a CS/CJ-series I/O Connecting Cable.

Name	Model	Specifications
End Cover	CJ1W-TER01	Must be connected to the right end of the CPU Rack. One End Cover is provided with the CPU Unit and with an I/O Interface Unit. A fatal error will occur if the End Cover is not connected.
DIN Track	PFP-50N	Track length: 50 cm, height: 7.3 mm
	PFP-100N	Track length: 1 m, height: 7.3 mm
	PFP-100N2	Track length: 1 m, height: 16 mm
	PFP-M	Stopper to prevent Units from moving on the track. Two each are provided with the CPU Unit and with an I/O Interface Unit.
Programming Consoles	CQM1H-PRO01-E	An English Keyboard Sheet (CS1W-KS001-E) is required.
	CQM1-PRO01-E	
	C200H-PRO27-E	
Programming Console Keyboard Sheet	CS1W-KS001-E	For CQM1H-PRO01-E, CQM1-PRO01-E, or C200H-PRO27-E.
Programming Console Connecting Cables	CS1W-CN114	Connects the CQM1-PRO01-E Programming Console. (Length: 0.05 m)
	CS1W-CN224	Connects the CQM1-PRO27-E Programming Console. (Length: 2.0 m)
	CS1W-CN624	Connects the CQM1-PRO27-E Programming Console. (Length: 6.0 m)
Programming Device Connecting Cables (for peripheral port)	CS1W-CN118	Connects DOS computers D-Sub 9-pin receptacle (For converting between RS-232C cable and peripherals) (Length: 0.1 m)
	CS1W-CN226	Connects DOS computers D-Sub 9-pin (Length: 2.0 m)
	CS1W-CN626	Connects DOS computers D-Sub 9-pin (Length: 6.0 m)
Programming Device Connecting Cables (for RS-232C port)	XW2Z-200S-CV	Connects DOS computers D-Sub 9-pin (Length: 2.0 m), Static-resistant connector used.
	XW2Z-500S-CV	Connects DOS computers D-Sub 9-pin (Length: 5.0 m), Static-resistant connector used.
	XW2Z-200S-V	Connects DOS computers D-Sub 9-pin (Length: 2.0 m) (see note)
	XW2Z-500S-V	Connects DOS computers D-Sub 9-pin (Length: 5.0 m) (see note)
Battery Set	CPM2A-BAT01	Also used for CPM2A and CQM1H. (Cannot be used with CS-series CPU Unit.)

Note A peripheral bus connection is not possible when connecting the CX-Programmer via an RS-232C Connecting Cable. Use the Host Link (SYSMAC WAY) connection.

Connecting Programming Devices

Programming Console

When using a Programming Console, connect the Programming Console to the peripheral port of the CPU Unit and set pin 4 of the DIP switch on the front panel of the Unit to OFF (automatically uses default communications parameters for the peripheral port).

CQM1H-PRO01-E/CQM1-PRO01-E

The Programming Console can be connected only to the peripheral port.

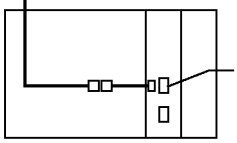
CS1W-KS001-E
English Keyboard
Sheet required.

CQM1H-PRO01-E,
CQM1-PRO01-E
Programming
Console

The following cable is included with the CQM1-PRO01-E Programming Console

Programming Console	Cable	Length
CQM1-PRO01-E	CS1W-CN114	0.05 m
CQM1H-PRO01-E	Not required.	---

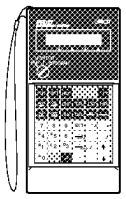
Note Set pin 4 of the DIP switch on the front panel of the CPU Unit to OFF.



Peripheral port

C200H-PRO27-E

The Programming Console can be connected only to the peripheral port.

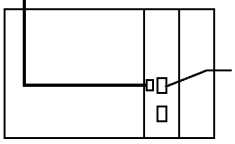


CS1W-KS001-E
English Keyboard
Sheet required.

C200H-PRO27-E
Programming Console

Programming Console	Cable	Length
CQM1-PRO27-E	CS1W-CN224	2.0 m
	CS1W-CN624	6.0 m

Note Set pin 4 of the DIP switch on the front panel of the CPU Unit to OFF.

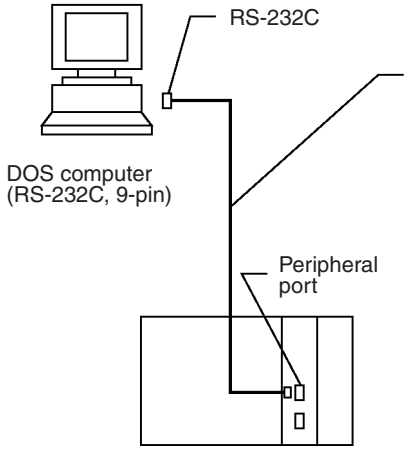


Peripheral port

Note When an OMRON Programmable Terminal (PT) is connected to the RS-232C port and Programming Console functions are being used, do not connect the Programming Console at the same time.

Connecting Personal Computers Running Support Software

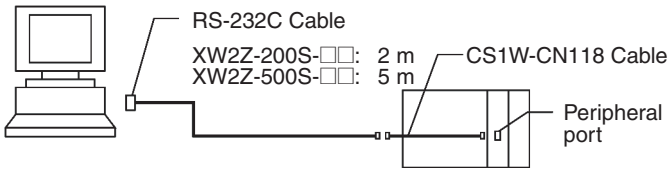
Connecting to Peripheral Port



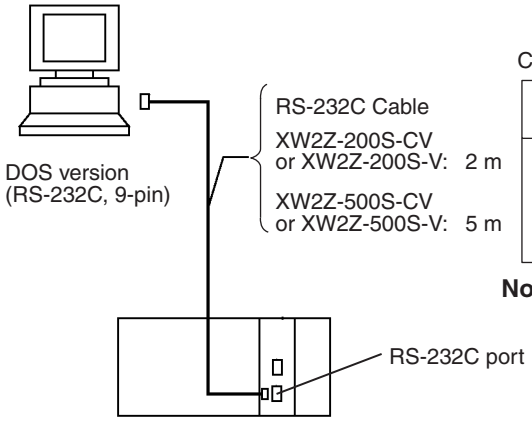
Connecting Cables for Peripheral Port

Computer	Cable	Length	Computer connector
DOS	CS1W-CN118	0.1 m	D-Sub, 9-pin
	CS1W-CN226	2.0 m	
	CS1W-CN626	6.0 m	

Note The CS1W-CN118 Cable is used with an RS-232C cable to connect to the peripheral port on the CPU Unit as shown below. The CS1W-CN118 Cable can not be used with an RS-232C cable whose model number ends in -V for a peripheral bus connection and must be used for a Host Link (SYSMAC WAY) connection.



Connecting to RS-232C Port



Connecting Cables for RS-232C Port

Computer	Cable	Length	Computer connector
DOS	XW2Z-200S-CV or XW2Z-200S-V	2.0 m	D-Sub, 9-pin
	XW2Z-500S-CV or XW2Z-500S-V	5.0 m	

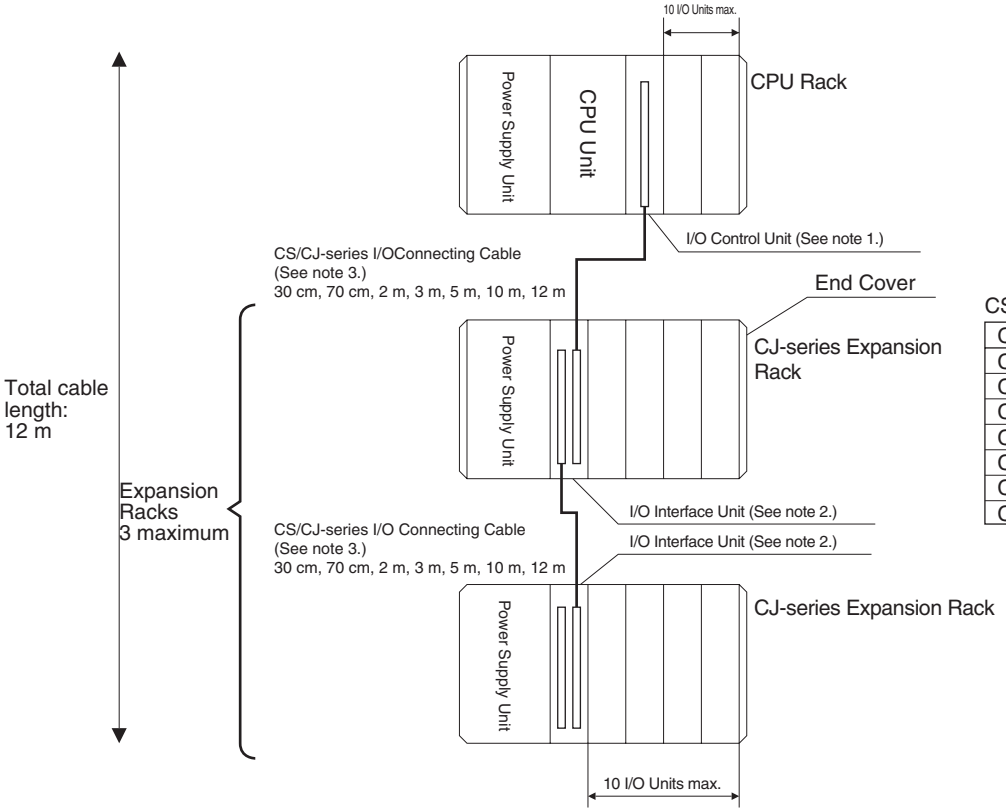
Note The XW2Z-200S-CV and XW2Z-500S-CV use static-resistant connectors and can be connected to the peripheral bus or the Host Link. The XW2Z-200S-V and XW2Z-500S-V, however, can only be connected to the Host Link, not the peripheral bus.

Programming Software

OS	Name	
Windows	CX-Programmer CJ1 CPU Units: Version 2.04 or later CJ1-H CPU Units: Version 2.1 or later	CD-ROM

2-3-2 CJ-series Expansion Racks

To expand the number of Units in the system, CJ-series Expansion Racks can be connected to CPU Racks. Up to 10 I/O Units can be mounted to each Expansion Rack and a total of 3 Expansion Racks can be connected. The maximum number of I/O Units that can be connected in one PC is thus 40.



CS/CJ I/O Connecting Cables

Cable	Length
CS1W-CN313	0.3 m
CS1W-CN713	0.7 m
CS1W-CN223	2 m
CS1W-CN323	3 m
CS1W-CN523	5 m
CS1W-CN133	10 m
CS1W-CN133B2	12 m

Note

1. Connect the I/O Control Unit directly to the CPU Unit. Proper operation may not be possible if it is connected any other location.
2. Connect the I/O Interface Unit directly to the Power Supply Unit. Proper operation may not be possible if it is connected any other location.
3. The total length of CS/CJ-series I/O Connecting cable between all Racks must be 12 m or less.

Maximum Expansion Racks

Expansion pattern	Rack	Maximum No. of Racks	Remarks
CJ-series CPU Rack with CJ-series Expansion Racks	CJ-series Expansion Racks	3 Racks	The total cable length must be 12 m or less.

Rack Configurations

Rack	Configuration	Remarks
CJ-series Expansion Racks	CJ-series Power Supply Unit	One of each Unit required for every CPU Rack.
	I/O Interface Unit (one End Cover included.)	Refer to the following table for details on applicable models.
	CJ-series Basic I/O Units	A total of up to 10 Units can be connected. (An error will occur if 11 or more Units are connected.)
	CJ-series Special I/O Units	
	CJ-series CPU Bus Units	
	End Cover (CJ1W-TER01)	Must be connected to the right end of the Expansion Rack. One End Cover is provided with the I/O Interface Unit. A fatal error will occur if the End Cover is not connected.
	CS/CJ-series I/O Connecting Cable	Required to connect the I/O Interface Unit to the I/O Control Unit or previous I/O Interface Unit. Proper operation may not be possible if the total length of I/O Connecting Cable between all Racks is more than 12 m.

Configuration Device List

Name	Model	Specifications	Cable length
CJ-series Power Supply Unit	CJ1W-PA205R	100 to 240 V AC (with RUN output), Output capacity: 5 A at 5 V DC	---
	CJ1W-PA202	100 to 240 V AC, Output capacity: 2.8A at 5 V DC	
	CJ1W-PD025	24 V DC, Output capacity: 5 A at 5 V DC	
I/O Interface Unit	CJ1W-II101	One Interface Unit is required for each CJ-series Expansion Rack. One End Cover is provided with each Unit. (Connect to an I/O Control Unit mounted on a CJ-series CPU Rack or an Interface Unit mounted on an Expansion Rack using an I/O connecting cable.)	
End Cover	CJ1W-TER01	Must be connected to the right end of the CPU Rack. One End Cover is provided with the CPU Unit and with an I/O Interface Unit. A fatal error will occur if the End Cover is not connected.	
CS/CJ-series I/O Connecting Cables	CS1W-CN313	Connects Expansion Racks to CPU Racks or other Expansion Racks.	0.3 m
	CS1W-CN713		0.7 m
	CS1W-CN223		2 m
	CS1W-CN323		3 m
	CS1W-CN523		5 m
	CS1W-CN133		10 m
	CS1W-CN133B2		12 m

2-3-3 Connectable Units

The following table shows the Units that can be connected to CPU Racks and Expansion Racks. Refer to *2-4 I/O Units* for details on the limitations on each particular Unit.

Unit	CJ-series Basic I/O Units	CJ-series Special I/O Units	CJ-series CPU Bus Units
CJ-series CPU Rack	Yes	Yes	Yes
CJ-series Expansion Racks	Yes	Yes	Yes

2-3-4 Maximum Number of Units

The maximum number of I/O Units that can be connected to the CPU Rack and Expansion Racks is 40, i.e., 10 each for the CPU Rack and up to 3 Expansion Racks. The total number of each type of Unit is not limited according to connection locations

Note A fatal error will occur and the CPU Unit will not operate if more than 10 I/O Units are connected to the CPU Rack or any Expansion Rack.

2-4 I/O Units

2-4-1 CJ-series Basic I/O Units

Basic Input Units

Name	Specifications	Model	Number of bits allocated	Mountable Racks	
				CJ-series CPU Rack	CJ-series Expansion Racks
DC Input Units	Terminal block 24 V DC, 16 inputs	CJ1W-ID211	16	Yes	Yes
	Fujitsu-compatible connector 24 V DC, 32 inputs (See note 1.)	CJ1W-ID231	32	Yes	Yes
	MIL connector 24 V DC, 32 inputs (See note 1.)	CJ1W-ID232	32	Yes	Yes
	Fujitsu-compatible connector 24 V DC, 64 inputs (See note 1.)	CJ1W-ID261	64	Yes	Yes
	MIL connector 24 V DC, 64 inputs (See note 1.)	CJ1W-ID262	64	Yes	Yes
AC Input Units	200 to 240 V DC, 8 inputs	CJ1W-IA201	16 (See note 2.)	Yes	Yes
	100 to 120 V DC, 16 inputs	CJ1W-IA111	16	Yes	Yes
Interrupt Input Units	24 V DC, 16 inputs	CJ1W-INT01	16	Yes (See note 3.)	No

Note

1. The cable-side connector is not provided with Units equipped with cables. Purchase the cable separately (see page 156), or use an OMRON Connector-Terminal Block Conversion Unit or I/O Terminal (see page 159).
2. Although 16 output bits are allocated, only 8 of these can be used for external outputs. This Unit is also treated as a 16-point Output Unit in the I/O tables.
3. The Unit must be connected in one of the 5 positions next to the CPU Unit on the CPU Rack. An I/O setting error will occur if the Unit is connected to other positions on the CPU Rack or to any position on an Expansion Rack.

Basic Output Units

Name	Specifications	Model	Number of bits allocated	Mountable Racks	
				CJ-series CPU Rack	CJ-series Expansion Racks
Relay Output Units	Terminal block, 250 V AC/24 V DC, 2 A; 8 points, independent contacts	CJ1W-OC201	16 (See note 2.)	Yes	Yes
	Terminal block, 250 V AC, 0.6 A; 8 points	CJ1W-OC211	16	Yes	Yes
Triac Output Unit	Terminal block, 250 V AC, 0.6 A/24 V DC, 2 A; 8 points, independent contacts	CJ1W-OA201	16 (See note 2.)	Yes	Yes

Name		Specifications	Model	Number of bits allocated	Mountable Racks	
					CJ-series CPU Rack	CJ-series Expansion Racks
Transistor Output Units	Sinking outputs	Terminal block, 12 to 24 V DC, 2 A, 8 outputs	CJ1W-OD201	16 (See note 2.)	Yes	Yes
		Terminal block, 12 to 24 V DC, 0.5 A, 16 outputs	CJ1W-OD211	16	Yes	Yes
		Fujitsu-compatible connector, 12 to 24 V DC, 0.5 A, 32 outputs (See note 1.)	CJ1W-OD231	32	Yes	Yes
		MIL connector, 12 to 24 V DC, 0.3 A, 32 outputs (See note 1.)	CJ1W-OD233	32	Yes	Yes
		Fujitsu-compatible connector, 12 to 24 V DC, 0.3 A, 64 outputs (See note 1.)	CJ1W-OD261	64	Yes	Yes
		MIL connector, 12 to 24 V DC, 0.3 A, 64 outputs (See note 1.)	CJ1W-OD263	64	Yes	Yes
	Sourcing outputs	Terminal block, 24 V DC, 2 A, 8 outputs, load short-circuit protection	CJ1W-OD202	16 (See note 2.)	Yes	Yes
		Terminal block, 24 V DC, 0.5 A, 16 outputs, load short-circuit protection and disconnected line detection	CJ1W-OD212	16	Yes	Yes
		MIL connector, 24 V DC, 0.5 A, 32 outputs, load short-circuit protection (See note 1.)	CJ1W-OD232	32	Yes	Yes

Note

1. The cable-side connector is not provided with Units equipped with cables. Purchase the cable separately (see page 156), or use an OMRON Connector-Terminal Block Conversion Unit or I/O Terminal (see page 159).
2. Although 16 output bits are allocated, only 8 of these can be used for external outputs. This Unit is also treated as a 16-point Output Unit in the I/O tables.
3. The Unit must be connected in one of the 5 positions next to the CPU Unit on the CPU Rack. An I/O setting error will occur if the Unit is connected to other positions on the CPU Rack or to any position on an Expansion Rack.

2-4-2 CJ-series Special I/O Units

Name	Specifications	Model	Number of words allocated (CIO 2000 to CIO 2959)	Number of words allocated (D20000 to D29599)	Mountable Racks		Unit No.
					CJ-series CPU Rack	CJ-series Expansion Racks	
Analog Input Unit	8 inputs (4 to 20 mA, 1 to 5 V, etc.)	CJ1W-AD081 (-V)	10 words	100 words	Yes	Yes	0 to 95
	4 inputs (4 to 20 mA, 1 to 5 V, etc.)	CJ1W-AD041	10 words	100 words	Yes	Yes	0 to 95
Analog Output Unit	4 outputs (1 to 5 V, 4 to 20 mA, etc.)	CJ1W-DA041	10 words	100 words	Yes	Yes	0 to 95
	2 outputs (1 to 5 V, 4 to 20 mA, etc.)	CJ1W-DA021	10 words	100 words	Yes	Yes	0 to 95
Temperature Control Units	4 control loops, thermocouple inputs, NPN outputs	CJ1W-TC001	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	4 control loops, thermocouple inputs, PNP outputs	CJ1W-TC002	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	2 control loops, thermocouple inputs, NPN outputs, heater burnout detection	CJ1W-TC003	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	2 control loops, thermocouple inputs, NPN outputs, heater burnout detection	CJ1W-TC004	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	4 control loops, temperature-resistance thermometer inputs, NPN outputs	CJ1W-TC101	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	4 control loops, temperature-resistance thermometer inputs, PNP outputs	CJ1W-TC102	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	2 control loops, temperature-resistance thermometer inputs, NPN outputs, heater burnout detection	CJ1W-TC103	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	2 control loops, temperature-resistance thermometer inputs, PNP outputs, heater burnout detection	CJ1W-TC104	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)

Name	Specifications	Model	Number of words allocated (CIO 2000 to CIO 2959)	Number of words allocated (D20000 to D29599)	Mountable Racks		Unit No.
					CJ-series CPU Rack	CJ-series Expansion Racks	
Position Control Units	1 axis, pulse output; open collector output	CJ1W-NC113	10 words	100 words	Yes	Yes	0 to 95
	2 axes, pulse outputs; open collector outputs	CJ1W-NC213	10 words	100 words	Yes	Yes	0 to 95
	4 axes, pulse outputs; open collector outputs	CJ1W-NC413	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
	1 axis, pulse output; line driver output	CJ1W-NC133	10 words	100 words	Yes	Yes	0 to 95
	2 axes, pulse outputs; line driver outputs	CJ1W-NC233	10 words	100 words	Yes	Yes	0 to 95
	4 axes, pulse outputs; line driver outputs	CJ1W-NC433	20 words	200 words	Yes	Yes	0 to 94 (uses words for 2 unit numbers)
High-speed Counter Unit	Two-axis pulse input, counting rate: 500 kcps max., line driver compatible	CJ1W-CT021	40 words	400 words	Yes	Yes	0 to 92 (uses words for 4 unit numbers)
CompoBus/S Master Units	CompoBus/S Remote I/O, 256 bits max.	CJ1W-SRM21	10 words or 20 words	None	Yes	Yes	0 to 95 or 0 to 94

2-4-3 CJ-series CPU Bus Units

Name	Specifications	Model	Number of words allocated (CIO 1500 to CIO 1899)	Mountable Racks		Unit No.
				CJ-series CPU Rack	CJ-series Expansion Racks	
Controller Link Units	Wired	CJ1W-CLK21	25 words	Yes	Yes	0 to F (4 Units max.)
Serial Communications Unit	One RS-232C port and one RS-422A/485 port	CJ1W-SCU41	25 words	Yes	Yes	0 to F
Ethernet Unit	10Base-T, FINS communications, socket service, FTP server, and mail communications	CJ1W-ETN11	25 words	Yes	Yes	0 to F (4 Units max.)
DeviceNet Unit	DeviceNet remote I/O, 2,048 points; Both master and slave functions, Automatic allocation possible without Configurator	CJ1W-DRM21	25 words (See note 1.)	Yes	Yes	0 to F

Note
1. Slave I/O are allocated in DeviceNet Area (CIO 3200 to CIO 3799).
2. Some CJ-series CPU Bus Units are allocated words in the CPU Bus Unit Setting Area. The system must be designed so that the number of words allocated in the CPU Bus Unit Setting Area does not exceed its capacity. Refer to *2-7 CPU Bus Unit Setting Area Capacity* for details.

2-5 Expanded System Configuration

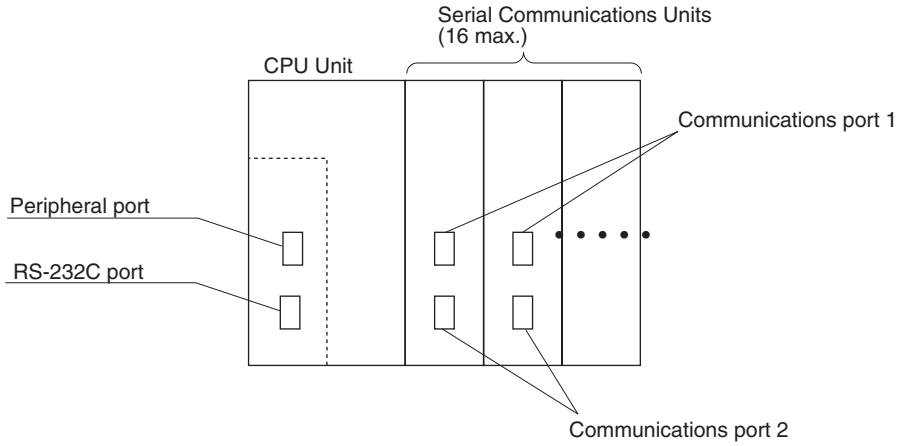
2-5-1 Serial Communications System

The CJ-series system configuration can be expanded by using the following serial communications ports.

- CPU Unit built-in ports × 2 (peripheral port and RS-232C port)
- Serial Communications Unit ports × 2 (RS-232C and RS-422A/485)

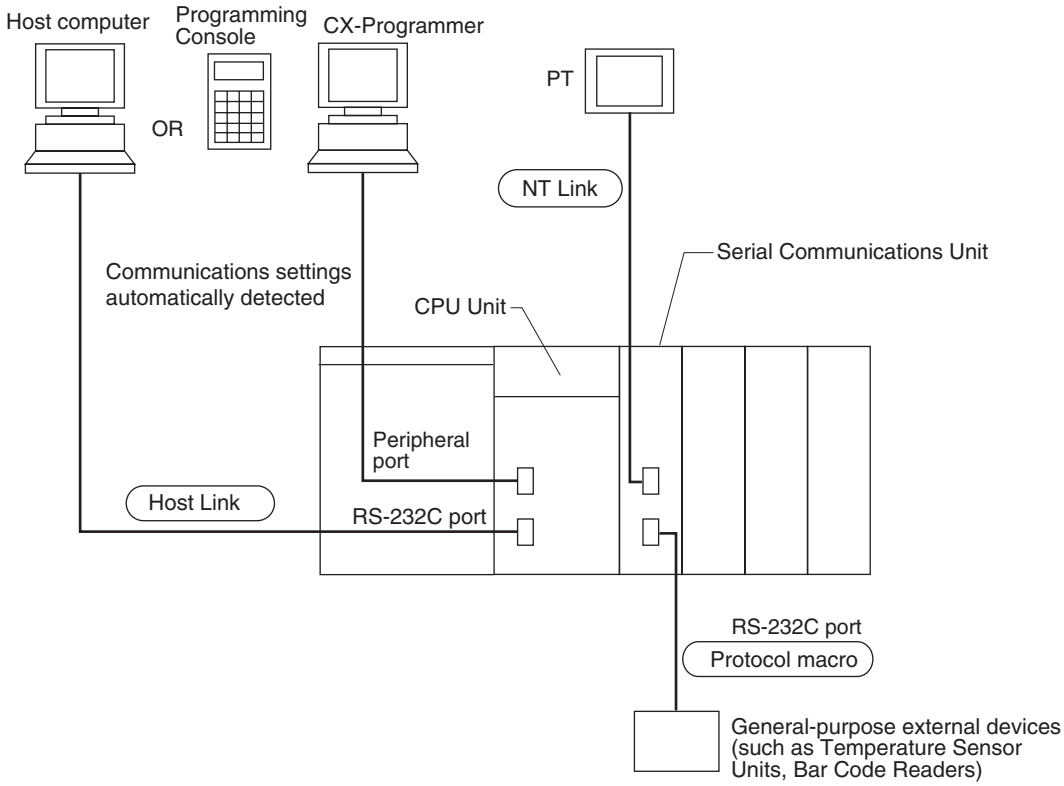
1,2,3...

1. If the CPU Unit built-in ports or Serial Communications Unit ports are used, various protocols can be allocated, such as Host Link and protocol macros.
2. Up to 16 Serial Communications Units can be connected for one CPU Unit. The system configuration can then be expanded by connecting devices with RS-232C or RS-422/485 ports, such as Temperature Sensor Units, Bar Code Readers, ID Systems, personal computers, Board Computers, Racks, and other companies' PCs.



Expanding the system configuration as shown above allows a greater number of serial communications ports, and greater flexible and simpler support for different protocols.

System Configuration Example



Refer to page 62 for a table showing which communications protocols are supported by each Unit.

2-5-2 Systems

The serial communications port mode (protocol) can be switched in the CPU Unit's PC Setup. Depending on the protocol selected, the following systems can be configured.

Protocols

The following protocols support serial communications.

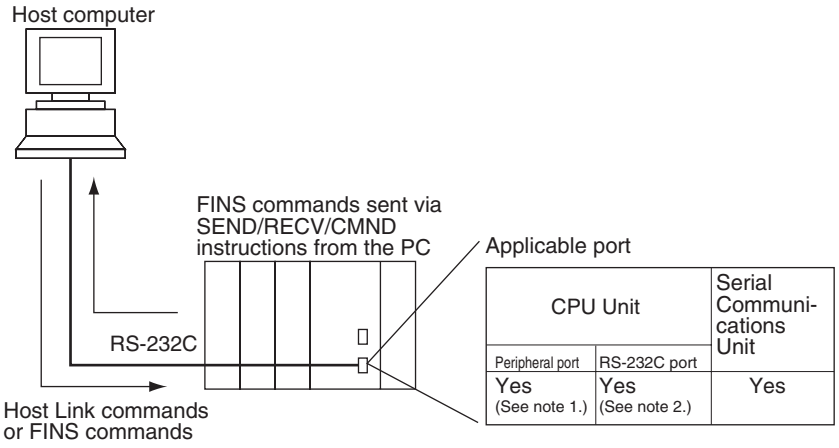
Protocol	Main connection	Use	Applicable commands, communications instructions
Host Link (SYSMAC WAY)	Personal computer OMRON Programmable Terminals	Communications between the Host computer and the PC. Commands can be sent to a computer from the PC.	Host Link commands/ FINS commands. Commands can be sent to a computer from the PC.
No-protocol (customer) communications	General-purpose external devices	No-protocol communications with general-purpose devices.	TXD(236) instruction, RXD(235) instruction
Protocol macro	General-purpose external devices	Sending and receiving messages (communications frames) according to the communications specifications of external devices. (SYSMAC-PST is used to create protocols by setting various parameters.)	PMCR(260) instruction

Protocol	Main connection	Use	Applicable commands, communications instructions
NT Links (1: N)	OMRON Programmable Terminals	High-speed communications with Programmable Terminals via direct access.	None
Peripheral bus (See note.)	Programming Devices CX-Programmer	Communications between Programming Devices and the PC from the computer.	None

Note The peripheral bus mode is used for Programming Devices excluding Programming Console. If Programming Console is to be used, set pin 4 of the DIP switch on the front panel of the Unit to OFF so that the default peripheral port communications parameters are used instead of those specified in the PC Setup.

Host Link System (SYSMAC WAY Mode 1:N)

The Host Link System allows the I/O memory of the PC to be read/written, and the operating mode to be changed from a Host computer (personal computer or Programmable Terminal) by executing Host Link commands or FINS commands that are preceded by a header and followed by a terminator. Alternatively, FINS commands (preceded by a header and followed by a terminator) can be sent to a computer connected via the Host Link System by executing Network Communications Instructions (SEND(090)/RECV(098)/CMND(490)) from the PC.

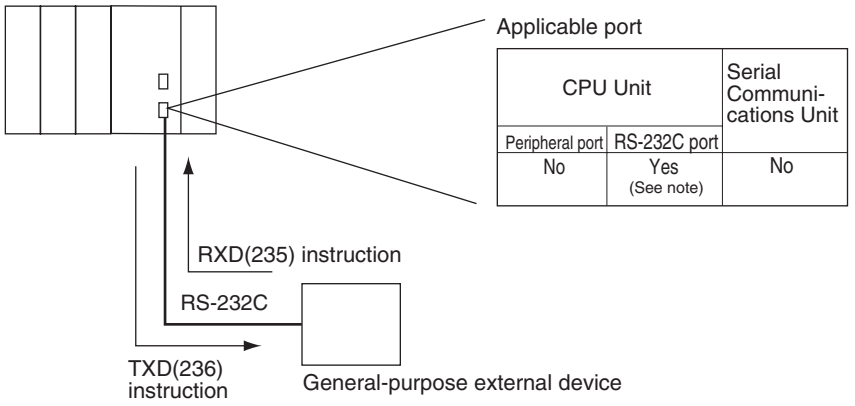


Note

1. Set pin 4 of the DIP switch on the front panel of the CPU Unit to ON, and set the serial communications mode in the PC Setup to Host Link.
2. Set pin 5 of the DIP switch on the front panel of the CPU Unit to OFF, and set the serial communications mode in the PC Setup to Host Link.

No-protocol (Custom) Communications System

No-protocol communications allow simple data transmissions, such as inputting bar code data and outputting printer data using communications port I/O instructions TXD(236) and RXD(235). The start and completion codes can be set and, RS and CS signal control is also possible with no-protocol communications.

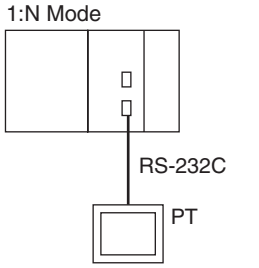


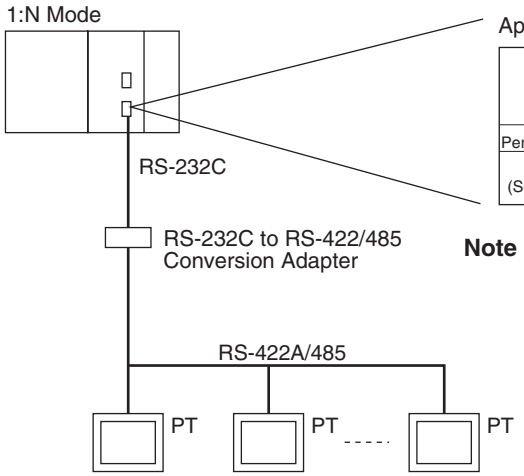
Note Set pin 5 of the DIP switch on the front panel of the CPU Unit to OFF, and set the serial communications mode in the PC Setup to no-protocol communications.

NT Link System (1:N Mode)

If the PC and Programmable Terminal (PT) are connected together using RS-232C ports, the allocations for the PT's status control area, status notify area, objects such as touch switches, indicators, and memory maps can be allocated in the I/O memory of the PC. The NT Link System allows the PT to be controlled by the PC, and the PT can periodically read data from the status control area of the PC, and perform necessary operations if there are any changes in the area. The PT can communicate with the PC by writing data to the status notify area of the PC from the PT. The NT Link system allows the PT status to be controlled and monitored without using PC ladder programs. The ratio of PCs to PTs is 1: n ($n \geq 1$).

Set the PT communications settings for a 1:N NT Link. Either one or up to eight PTs can be connected to each PC.





Applicable port

CPU Unit		Serial Communications Unit
Peripheral port	RS-232C	
Yes (See note 1.)	Yes (See note 2.)	Yes

Note 1. Turn ON pin 4 on the DIP switch on the front of the CPU Unit and set the serial communications mode in the PC Setup for an NT Link.
2. Turn OFF pin 5 on the DIP switch on the front of the CPU Unit and set the serial communications mode in the PC Setup for an NT Link.

Note

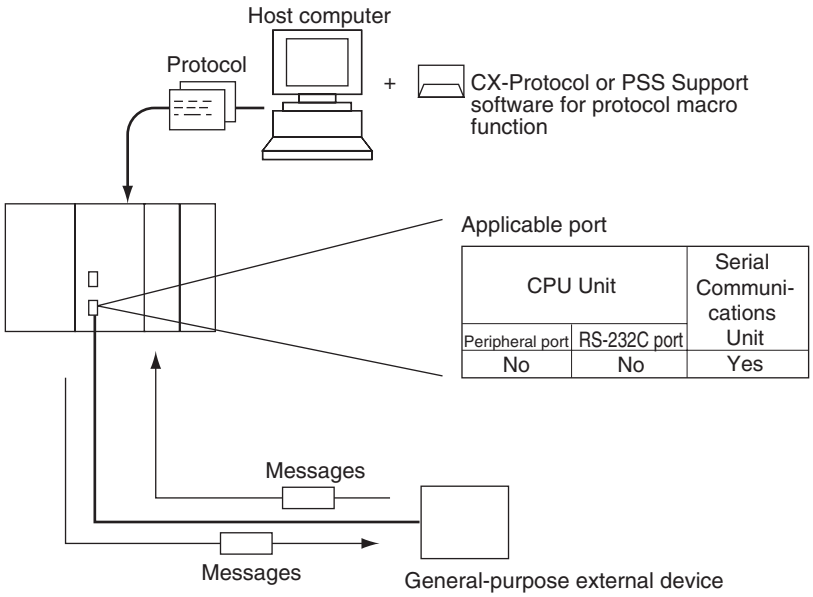
1. The PC can be connected to any PT port that supports 1:N NT Links. It cannot be connected to the RS-232C ports on the NT30 or NT30C, because these ports support only 1:1 NT Links.
2. The NT20S, NT600S, NT30, NT30C, NT620S, NT620C, and NT625C cannot be used if the CPU Unit's cycle time is 800 ms or longer (even if only one of these PTs is connected).
3. The Programming Console functionality of a PT (Expansion Function) can be used only when the PT is connected to the RS-232C or peripheral port on the CPU Unit. It cannot be used when connected to an RS-232C or RS-422A/485 port on a Serial Communications Unit.
4. A PT implementing Programming Console functionality and a PT implementing normal PT functionality cannot be used at the same time.
5. When more than one PT is connected to the same PC, be sure that each PT is assigned a unique unit number. Malfunctions will occur if the same unit number is set on more than one PT.
6. The 1:1 and 1:N NT Link protocols are not compatible with each other, i.e., they are separate serial communications protocols.

Protocol Macros

The CX-Protocol is used to create data transmission procedures (protocols) for general-purpose external devices according to the communications specifications (half-duplex or full-duplex, asynchronous) of the general-purpose external devices. The protocols that have been created are then recorded in a Serial Communications Unit, enabling data to be sent to and received from the external devices by simply executing the PMCR(260) instruction in the CPU Unit. Protocols for data communications with OMRON devices, such as

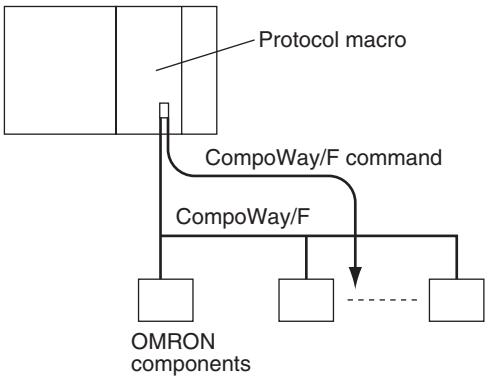
Temperature Controller, Intelligent Signal Processors, Bar Code Readers, and Modems, are supported as standard protocols. (See note.)

Note The standard protocols are provided with the CX-Protocol and Serial Communications Unit.



CompoWay/F (Host Function)

The CJ-series CPU Unit can operate as a host to send CompoWay/F commands to OMRON components connected in the system. CompoWay/F commands are executed by using the CompoWay/F send/receive sequences in the standard protocols of the protocol macro function.



Unit/Protocol Compatibility

Unit	Model	Port	Peripheral bus (See note.)	Host Link	No-protocol (customer) communications	Protocol macro	NT Link (1:N Mode)
CPU Units	CJ1G/H-CPU□□H CJ1G-CPU□□	Peripheral	Yes	Yes	---	---	Yes
		RS-232C	Yes	Yes	Yes	---	Yes
Serial Communications Unit	CJ1W-SCU41	RS-422A/485	---	Yes	---	Yes	Yes
		RS-232C	---	Yes	---	Yes	Yes

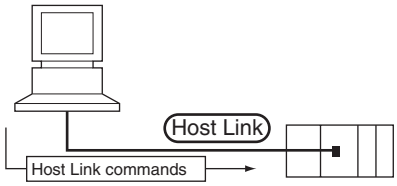
Note The peripheral bus mode is used for Programming Devices excluding Programming Consoles. If Programming Console is to be used, set pin 4 of the

DIP switch on the front panel of the Unit to OFF so that the communications settings are automatically detected instead of using those specified in the PC Setup.

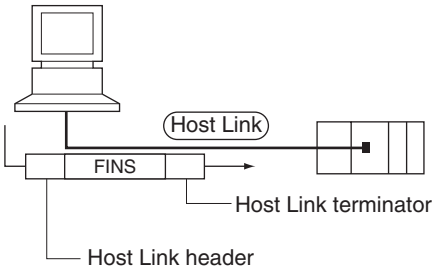
Host Link System

The following system configurations are possible for a Host Link System.

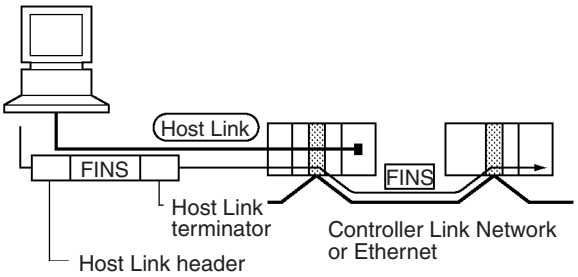
C-mode Commands

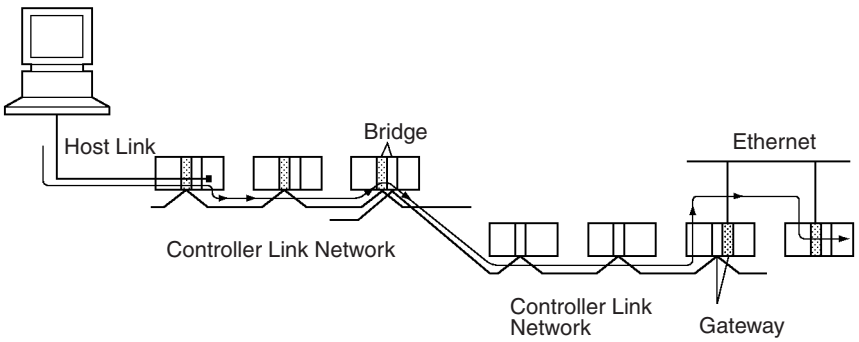


FINS Commands

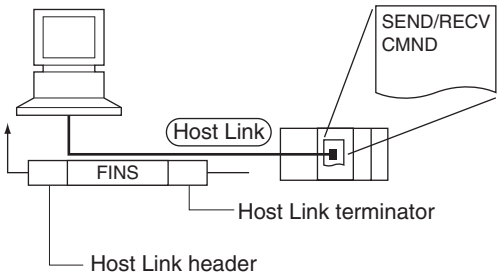


Note In Host Link mode, FINS commands contained between a header and terminator can be sent from the host computer to any PC on the Network. Communications are possible with PCs on the same or different types of interconnected Networks up to two levels away (three levels including the local level but not including the Host Link connection).



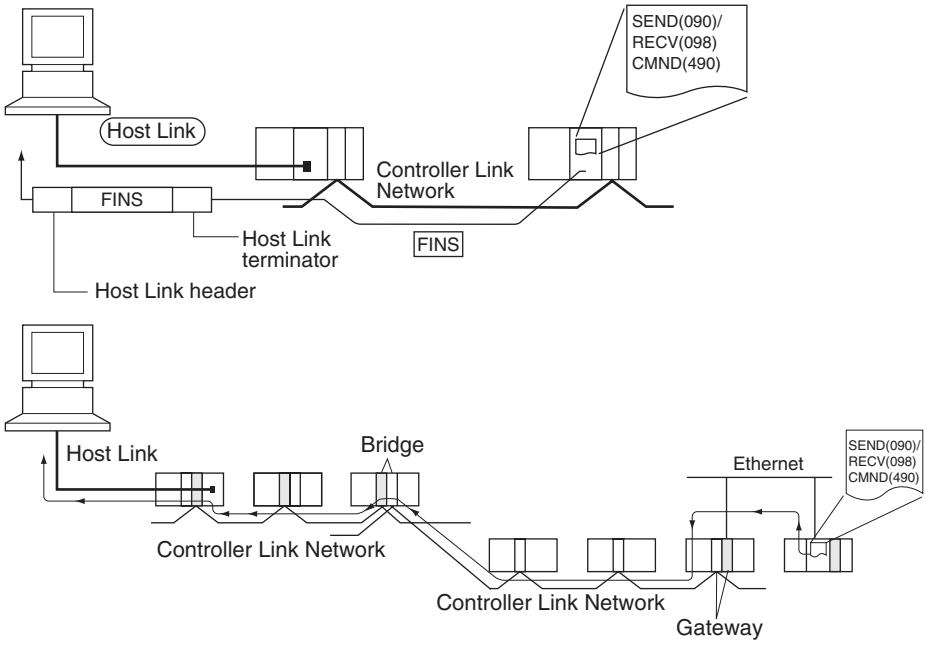


Communications from Host Computer



SEND(090): Sends data to the Host computer.
RECV(098): Receives data from the Host computer.
CMND(490): Executes a specified FINS command.

Note In Host Link mode, FINS commands contained between a header and terminator can be sent from the host computer to any PC on the Network. Communications are possible with PCs on the same or different types of interconnected Networks up to two levels away (three levels including the local level but not including the Host Link connection).

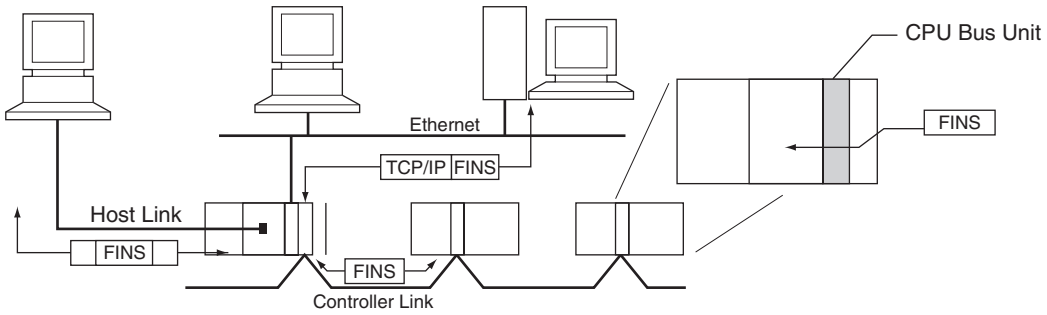


FINS Messages

FINS (Factory Interface Network Service) messages are commands and responses that are used as a message service in an OMRON Network. FINS messages enable the user to control operations such as sending and receiving data and changing operating modes when necessary. The features of FINS messages are as follows:

Flexible Communications

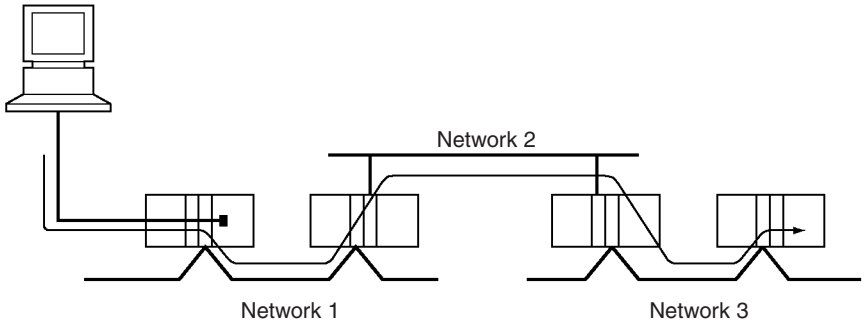
FINS messages are defined in the application layer and do not rely on the physical layer, data link layer, or other lower-level layers. This enables flexible communications on the CPU bus and different types of networks. Basically, communications with Ethernet, Controller Link, or Host Link Networks, and between the CPU Unit and CPU Bus Units is possible via the CPU bus.



Note A TCP/IP header must be attached to the FINS command for an Ethernet Network, and a Host Link header must be attached to the FINS command for a Host Link Network

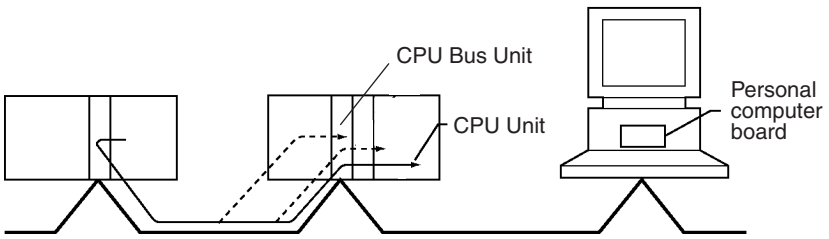
Supports Network Relay

Up to three network levels, including the local network, can be bypassed to access other Racks.



Access to CPU Unit Plus Other Devices on Racks

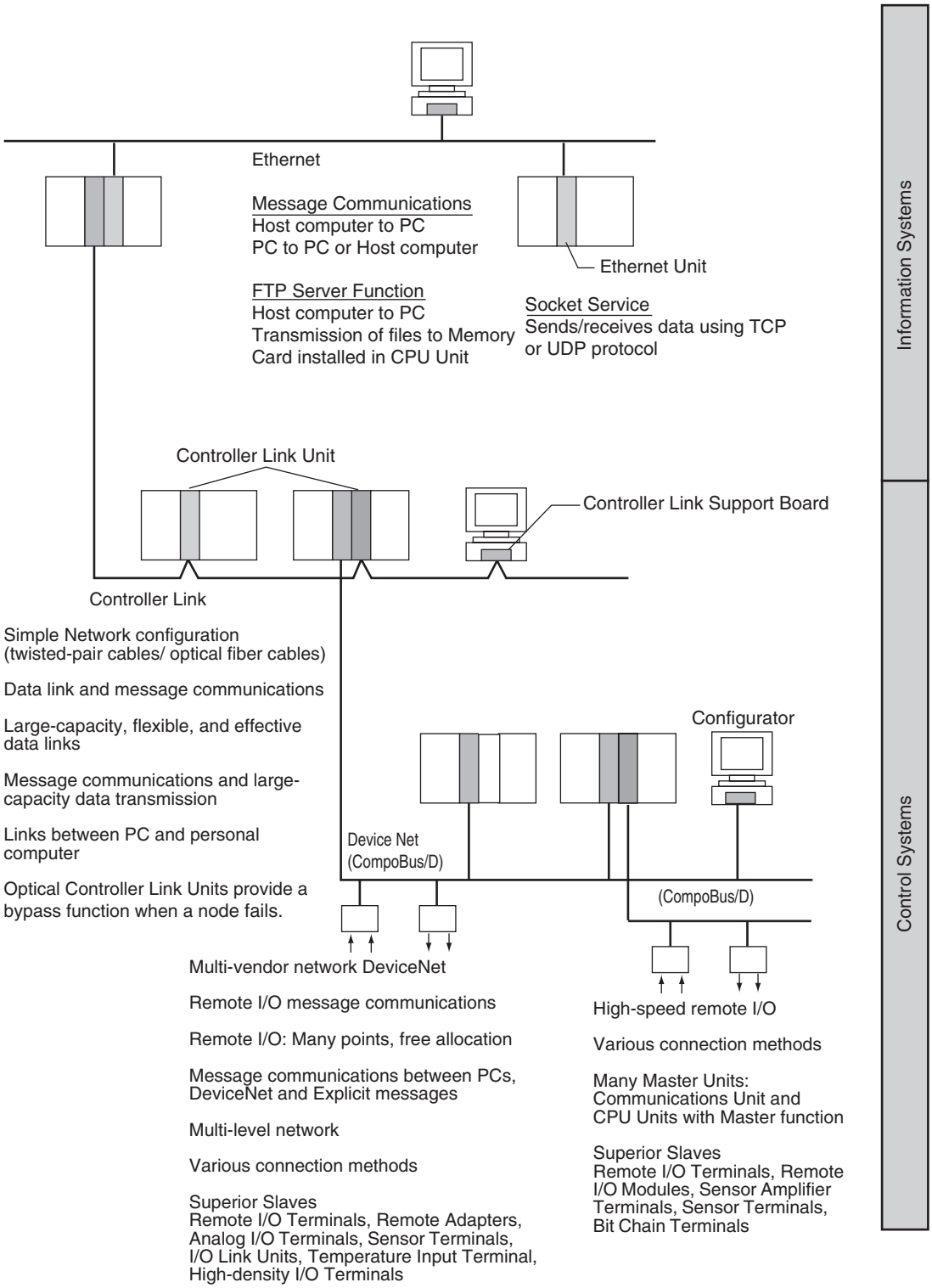
The CPU Unit, CPU Bus Units, personal computers (boards), and other devices can be identified and specified using unit addresses.



2-5-3 Communications Network System

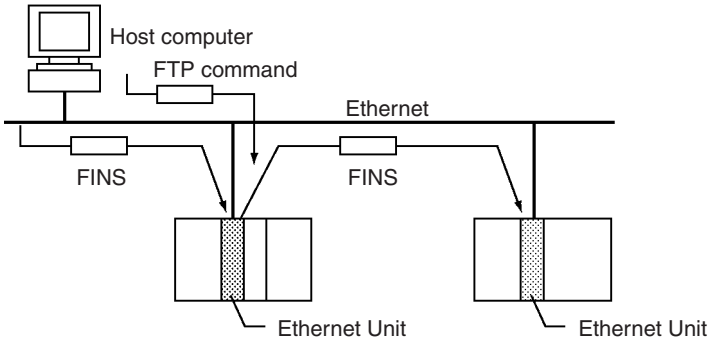
Communications Networks

The following network systems can be configured when using CJ-series Units.



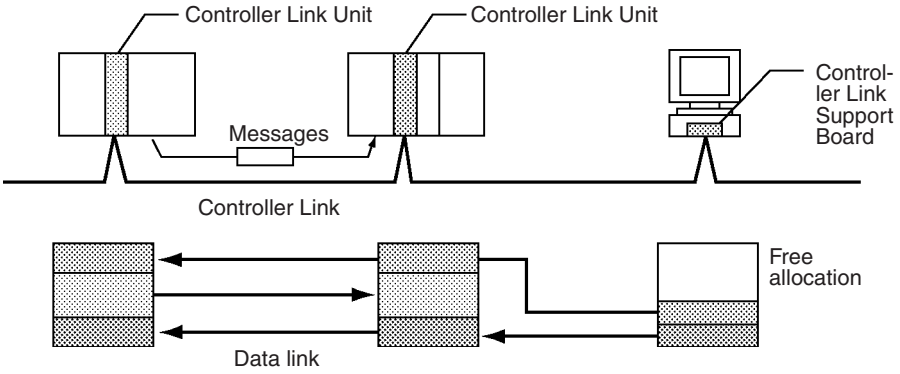
Ethernet

If an Ethernet Unit is connected to the system, FINS messages can be used to communicate between the Host computer connected to the Ethernet and the PC, or between PCs. By executing FTP commands for the PC from the Host computer connected to the Ethernet, the contents of the files on the Memory Card installed in the CPU Unit can be read or written (transferred). Data can be sent and received using UDP and TCP protocols. These functions enable a greater compatibility with information networks.



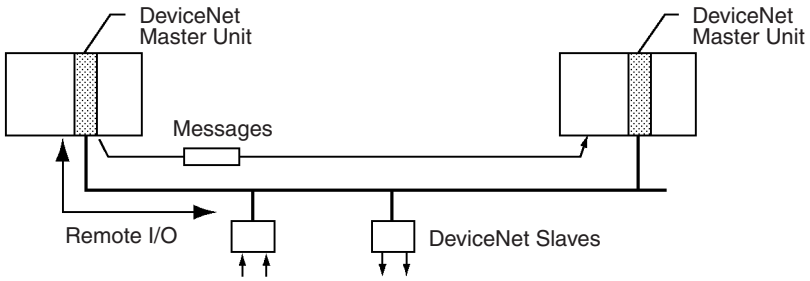
Controller Link

The Controller Link Network is the basic framework of the OMRON PC FA Network. Connecting a Controller Link Unit to the network enables data links between PCs, so that data can be shared without programming, and FINS message communications between PCs, which enable separate control and data transfer when required. The Controller Link Network connections use either twisted-pair cables or optical fiber cables. Data links and message communications are also possible between the PC and personal computer. Data links enable large-capacity and free allocations. FINS message communications also allow large-capacity data transfer.



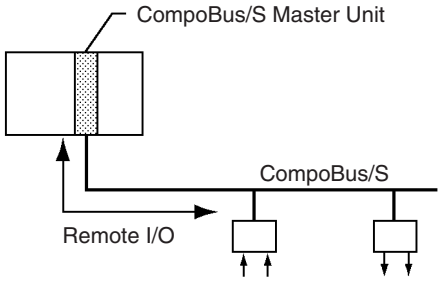
DeviceNet (CompoBus/D)

DeviceNet is a multi-vendor network consisting of multi-bit control and information systems and conforms to the Open Field DeviceNet specification. Connecting a DeviceNet Master Unit to the network enables remote I/O communications between the PC and the Slaves on the network. Remote I/O communications enable large-capacity I/O and user-set allocations. Analog I/O Terminals are used for the Slaves. Message communications are possible between PCs and between the PC and DeviceNet devices manufactured by other companies.



CompoBus/S

CompoBus/S is a high-speed ON/OFF bus for remote I/O communications. Connecting a CompoBus/S Master Unit to the network allows remote I/O communications between the PC and Slaves. High-speed communications are performed with 256 points in a cycle time of 1 ms max.



Communications Network Overview

System	Network	Function	Communications	Communications Device
Information networks	Ethernet	Between Host computer and PC.	FINS message communications	Ethernet Unit
		Between PCs.		
		Between Host computer and Memory Card installed in CPU Unit.	FTP servo	
		Between PC and nodes with socket service, such as UNIX computers.	Socket service	
	Controller Link	Between PC and personal computer directly connected to the Network.	FINS message communications	Controller Link Unit
			Data link (offset, simple settings)	
	RS-232C → Controller Link	Between Host Link computer and PC on the Network.	Host Link commands and gateway.	RS-232C cables and Controller Link Unit
Control networks	Controller Link	Between PCs.	FINS message communications	Controller Link Unit
	DeviceNet (CompoBus/D)		FINS message communications in an open network.	CompoBus/D Master Unit and Configurator
	DeviceNet (CompoBus/D)	PC and Network devices (Slaves).	Large-capacity remote I/O (fixed or free allocation) in an open network	
	CompoBus/S		High-speed remote I/O in a network with OMRON devices only (fixed allocations).	CompoBus/S Master Unit

Communications Specifications

Network	Communications			Max. baud rate	Communications distance	Max. No. of Units	Communications medium	Data link capacity (per network)	Max. remote I/O points	Connectable devices
	Messages	Data link	Remote I/O							
Ethernet	Yes	---	---	10 Mbps	2.5 km	---	Twisted-pair	---	---	Host computer-to-PC, PC-to-PC
Controller Link	Yes	Yes	---	2 Mbps	Twisted-pair cables: 500 m	32	Special (twisted-pair) cables	32000 words	---	PC-to-PC, personal computer-to-PC
DeviceNet (CompoBus/D)	Yes	---	Yes	500 Kbps Communications cycle: Approx. 5 ms (128 inputs, 128 outputs)	100 m	63	Special cables	---	2,048	PC-to-Slave (Slaves: Remote I/O Terminals, Remote Adapters. Sensor Terminals, CQM1 I/O Link Units, Analog Output Terminals, Analog Input Terminals)

Network	Communications			Max. baud rate	Communications distance	Max. No. of Units	Communications medium	Data link capacity (per network)	Max. remote I/O points	Connectable devices
	Messages	Data link	Remote I/O							
CompoBus/S	---	---	Yes	750 Kbps Communications cycle: Approx. 1 ms max. (128 inputs, 128 outputs)	100 m	32	Two-core wires, special flat cables	---	256	PC-to-Slave (Slaves: Remote I/O Terminals, Remote I/O Modules, Sensor Terminals, Sensor Amp Terminals, Bit Chain Terminals)

2-6 Unit Current Consumption

The amount of current/power that can be supplied to the Units mounted in a Rack is limited by the capacity of the Rack's Power Supply Unit. Refer to the following tables when designing your system so that the total current consumption of the mounted Units does not exceed the maximum current for each voltage group and the total power consumption does not exceed the maximum for the Power Supply Unit.

2-6-1 CJ-series CPU Racks and Expansion Racks

The following table shows the maximum currents and power that can be supplied by Power Supply Units in CPU Racks and Expansion Racks.

When calculating current/power consumption in a CPU Rack, be sure to include the power required by the CPU Unit itself, as well as the I/O Control Unit if one or more Expansion Racks is connected. Likewise, be sure to include the power required by the I/O Interface Unit when calculating current/power consumption in an Expansion Rack.

Power Supply Unit	Max. Current Consumption			Max. Total Power Consumption
	5-V group (Internal logic)	24-V group (Relays)	24-V group (Service)	
CJ1W-PA205R	5.0 A	0.8 A	None	25 W
CJ1W-PA202	2.8 A	0.4 A	None	14 W
CJ1W-PD025	5.0 A	0.8 A	None	25 W

2-6-2 Example Calculations

Example 1: CPU Rack

In this example, the following Units are mounted to a CPU Rack with a CJ1W-PA205R Power Supply Unit.

Unit	Model	Quantity	Voltage group	
			5-V DC	24-V DC
CPU Unit	CJ1G-CPU45	1	0.910 A	---
I/O Control Unit	CJ1W-IC101	1	0.020 A	
Input Units	CJ1W-ID211	2	0.080 A	---
	CJ1W-ID231	2	0.090 A	---
Output Units	CJ1W-OC201	2	0.090 A	0.048 A
Special I/O Unit	CJ1W-DA041	1	0.120 A	---
CPU Bus Unit	CJ1W-CLK21	1	0.350 A	---

Current Consumption

Group	Current consumption
5 V DC	0.910 A + 0.020 A + 0.080 × 2 + 0.090 A × 2 + 0.090 A × 2 + 0.120 A + 0.350 A = 1.92 A (≤5.0 A)
24 V DC	0.048 A x 2 = 0.096 (≤0.8 A)

Power Consumption

1.92 A × 5 V + 0.096 A × 24 V
= 9.60 W + 2.304 W
= 11.904 W (≤25 W)

Example 2: Expansion Rack

In this example, the following Units are mounted to a CJ-series Expansion Rack with a CJ1W-PA205R Power Supply Unit.

Unit	Model	Quantity	Voltage group	
			5-V DC	24-V DC
I/O Interface Unit	CJ1W-II101	1	0.130 A	---
Input Units	CJ1W-ID211	2	0.080 A	---
Output Units	CJ1W-OD231	8	0.140 A	---

Current Consumption

Group	Current consumption
5 V DC	0.130 A + 0.080 A × 2 + 0.140 A × 8 = 1.41 A (≤5.0 A)
24 V DC	---

Power Consumption

1.41 A × 5 V = 7.05 W (≤25 W)

2-6-3 Current Consumption Tables

5-V DC Voltage Group

Name	Model	Current consumption (A)
CPU Units (including power supplied to CX/Programmer or Programming Console)	CJ1H-CPU66H	0.99 (See note.)
	CJ1H-CPU65H	0.99 (See note.)
	CJ1G-CPU45H	0.91 (See note.)
	CJ1G-CPU44H	0.91 (See note.)
	CJ1G-CPU43H	0.91 (See note.)
	CJ1G-CPU42H	0.91 (See note.)
	CJ1G-CPU45	0.91 (See note.)
	CJ1G-CPU44	0.91 (See note.)
I/O Control Unit	CJ1W-IC101	0.02
I/O Interface Unit	CJ1W-II101	0.13
End Cover	CJ1W-TER01	Included with CPU Unit or I/O Interface Unit power supply.

Note The NT-AL001 Link Adapter consumes 0.15 A/Unit when used.

CJ-series Basic I/O Units

Category	Name	Model	Current consumption (A)
Basic Input Units	DC Input Units	CJ1W-ID211	0.08
		CJ1W-ID231	0.09
		CJ1W-ID232	0.09
		CJ1W-ID261	0.09
		CJ1W-ID262	0.09
	AC Input Units	CJ1W-IA111	0.09
		CJ1W-IA201	0.08
	Interrupt Input Unit	CJ1W-INT01	0.08
Basic Output Units	Transistor Output Units	CJ1W-OD201	0.09
		CJ1W-OD202	0.11
		CJ1W-OD211	0.10
		CJ1W-OD212	0.10
		CJ1W-OD231	0.14
		CJ1W-OD232	0.15
		CJ1W-OD233	0.14
		CJ1W-OD261	0.17
		CJ1W-OD263	0.17
	Relay Output Units	CJ1W-OC201	0.09
		CJ1W-OC211	0.11
	Triac Output Units	CJ1W-OA201	0.22

CJ-series Special I/O Units

Category	Name	Model	Current consumption (A)
Special I/O Units	Analog Input Units	CJ1W-AD081/ AD081-V1	0.42
		CJ1W-AD041-V1	0.42
	Analog Output Units	CJ1W-DA041	0.12
		CJ1W-DA021	0.12
	Temperature Control Unit	CJ1W-TC□□□	0.25
	Position Control Units	CJ1W-NC113/NC133/ NC213/CN233	0.25
		CJ1W-NC413/NC433	0.36
	High-speed Counter Unit	CJ1W-CT021	0.28
	CompoBus/S Master Unit	CJ1W-SRM21	0.15

CJ-series CPU Bus Units

Category	Name	Model	Current consumption (A)
CPU Bus Units	Controller Link Unit	CJ1W-CLK21	0.35
	Serial Communications Unit	CJ1W-SCU41	0.38 (See note.)
	Ethernet Unit	CJ1W-ETN11	0.38
	DeviceNet Unit	CJ1W-DRM21	0.33

Note NT-AL001 Link Adapters consume 0.15/Unit when used.

Current Consumptions for 24-V Supply

Category	Name	Model	Current consumption (A)
Basis Output Units	Relay Contact Output Units	CJ1W-OC201	0.048 (0.006 x number of ON points)
		CJ1W-OC211	0.096 (0.006 x number of ON points)

2-7 CPU Bus Unit Setting Area Capacity

Settings for most CPU Bus Units are stored in the CPU Bus Unit Setting Area in the CPU Unit. Refer to *9-21 Parameter Areas* for details. The CPU Bus Units are allocated the required number of works for settings from this area.

There is a limit to the capacity of the CPU Bus Unit Setting Area of 10,752 bytes (10 Kbytes). The system must be designed so that the number of words used in the CPU Bus Unit Setting Area by all of the CPU Bus Units not exceed this capacity. If the wrong combination of Units is used, the capacity will be exceeded and either Units will operate from default settings only or will not operate at all.

The following table shows the number of bytes required in the CPU Bus Unit Setting Area by each Unit. Any Unit with a usage of "0" does not use the CPU Bus Unit Setting Area at all.

Classification	Name	Model number	Capacity in bytes
CPU Bus Units	Controller Link Unit	CJ1W-CLK21	512
	Serial Communications Unit	CJ1W-SCU41	0
	Ethernet Unit	CJ1W-ETN11	412
	DeviceNet Unit	CJ1W-DRM21	0

2-8 I/O Table Settings List

The setting contents when editing I/O tables with CX-Programmer are as shown below.

2-8-1 CJ-series Basic I/O Units

Unit name	Model	Unit type	Number of allocated Units	Number of allocated words	
				Input	Output
DC Input Units	CJ1W-ID211	16-point Input Unit	---	---	---
	CJ1W-ID231	32-point Input Unit	---	---	---
	CJ1W-ID232	32-point Input Unit	---	---	---
	CJ1W-ID261	64-point Input Unit	---	---	---
	CJ1W-ID262	64-point Input Unit	---	---	---
AC Input Units	CJ1W-IA111	16-point Output Unit	---	---	---
	CJ1W-IA201	16-point Output Unit	---	---	---
Interrupt Input Unit	CJ1W-INT01	16-point Output Unit (16 interrupt points)	---	---	---
Relay Output Units	CJ1W-OC201	16-point Output Unit	---	---	---
	CJ1W-OC211	16-point Output Unit	---	---	---
Triac Output Unit	CJ1W-OA201	16-point Output Unit	---	---	---

Unit name	Model	Unit type	Number of allocated Units	Number of allocated words	
				Input	Output
Transistor Output Units with sinking outputs	CJ1W-OD201	16-point Output Unit	---	---	---
	CJ1W-OD211	16-point Output Unit	---	---	---
	CJ1W-OD231	32-point Output Unit	---	---	---
	CJ1W-OD233	32-point Output Unit	---	---	---
	CJ1W-OD261	64-point Output Unit	---	---	---
	CJ1W-OD263	64-point Output Unit	---	---	---
Transistor Output Units with sourcing outputs	CJ1W-OD202	16-point Output Unit	---	---	---
	CJ1W-OD212	16-point Output Unit	---	---	---
	CJ1W-OD232	32-point Output Unit	---	---	---

Note If the selected Unit is incorrect, an I/O Table Setting error will be generated.

2-8-2 CJ-series Special I/O Units

Unit name	Model	Unit type	Number of allocated Units	Number of allocated words	
				Input	Output
Analog Input Unit	CJ1W-AD041	SIOU (Special I/O Unit)	1	9	1
	CJ1W-AD081 (-V1)		1	9	1
Analog Output Unit	CJ1W-DA021		1	1	9
	CJ1W-DA041		1	1	9
Temperature Control Units	CJ1W-TC001		2	14	6
	CJ1W-TC002		2	14	6
	CJ1W-TC003		2	14	6
	CJ1W-TC004		2	14	6
	CJ1W-TC101		2	14	6
	CJ1W-TC102		2	14	6
	CJ1W-TC103		2	14	6
	CJ1W-TC104		2	14	6
Position Control Units	CJ1W-NC113		1	3	2
	CJ1W-NC213		1	6	4
	CJ1W-NC413		2	12	8
	CJ1W-NC133		1	3	2
	CJ1W-NC233		1	6	4
	CJ1W-NC433		2	12	8
High-speed Counter Unit	CJ1W-CT021		4	26	14
CompoBus/S Master Unit	CJ1W-SRM21		1	6	4
			2	12	8

Note If the selected Unit, the number of input words, or the number of output words is incorrect, a Special I/O Unit Setup error will be generated.

2-8-3 CJ-series CPU Bus Units

Unit name	Model	Unit type	Number of allocated Units	Number of allocated words	
				Input	Output
Controller Link Unit	CJ1W-CLK21	Controller Link Unit	---	---	---
Serial Communications Unit	CJ1W-SCU41	Serial Communications Unit	---	---	---
Ethernet Unit	CJ1W-ETN11	Ethernet Unit	---	---	---
DeviceNet Unit	CJ1W-DRM21	Registration not possible	---	---	---

Note The DeviceNet Unit is not only compatible with versions 2.0 and earlier versions of CX-Programmer and so it cannot be registered in the I/O table. Create an I/O table online.

SECTION 3
Nomenclature, Functions, and Dimensions

This section provides the names of components and their functions for various Units. The Unit dimensions are also provided.

3-1 CPU Units

3-1-1 Models

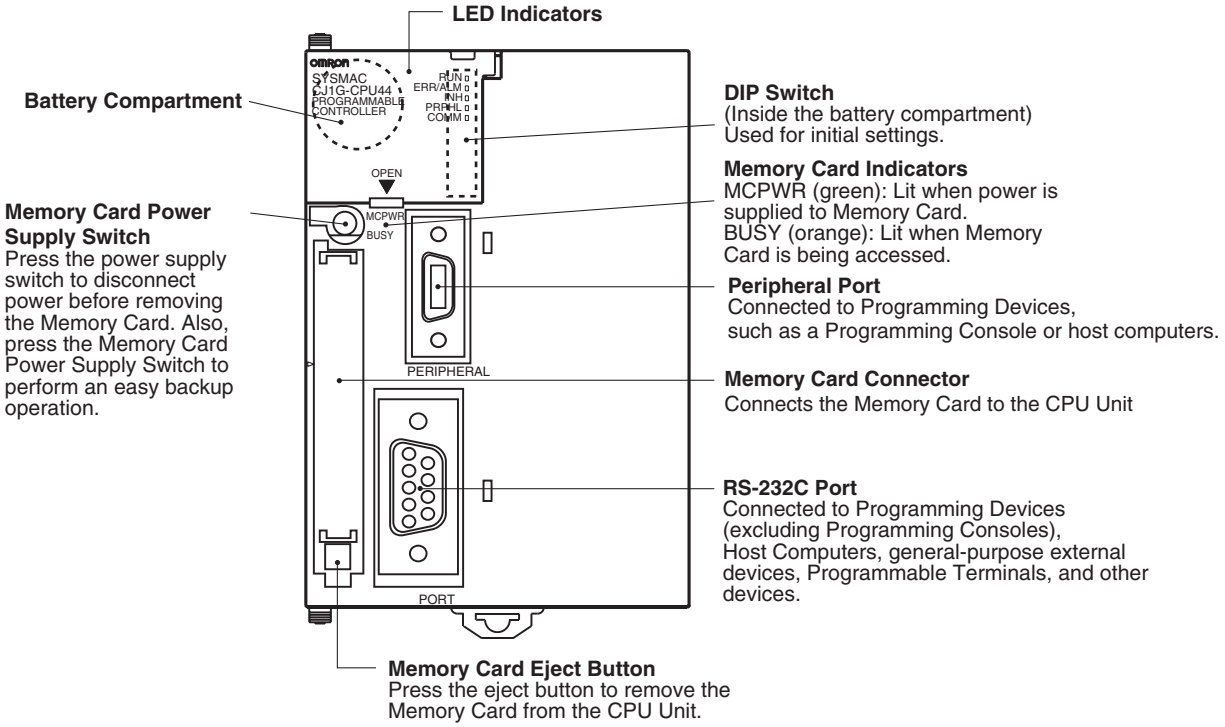
CJ1-H CPU Units

I/O points	Expansion Racks	Programming	Data Memory (DM + EM)	LD instruction processing time	Model	Weight
2,560	3 max.	120 Ksteps	256 Kwords	0.02 μs	CJ1H-CPU66H	200 g max.
		60 Ksteps	128 Kwords		CJ1H-CPU65H	
		60 Ksteps	128 Kwords	0.04 μs	CJ1G-CPU45H	190 g max.
1,280	3 max.	30 Ksteps	64 Kwords		CJ1G-CPU44H	
960	2 max.	20 Ksteps	64 Kwords		CJ1G-CPU43H	
		10 Ksteps	64 Kwords		CJ1G-CPU42H	

CJ1 CPU Units

I/O points	Expansion Racks	Programming	Data Memory (DM + EM)	LD instruction processing time	Model	Weight
1,280	3 max.	60 Ksteps	128 Kwords	0.08 μs	CJ1G-CPU45	200 g max.
		30 Ksteps	64 Kwords		CJ1G-CPU44	

3-1-2 Components

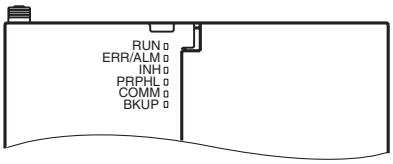


Note Always connect the connector covers to protect them from dust when not using the peripheral or RS-232C port.

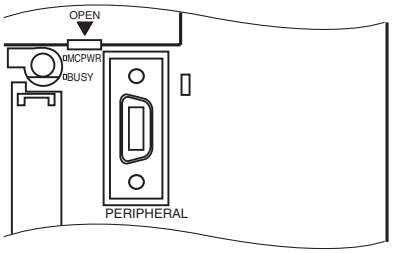
Indicators

The following table describes the LED indicators located on the front panel of the CPU Units.

Indicator	Color	Status	Meaning
RUN	Green	ON	PC is operating normally in MONITOR or RUN mode.
		Flashing	System download mode error or DIP switch settings error.
		OFF	PC has stopped operating while in PROGRAM mode, or has stopped operating due to a fatal error, or is downloading data from the system.
ERR/ALM	Red	ON	A fatal error has occurred (including FALS instruction execution), or a hardware error (watchdog timer error) has occurred. The CPU Unit will stop operating, and the outputs from all Output Units will turn OFF.
		Flashing	A non-fatal error has occurred (including FAL instruction execution) The CPU Unit will continue operating.
		OFF	CPU Unit is operating normally.
INH	Orange	ON	Output OFF Bit (A50015) has been turned ON. The outputs from all Output Units will turn OFF.
		OFF	Output OFF Bit (A50015) has been turned OFF.
PRPHL	Orange	Flashing	CPU Unit is communicating (sending or receiving) via the peripheral port.
		OFF	CPU Unit is not communicating via the peripheral port.
COMM	Orange	Flashing	CPU Unit is communicating (sending or receiving) via the RS-232C port.
		OFF	CPU Unit is not communicating via the RS-232C port.
BKUP (CJ1-H CPU Units only)	Orange	ON	User program and parameter area data is being backed up to flash memory in the CPU Unit or being restored from flash memory. **Note** Do not turn OFF the power supply to the PC while this indicator is lit.
		OFF	Data is not being written to flash memory.



Indicator	Color	Status	Meaning
MCPWR	Green	ON	Power is being supplied to the Memory Card.
		Flashing	Flashes once: Easy backup read, write, or verify normal Flashes five times: Easy backup write malfunction Flashes three times: Easy backup write warning Flashes continuously: Easy backup read or verify malfunction
		OFF	Power is not being supplied to the Memory Card.
BUSY	Orange	Flashing	Memory Card is being accessed.
		OFF	Memory Card is not being accessed.



DIP Switch

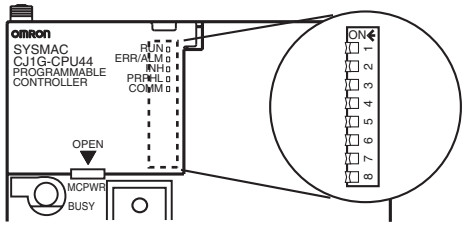
The CJ-series CPU Unit has an 8-pin DIP switch that is used to set basic operational parameters for the CPU Unit. The DIP switch is located under the cover of the battery compartment. The DIP switch pin settings are described in the following table.

Pin no.	Setting	Function	Usage	Default
1	ON	Writing disabled for user program memory. (See note.)	Used to prevent programs from being accidently overwritten from Programming Devices (including Programming Console).	OFF
	OFF	Writing enabled for user program memory.		
2	ON	The user program is automatically transferred from the Memory Card when power is turned ON.	Used to store the programs in the Memory Card to switch operations, or to automatically transfer programs at power-up (Memory Card ROM operation). **Note** When pin 7 is ON and pin 8 is OFF, easy backup reading from the Memory Card is given priority, so even if pin 2 is ON, the user program is not automatically transferred from the Memory Card when power is turned ON.	OFF
	OFF	The user program is not automatically transferred from the Memory Card when power is turned ON.		
3	---	Not used.	---	OFF
4	ON	Peripheral port communications parameters set in the PC Setup are used.	Turn ON to use the peripheral port for a device other than Programming Console or CX-Programmer (Peripheral bus only).	OFF
	OFF	Peripheral port communications parameters set using Programming Console or CX-Programmer (Peripheral bus only) are used.		
5	ON	RS-232C port communications parameters set using a CX-Programmer (Peripheral bus only) are used.	Turn ON to use the RS-232C port for a Programming Device.	OFF
	OFF	RS-232C port communications parameters set in the PC Setup are used.		
6	ON	User-defined pin. Turns OFF the User DIP Switch Pin Flag (A39512).	Set pin 6 to ON or OFF and use A39512 in the program to create a user-defined condition without using an I/O Unit.	OFF
	OFF	User-defined pin. Turns ON the User DIP Switch Pin Flag (A39512).		
7	ON	Writing from the CPU Unit to the Memory Card.	Press and hold the Memory Card Power Supply Switch for three seconds.	OFF
		Restoring from the Memory Card to the CPU Unit.	To read from the Memory Card to the CPU Unit, turn ON the PC power. This operation is given priority over automatic transfer (pin 2 is ON) when power is ON.	
	OFF	Verifying contents of Memory Card.	Press and hold the Memory Card Power Supply Switch for three seconds.	
8	OFF	Always OFF.		OFF

Note

1. The following data cannot be overwritten when pin 1 is ON:
   - All parts of the user program (programs in all tasks)
   - All data in the parameter area (such as the PC Setup and I/O table)

   When pin 1 is ON, the user program and parameter area will not be cleared when the memory clear operation is performed from a Programming Device.
2. The CPU Unit will not enter any mode except PROGRAM mode after backing up data to a Memory Card using DIP switch pin 7. To enter RUN or MONITOR mode, turn OFF the power supply, turn OFF pin 7, and then restart the PC. This will enable changing the operating mode as normal.



Note The language displayed for the CJ-series CPU Units is not set on the DIP switch, but rather is set using Programming Console keys.

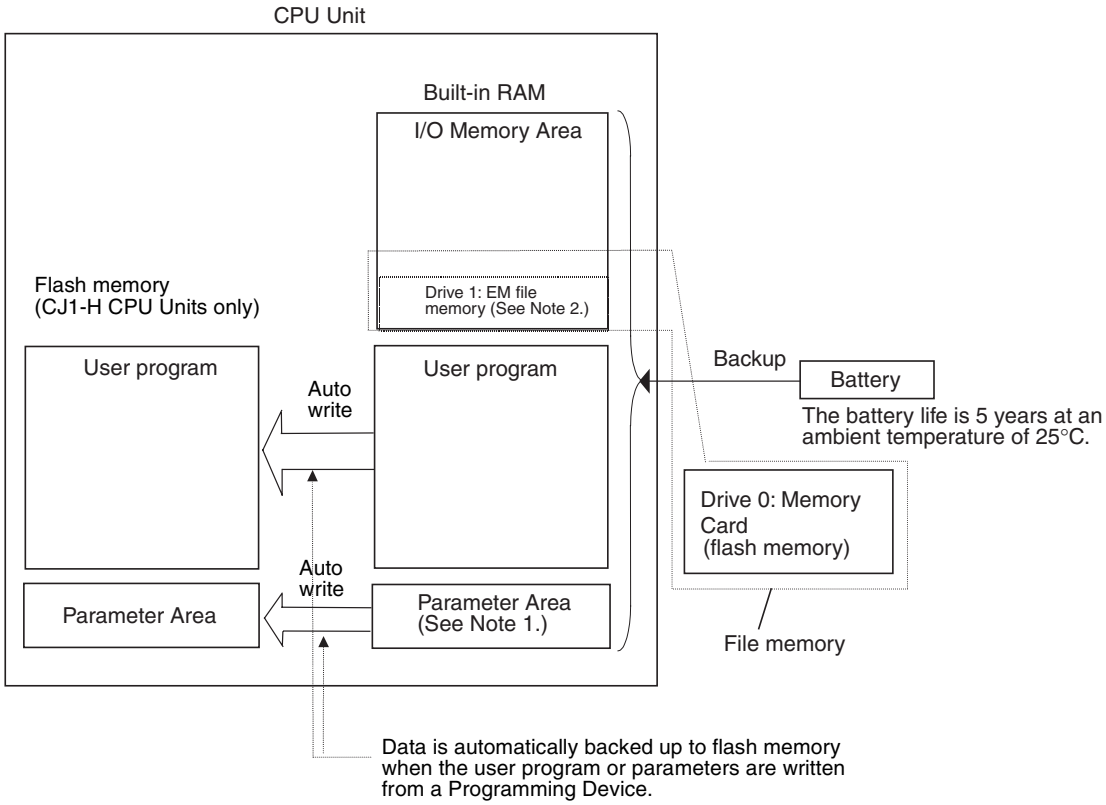
3-1-3 CPU Unit Memory Block Map

The memory of CJ-series CPU Units is configured in the following blocks.

- I/O Memory: The data areas accessible from the user program
- User Memory: The user program and parameter areas (See Note 1.)

The memory block and user memory block have battery back-up using the CPM2A-BAT01 Battery Set. If the battery voltage is low, the data in these areas will be erased.

With the CJ1-H CPU Units, however, the CPU Unit has a built-in flash memory to which the user program and parameter area data is backed up whenever the user memory is written to, including data transfers and online editing from a Programming Device (CX-Programmer or Programming Console, data transfers from a Memory Card, etc. The user program and the parameter area data will thus not be lost when using a CJ1-H CPU Unit.

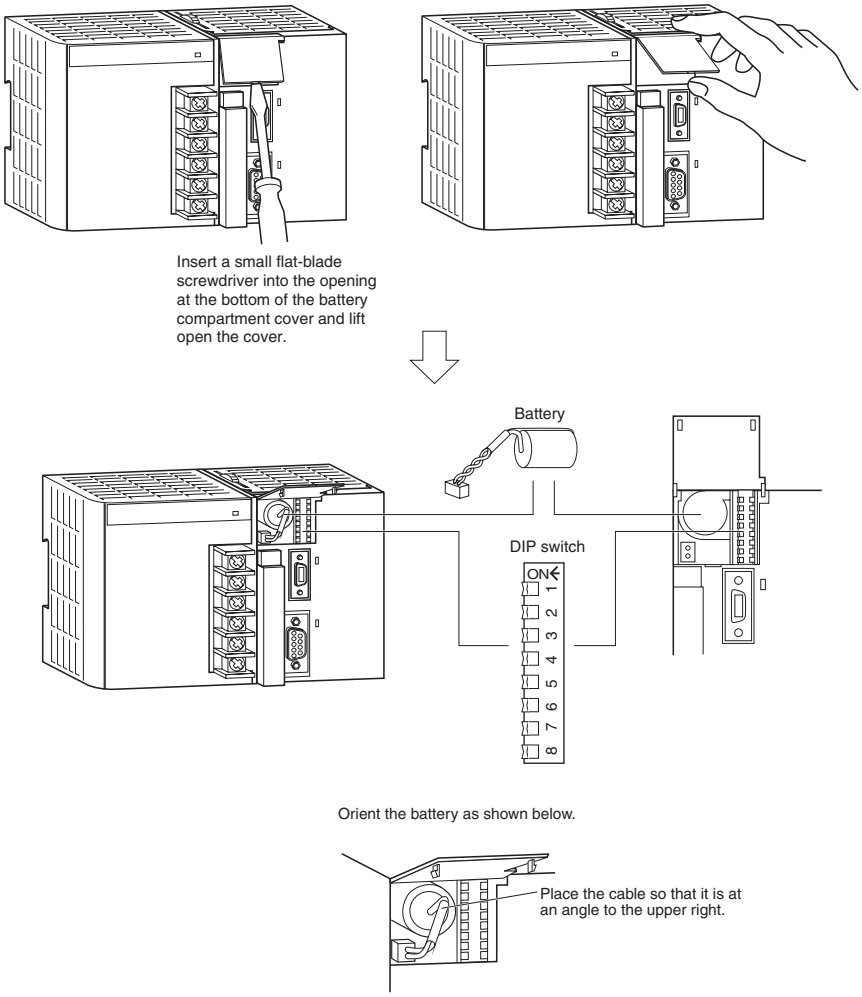


Note

1. The Parameter Area stores system information for the CPU Unit, such as the PC Setup. An attempt to access the Parameter Area by an instruction will generate an illegal access error.
2. Part of the EM (Extended Data Memory) Area can be converted to file memory to handle data files and program files in RAM memory format, which has the same format as Memory Cards.

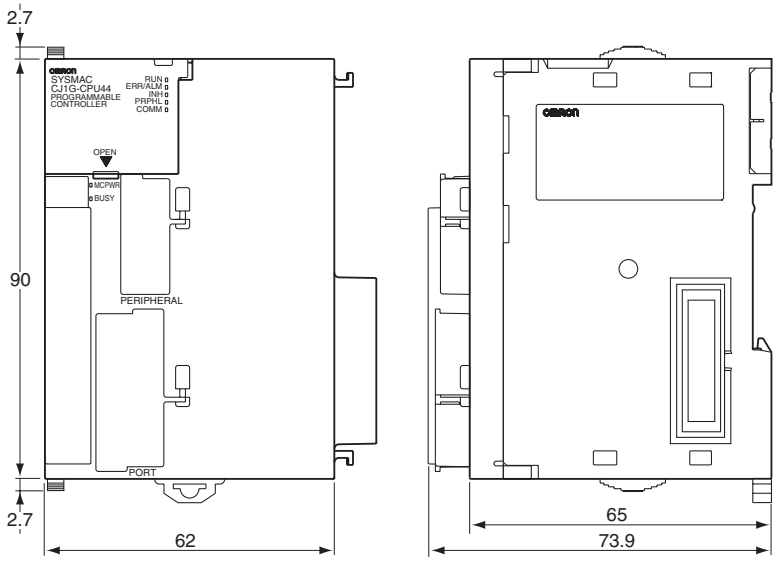
Opening the Battery Compartment Cover

Insert a small flat-blade screwdriver into the opening at the bottom of the battery compartment cover and lift open the cover.



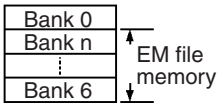
3-1-4 Dimensions

CJ1G-CPU□□
CJ1G/H-CPU□□H

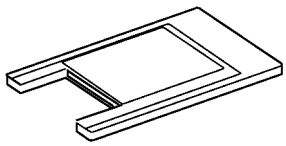


3-2 File Memory

For CJ-series CPU Units, the Memory Card and a specified part of the EM Area can be used to store files. All user programs, the I/O Memory Area, and the Parameter Area can be stored as files.

File memory	Memory type	Memory capacity	Model
Memory Card 	Flash memory	8 Mbytes	HMC-EF861
		15 Mbytes	HMC-EF171
		30 Mbytes	HMC-EF371
		48 Mbytes	HMC-EF571
EM file memory 	RAM	The maximum capacity of the CPU Unit's EM Area (e.g., the maximum capacity for a CPU66 is 448 Kbytes)	The specified bank (set in the PC Setup) to the last bank of the EM Area in the I/O Memory.

Note
1. A Memory Card can be written up to approximately 100,000 times.
2. The HMC-AP001 Memory Card Adapter is shown below.



3-2-1 Files Handled by CPU Unit

Files are ordered and stored in the Memory Card or EM file memory according to the file name and the extension attached to it.

General-use Files

File type	Contents		File name	Extension
Data files	Specified range in I/O memory	Binary	******** (See note 1.)	.IOM
		Text		.TXT
		CSV		.CSV
Program files	All user programs			.OBJ
Parameter files	PC Setup, registered I/O tables, routing tables, CPU Bus Unit settings, and Controller Link data link tables			.STD

Files Transferred Automatically at Startup

File type	Contents	File name	Extension
Data files	DM area data (stores data for specified number of words starting from D20000)	AUTOEXEC	.IOM
	DM area data (stores data for specified number of words starting from D00000)	ATEXECDM	.IOM
	EM area for bank No. □ (stores data for specified number of words starting from E□_00000)	ATEXECE□	.IOM
Program files	All user programs	AUTOEXEC	.OBJ
Parameter files	PC Setup, registered I/O tables, routing tables, CPU Bus Unit settings, and Controller Link data link tables	AUTOEXEC	.STD

Easy Backup Files

File type	Contents	File name	Extension
Data files	Words allocated to Special I/O Units, and CPU Bus Units in the DM area	BACKUP	.IOM
	CIO area	BACKUPIO	.IOR
	General-purpose DM area	BACKUPDM	.IOM
	General-purpose EM area	BACKUPE□	.IOM
Program files	All user programs	BACKUP	.OBJ
Parameter files	PC Setup, registered I/O tables, routing tables, CJ-series CPU Bus Unit settings, and Controller Link link tables		.STD
Unit backup files (CJ1-H CPU Units only)	Data from specific Units (e.g., protocol macro data for a Serial Communications Unit)	BACKUP□□	.PRM

Note

1. Specify 8 ASCII characters. For a file name with less than 8 characters, add spaces (20 Hex).
2. Always specify the name of files to be transferred automatically at power-up as AUTOEXEC.
3. Easy backup file names must be named BACKUP□□.

3-2-2 Initializing File Memory

File memory	Initializing procedure	Data capacity after initialization
Memory Card	1.Install Memory Card into CPU Unit. 2.Initialize the Memory Card using a Programming Device (including the CX-Programmer and Programming Consoles).	Essentially the specific capacity of the Memory Card
EM file memory	1.Convert the part of the EM Area from the specified bank No. to the last bank No. to file memory in the PC Setup. 2.Initialize the EM file memory using a Programming Device (including the CX-Programmer and Programming Consoles).	1 bank: Approx. 61 KB 7 banks: Approx. 445 KB

3-2-3 Using File Memory

Note For details on using file memory, refer to the *CS/CJ Series Programming Manual*.

Memory Card

Reading/Writing Files Using Programming Device (CX-Programmer or Programming Console)

File	File name and extension	Data transfer direction
Program files	********.OBJ	Between CPU Unit and Memory Card,
Data files	********.IOM	
Parameter files	********.STD	

1,2,3...

1. Install the Memory Card into the CPU Unit.
2. Initialize the Memory Card if necessary.
3. Name the file containing the data in the CPU Unit and save the contents in the Memory Card.
4. Read the file that is saved in the Memory Card to the CPU Unit.

Automatically Transferring Memory Card Files to the CPU Unit at Power-up

File	File name and extension	Data transfer direction
Program files	AUTOEXEC.OBJ	From Memory Card to CPU Unit
Data files	AUTOEXEC.IOM ATEXECDM.IOM ATEXECE□.IOM	
Parameter files	AUTOEXEC.STD	

1,2,3...

1. Install the Memory Card into the CPU Unit.
2. Set pin 2 of the DIP switch to ON.
3. The files are read automatically when the power is turned ON.

Reading/Writing Data Files Using FREAD(700)and FWRIT(701)

File	File name and extension	Data transfer direction
Data files	********.IOM ********.TXT ********.CSV	Between CPU Unit and Memory Card

1,2,3...

1. Install the Memory Card into the CPU Unit.
2. Initialize the Memory Card using a Programming Device.
3. Using the FWRIT(701) instruction, name the file of the specified I/O memory area, and save to the Memory Card.
4. Using the FREAD(700) instruction, read the I/O memory files from the Memory Card to the I/O memory in the CPU Unit.

Note When using spreadsheet software to read data that has been written to the Memory Card in CSV or text format, it is now possible to read the data using Windows applications by mounting a Memory Card in the personal computer card slot using a HMC-AP001 Memory Card Adapter.

Reading and Replacing Program Files during Operation

File	File name and extension	Data transfer direction
Program files	********.OBJ	Memory Card to CPU Unit

1,2,3...

1. Install a Memory Card into the CPU Unit.
2. Set the following information: Program File Name (A654 to A657) and Program Password (A651).
3. Next, from the program, turn ON the Replacement Start Bit (A65015).

Backing Up or Restoring CPU Unit Data and, for CJ1-H CPU Units, Special Data for CPU Bus Units

File	File name and extension	Data transfer direction
Program files	BACKUP.OBJ	CPU Unit to Memory Card (when backing up) Memory Card to CPU Unit (when restoring)
Data files	BACKUP.IOM	
	BACKUPIO.IOR	
	BACKUPDM.IOM	
	BACKUPE□.IOM	
Parameter files	BACKUP.STD	
Unit backup files (CJ1-H CPU Units only)	BACKUP□□.PRM	

1,2,3...

1. Install a Memory Card into the CPU Unit.
2. Turn ON pin 7 on the DIP switch.
3. To back up data, press and hold the Memory Card Power Supply Switch for three seconds. To restore data, turn ON the PC power.

Transferring Files between Memory Cards and the CX-Programmer

The following files can be transferred between a Memory Card and the CX-Programmer.

File	File name and extension	Data transfer direction
Symbols file	SYMBOLS.SYM	Between CX-Programmer and Memory Card
Comment file	COMMENTS.CNT	

1,2,3...

1. Insert a formatted Memory Card into the CPU Unit.
2. Place the CX-Programmer online and use the file transfer operations to transfer the above files from the personal computer to the PC or from the PC to the personal computer.

Reading/Writing EM File Memory Files Using Programming Device (CX-Programmer or Programming Console)

File	File name and extension	Data transfer direction
Program files	********.OBJ	Between CPU Unit and EM file memory
Data files	********.IOM	
Parameter files	********.STD	

1,2,3... 1. Convert the part of the EM Area specified by the first bank number into file memory in the PC Setup.
2. Initialize the EM file memory using a Programming Device.
3. Name the data in the CPU Unit and save in the EM file memory using the Programming Device.
4. Read the EM file memory files to the CPU Unit using the Programming Device.

Reading/Writing Data Files in EM File Memory Using FREAD(700)and FWRIT(701)

File	File name and extension	Data transfer direction
Data files	********.IOM	Between CPU Unit and EM file memory

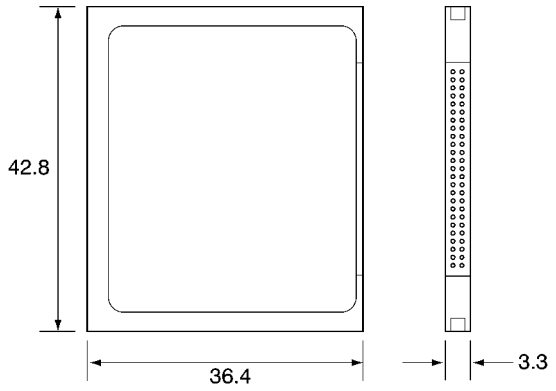
1,2,3... 1. Convert the part of the EM Area specified by the first bank number into file memory in the PC Setup.
2. Initialize the EM file memory using a Programming Device.
3. Using the FWRIT(701) instruction, name the specified area in I/O memory with a file name and save in the EM file memory.
4. Using the FREAD(700) instruction, read the I/O memory files from the EM file memory to the I/O memory in the CPU Unit.

Note The following files can be transferred between EM file memory and the CX-Programmer.

File	File name and extension	Data transfer direction
Symbols file	SYMBOLS.SYM	Between CX-Programmer and EM file memory
Comment file	COMMENTS.CNT	

1,2,3... 1. Format the EM Area in the CPU Units as file memory.
2. Place the CX-Programmer online and use the file transfer operations to transfer the above files from the personal computer to the PC or from the PC to the personal computer.

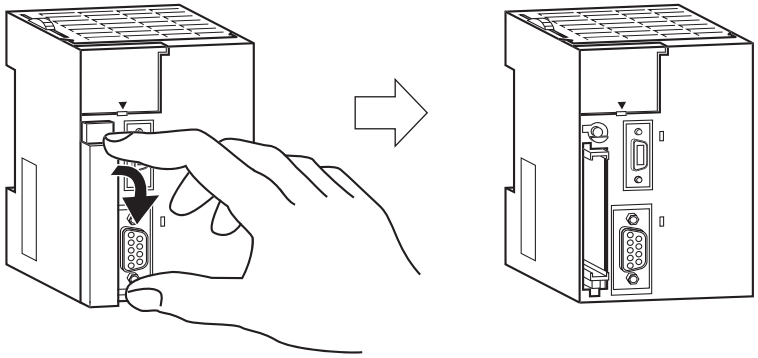
3-2-4 Memory Card Dimensions



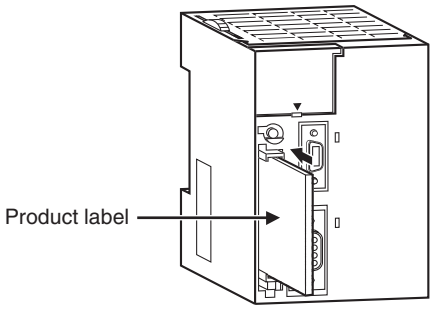
3-2-5 Installing and Removing the Memory Card

Installing the Memory Card

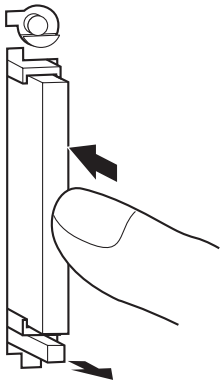
1,2,3... 1. Pull the top end of the Memory Card cover forward and remove from the Unit.



2. Insert the Memory Card with the label facing to the right. (Insert with the Δ on the Memory Card label and the Δ on the CPU Unit facing each other.)

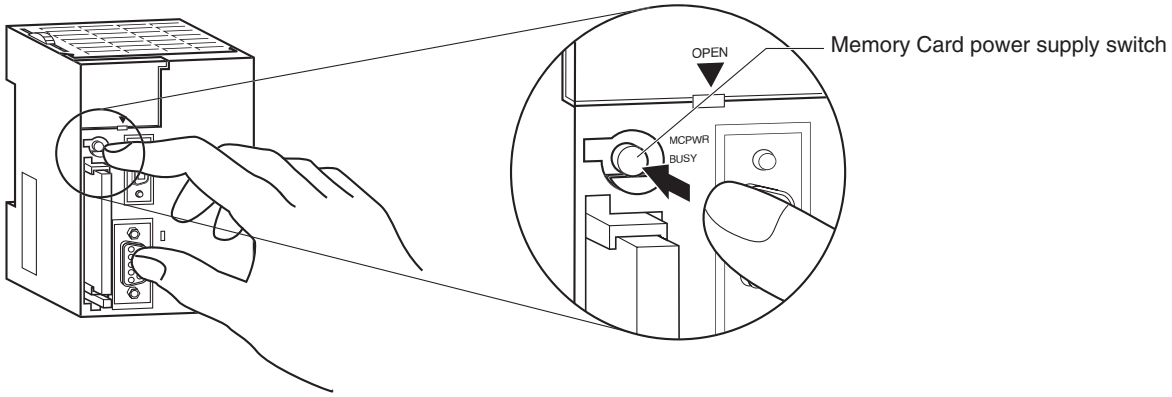


3. Push the Memory Card securely into the compartment. If the Memory Card is inserted correctly, the Memory Card eject button will be pushed out.

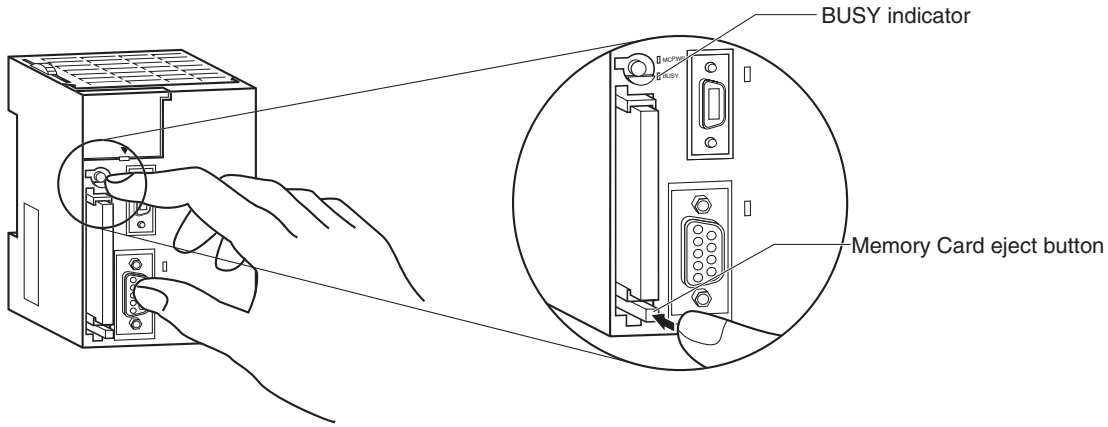


Removing the Memory Card

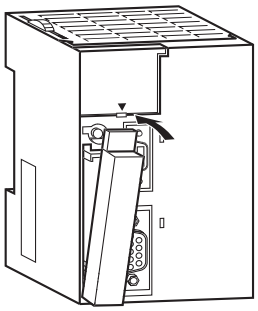
1,2,3... 1. Press the Memory Card power supply switch.



2. Press the Memory Card eject button after the BUSY indicator is no longer lit.

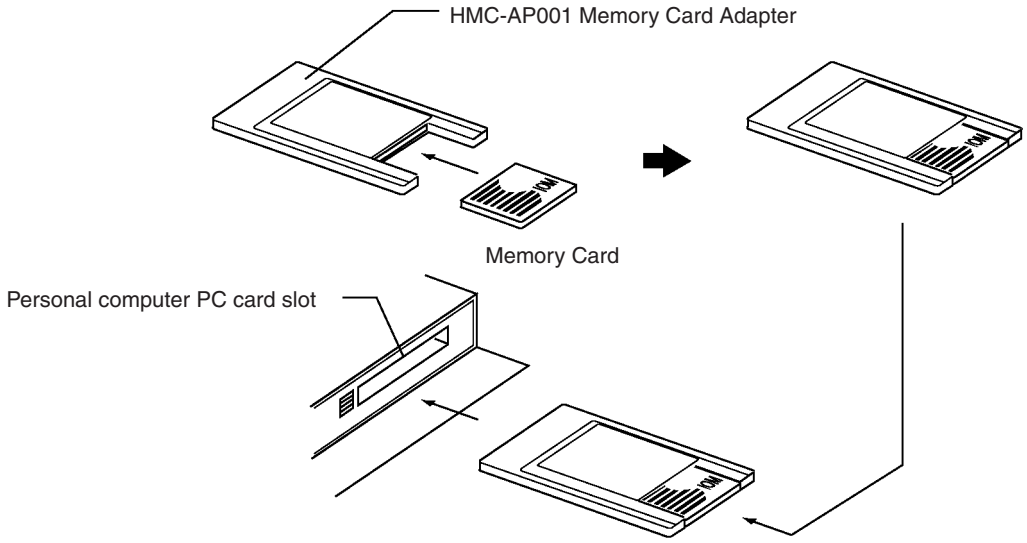


3. The Memory Card will eject from the compartment.
4. Remove the Memory Card cover when a Memory Card is not being used.



Note
1. Never turn OFF the PC while the CPU is accessing the Memory Card.
2. Never remove the Memory Card while the CPU is accessing the Memory Card. Press the Memory Card power supply switch and wait for the BUSY indicator to go OFF before removing the Memory Card. In the worst case, the Memory Card may become unusable if the PC is turned OFF or the Memory Card is removed while the Card is being accessed by the CPU.
3. Never insert the Memory Card facing the wrong way. If the Memory Card is inserted forcibly, it may become unusable.

Installing the Memory Card into a Personal Computer



Note
1. When a Memory Card is inserted into a computer using a Memory Card Adapter, it can be used as a standard storage device, like a floppy disk or hard disk.
2. When deleting all of the data in a Memory Card or formatting it in any way, always place it in the CPU Unit and perform the operation from the CX-Programmer or a Programming Console.

3-3 Programming Devices

There are 2 types of Programming Devices that can be used: Any of three models of Hand-held Programming Consoles or the CX-Programmer, which is operated on a Windows computer. The CX-Programmer is usually used to write the programs, and a Programming Console is then used to change the operating modes, edit the programs, and monitor a limited number of points.

The following table provides a comparison between the CX-Programmer functions and the Programming Console functions.

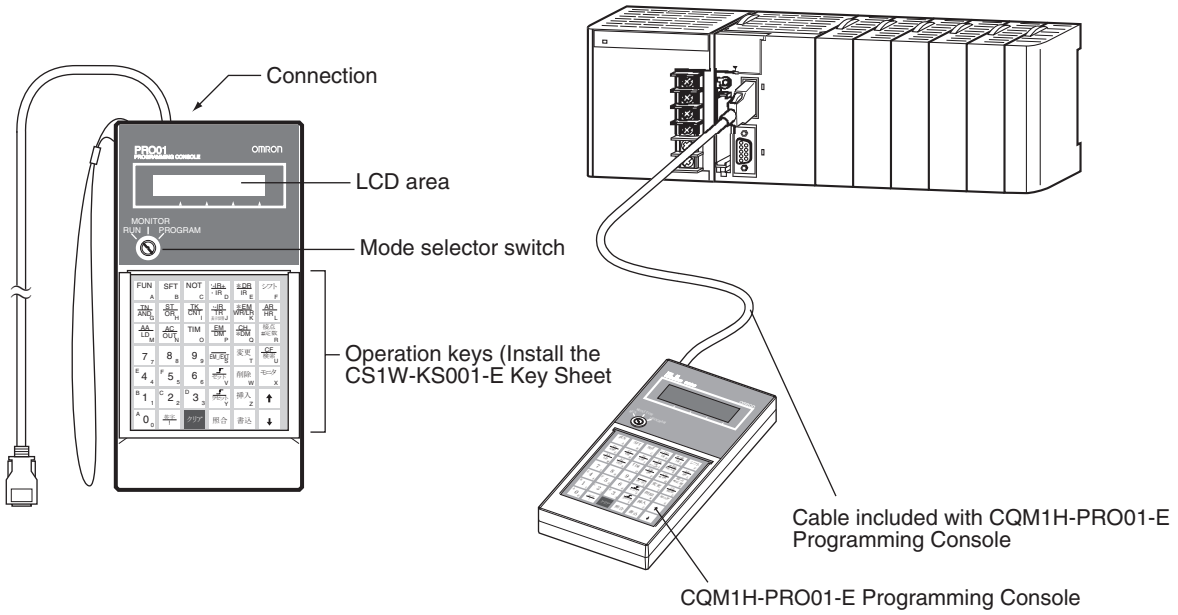
Function		Programming Console	CX-Programmer
Editing and referencing I/O tables		Yes	Yes
Deleting I/O tables		No	Yes
Selecting tasks		Yes	Yes
Writing programs	Inputting instructions	Writes instructions one at a time using mnemonics	Writes multiple blocks using mnemonics or ladder programs
	Inputting addresses	Addresses only	Addresses or symbols
	I/O comment, rung comment	No	Yes
	Setting global/local symbols	No	Yes (Automatic allocation of local symbols)
Editing programs		Inserts instructions and searches for program addresses	Yes (Cutting, pasting, inserting within programs; searching/exchanging instructions, addresses, and symbols; displaying cross-references)
Checking programs		No	Yes
Monitoring programs		Monitors in program address units	Monitors multiple blocks
Monitoring I/O memory		Simultaneous, 2 points max.	Monitors multiple points

Function		Programming Console	CX-Programmer
Changing I/O memory present values		Changes 1 point at a time	Yes
Online editing		Edits in instruction units	Edits multiple adjacent blocks
Debugging	Changing timer and counter settings	Yes	Yes
	Control set/ reset	Executes 1 point at a time (or resets all at once)	Yes
	Differentiation monitoring	Yes	Yes
	Reading cycle time	Yes	Yes
	Data tracing	No	Yes
	Time chart monitoring	No	Yes
Reading error information		Yes (error message display)	Yes
Reading error log		No	Yes
Reading/setting timer information		Yes	Yes
Reading/setting PC parameters		Yes	Yes
Setting CPU Bus Unit parameters		No	Yes
File memory operations	Initializing Memory Card	Yes	Yes
	Initializing EM file memory	Yes	Yes
	Transferring files between CPU Unit and file memory	Yes	Yes
Remote programming and monitoring	Between Host Link and Network PC	No	Yes
	Via modem	No	Yes
Setting password protection		No	Yes
Managing files		No	Manages files by project.
Printing		No	Yes

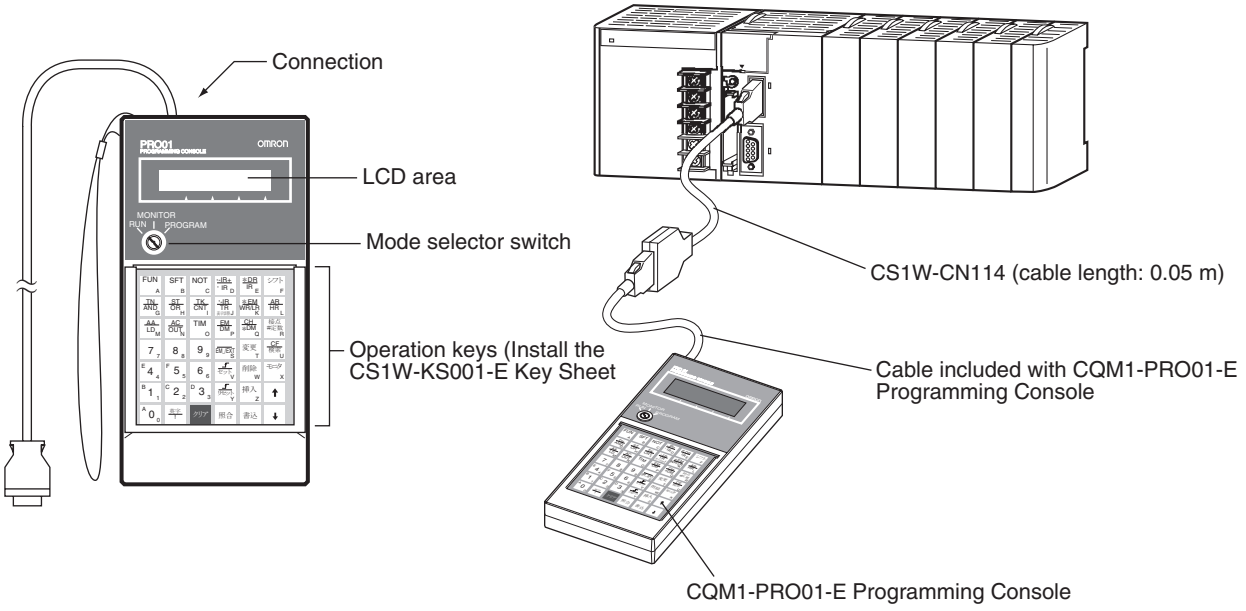
3-3-1 Programming Consoles

There are three Programming Consoles that can be used with the CJ-series CPU Units: The CQM1H-PRO01-E, CQM1-PRO01-E, and C200H-PRO27-E. These Programming Consoles are shown here.

CQM1H-PRO01-E Programming Console

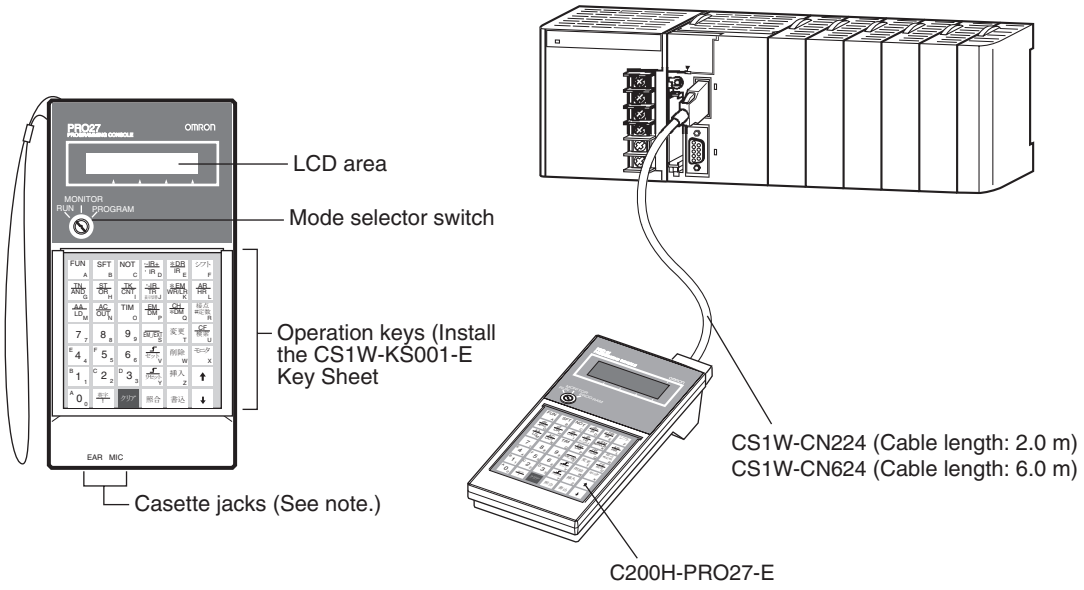


CQM1-PRO01-E Programming Console

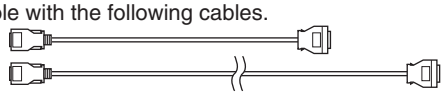


Connect the CPU Unit to the Programming Console with the following cables.
CS1W-CN114 (Cable length: 0.05 m)

C200H-PRO27-E Programming Console



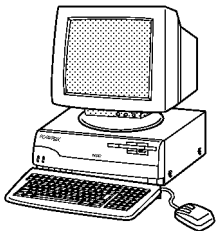
Connect the CPU Unit to the Programming Console with the following cables.
CS1W-CN224 (Cable length: 2.0 m)
CS1W-CN624 (Cable length: 6.0 m)



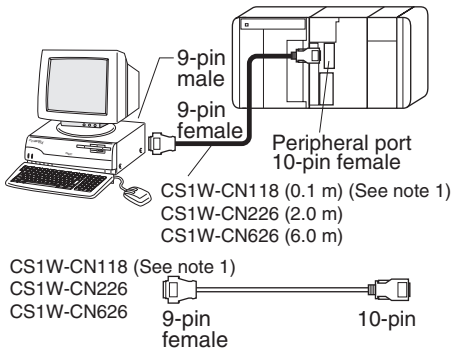
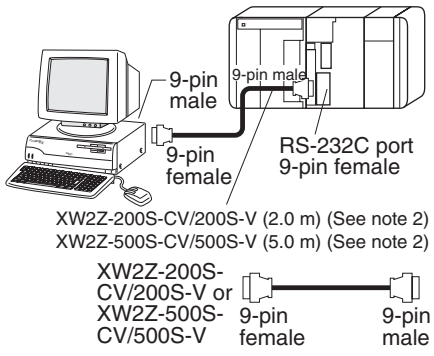
Note The cassette jacks are not used with CJ-series CPU Units.

3-3-2 CX-Programmer

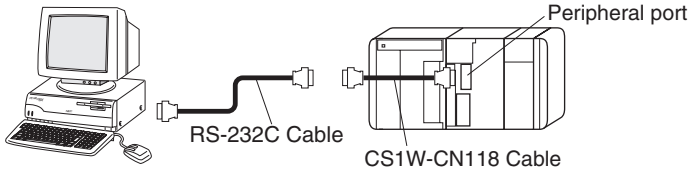
Item	Details
Applicable PC	CS/CJ-series, CV-series, C200HX/HG/HE (-Z), C200HS, CQM1, CPM1, CPM1A, SRM1, C1000H/2000H
Personal computer	DOS version
OS	Microsoft Windows 95, 98, Me, 2000, or NT 4.0
Connection method	CPU Unit's peripheral port or built-in RS-232C port
Communications protocol with PC	Peripheral bus or Host Link
Offline operation	Programming, I/O memory editing, creating I/O tables, setting PC parameters, printing, program changing
Online operation	Transmitting, referencing, monitoring, creating I/O tables, setting PC parameters
Basic functions	1.Programming: Creates and edits ladder programs and mnemonic programs for the applicable PC. 2.Creating and referencing I/O tables. 3.Changing the CPU Unit operating mode. 4.Transferring: Transfers programs, I/O memory data, I/O tables, PC Setup, and I/O comments between the personal computer and the CPU Unit. 5.Program execution monitoring: Monitors I/O status/present values on ladder displays, I/O status/present values on mnemonic displays, and present values on I/O memory displays



Connections

Personal computer	Peripheral port connection	RS-232C port connection
DOS		

Note 1. The CJ1W-CN118 Cable is used with one of the RS-232C Cables shown on the right (XW2Z-□□□□-□□) to connect to the peripheral port on the CPU Unit.



2. If cables with model numbers ending in -V instead of -CV are used to connect the computer running the CX-Programmer to the RS-232C port (including when using a CJ1W-CN118 Cable), a peripheral bus connection cannot be used. Use a Host Link (SYSMAC WAY) connection. To connect to the port using a peripheral bus connection, prepare an RS-232C cable as described in *3-3-4 RS-232C Port Specifications*.

CX-Programmer Connecting Cables

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in peripheral port	DOS	D-Sub, 9-pin, male	Peripheral Bus or Host Link	CJ1W-CN226	2.0 m	---
					CJ1W-CN626	6.0 m	
	Built-in RS-232C port D-Sub, 9-pin, female	DOS	D-Sub, 9-pin, male	Peripheral Bus or Host Link	XW2Z-200S-CV	2 m	Use a static-resistant connector.
					XW2Z-500S-CV	5 m	
Serial Communications Units	RS-232C Port D-Sub, 9-pin, female	DOS	D-Sub, 9-pin, male	Host Link	XW2Z-200S-CV	2 m	Use a static-resistant connector.
					XW2Z-500S-CV	5 m	

Note Before connecting a connector from the above table to the RS-232C port, touch a grounded metal object to discharge static electricity from your body.

The XW2Z-□□□S-CV Cables have been strengthened against static because they use a static-resistant connector hood (XM2S-0911-E). Even so, always discharge static electricity before touching the connectors.

Do not use commercially available RS-232C personal computer cables. Always use the special cables listed in this manual or make cables according to manual specifications. Using commercially available cables may damage the external devices or CPU Unit.

RS-232C Cables for a Peripheral Port

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in peripheral port	DOS	D-Sub, 9-pin, male	Peripheral Bus or Host Link	CJ1W-CN118 + XW2Z-200S-CV/ 500S-CV	0.1 m+ (2 m or 5 m)	XW2Z-□□□S-CV models use a static -resistant connector

Using a CQM1-CIF01/02 Cable for a Peripheral Port

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in peripheral port	DOS	D-Sub, 9-pin, male	Host Link	CJ1W-CN114 + CQM1-CIF02	0.05 m + 3.3 m	---

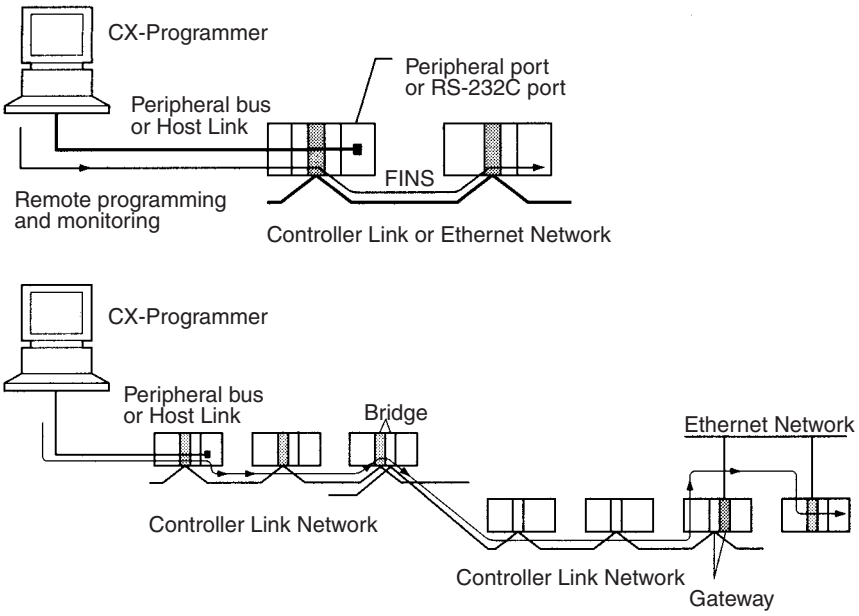
Using a RS-232C Cable for a IBM PC/AT or Compatible

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in RS-232C port D-Sub, 9-pin, female	DOS	D-Sub, 9-pin, male	Host Link	XW2Z-200S-V	2 m	---
					XW2Z-500S-V	5 m	
Serial Communications Units	RS-232C port D-Sub, 9-pin, female	DOS	D-Sub, 9-pin, male	Host Link	XW2Z-200S-V	2 m	
					XW2Z-500S-V	5 m	

Communications Modes when Connecting a CX-Programmer to a CJ-series CPU Unit

Serial communications mode	Characteristics
Peripheral Bus	High-speed communications are possible. Consequently, connecting via a peripheral bus is recommended when using a CX-Programmer. Only 1:1 connection is possible. When using a CJ-series CPU Unit, the baud rate of the communications devices can be automatically recognized for connection.
Host Link	This is a communications protocol with a general-purpose host computer. Either 1:1 or 1:N connections are possible. Host Link communications are slow compared with the Peripheral Bus communications. The following connections are possible: Via a modem or optical fiber adapter, over long distance using a RS-422A/485, and 1:N.

Note The CX-Programmer can be used for remote programming and monitoring. It can be used to program and monitor not only the PC to which it is directly connected, but also to program and monitor any PC connected through a Controller Link or Ethernet network to which the PC that the CX-Programmer is connected to is a part of. All programming and monitoring functionality for the directly connected PC is supported for remote programming and monitoring, the PC can be connected though either the peripheral or an RS-232C port, and either the peripheral bus or Host Link bus can be used. Remote programming is possible for up to three levels of networks (counting the local network but not counting the peripheral bus or Host Link connection between the CX-Programmer and the local PC).



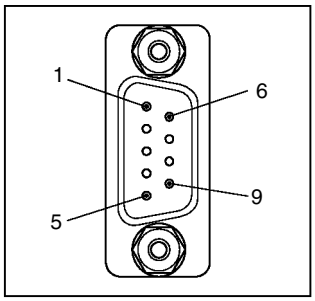
3-3-3 Peripheral Port Specifications

Protocol PC Setup and DIP Switch Settings

Pin No. 4	Peripheral port settings (in PC Setup)			
	Default value: 0 Hex	**NT Link: 2 Hex**	**Peripheral bus: 4 Hex**	**Host Link: 5 Hex**
OFF	Programming Console or other CX-Programmer through peripheral bus (automatically detects the Programming Device's communications parameters)			
ON	Host computer or CX-Programmer (Host Link)	PT (NT Link))	CX-Programmer (Peripheral bus)	Host computer or CX-Programmer (Host Link)

3-3-4 RS-232C Port Specifications

Connector Pin Arrangement

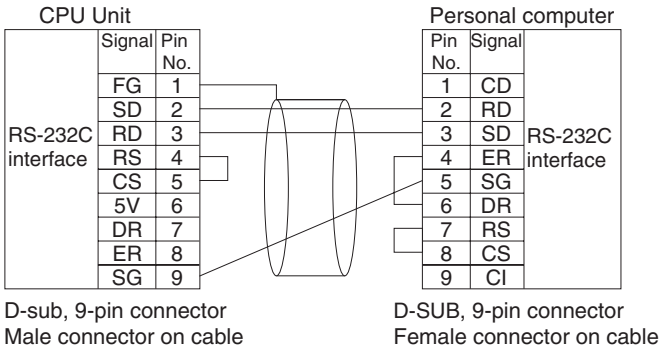


Pin No.	Signal	Name	Direction
1	FG	Protection earth	---
2	SD (TXD)	Send data	Output
3	RD (RXD)	Receive data	Input
4	RS (RTS)	Request to send	Output
5	CS (CTS)	Clear to send	Input
6	5 V	Power supply	---
7	DR (DSR)	Data set ready	Input
8	ER (DTR)	Data terminal ready	Output

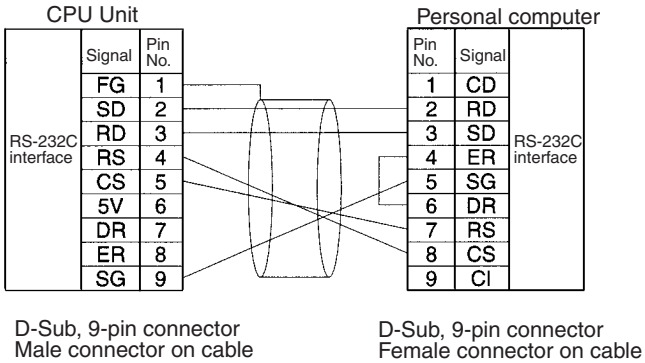
Pin No.	Signal	Name	Direction
9	SG (0 V)	Signal ground	---
Connector hood	FG	Protection earth	---

Connection between CJ-series CPU Unit and Personal Computer

The following connections are in Host Link serial communications mode.



The following connections are in Peripheral Bus serial communications mode.



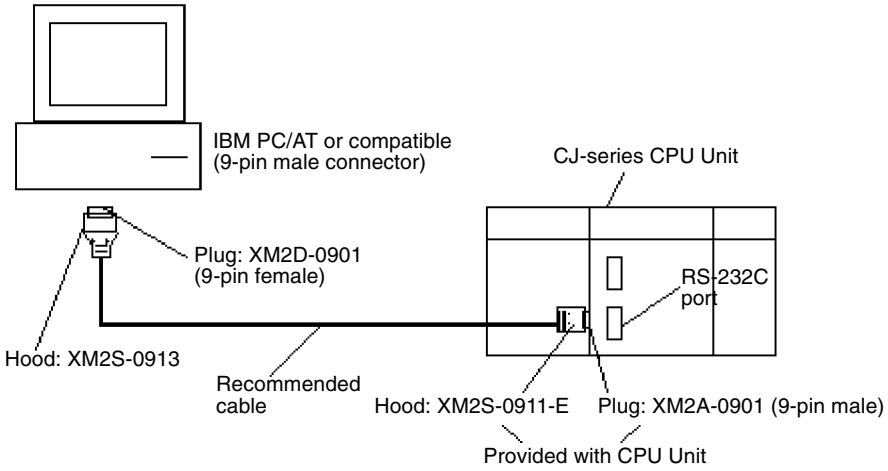
Applicable Connectors

CPU Unit Connector

Item	Model	Specifications	
Plug	XM2A-0901	9-pin male	Used together (One of each provided with CPU Unit.)
Hood	XM2S-0911-E	9-pin, millimeter screws, static-resistant	

Personal Computer Connector

Item	Model	Specifications	
Plug	XM2D-0901	9-pin female	Used together
Hood	XM2S-0913	9-pin, inch screws	



Note Use the special cables provided from OMRON for all connections whenever possible. If cables are produced in-house, be sure they are wired correctly. External devices and the CPU Unit may be damaged if general purpose (e.g., computer to modem) cables are used or if wiring is not correct.

Recommended Cables

Fujikura Ltd.: UL2464 AWG28 × 5P IFS-RVV-SB (UL product)
AWG 28 × 5P IFVV-SB (non-UL product)

Hitachi Cable, Ltd.: UL2464-SB(MA) 5P × 28AWG (7/0.127) (UL product)
CO-MA-VV-SB 5P × 28AWG (7/0.127) (non-UL product)

RS-232C Port Specifications

Item	Specification
Communications method	Half duplex
Synchronization	Start-stop
Baud rate	0.3/0.6/1.2/2.4/4.8/9.6/19.2/38.4/57.6/115.2 kbps (See note.)
Transmission distance	15 m max.
Interface	EIA RS-232C
Protocol	Host Link, NT Link, 1:N, No-protocol, or Peripheral Bus

Note Baud rates for the RS-232C are specified only up to 19.2 kbps. The CJ Series supports serial communications from 38.4 kbps to 115.2 kbps, but some computers cannot support these speeds. Lower the baud rate if necessary.

Protocol PC Setup and DIP Switch Settings

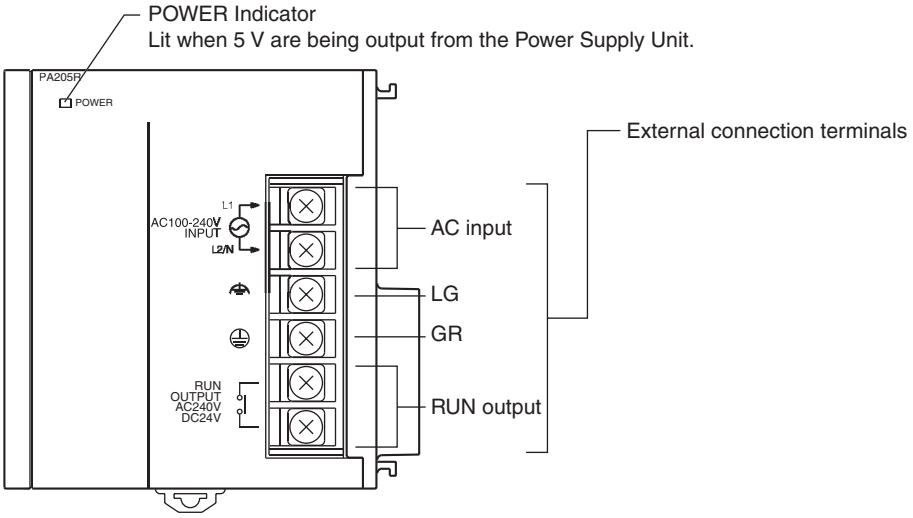
Pin No. 5	RS-232C port settings (in PC Setup)				
	Default value: 0 Hex	**NT Link: 2 Hex**	**No protocol: 3 Hex**	**Peripheral bus: 4 Hex**	**Host Link: 5 Hex**
OFF	Host computer (Host Link)	PT (NT Link)	General-purpose external devices (No protocol)	CX-Programmer (Peripheral bus)	Host computer or CX-Programmer (Host Link)
ON	CX-Programmer (not a Programming Console) connected through the peripheral bus. (The Programming Device's communications parameters are detected automatically.)				

3-4 Power Supply Units

3-4-1 Power Supply Units

Power supply voltage	Output	Power output terminals	RUN output	Model	Weight
100 to 240 V AC (allowable: 85 to 264 V AC) 50/60 Hz (allowable: 47 to 63 Hz)	5 A at 5 V DC 0.8 A at 24 V DC Total: 25 W	No	Yes	CJ1W-PA205R	350 g max.
	2.8 A at 5 V DC 0.4 A at 24 V DC Total: 14 W	No	No	CJ1W-PA202	200 g max.
24 V DC (allowable:19.2 to 28.8 V DC)	5 A at 5 V DC 0.8 A at 24 V DC Total: 25 W	No	No	CJ1W-PD025	300 g max.

3-4-2 Components and Switch Settings



AC Input Supply 100 to 240 V AC (allowable: 85 to 264 V AC). (Voltage selection is not required.)

DC Input Supply 24 V DC (allowable:19.2 to 28.8 V DC).

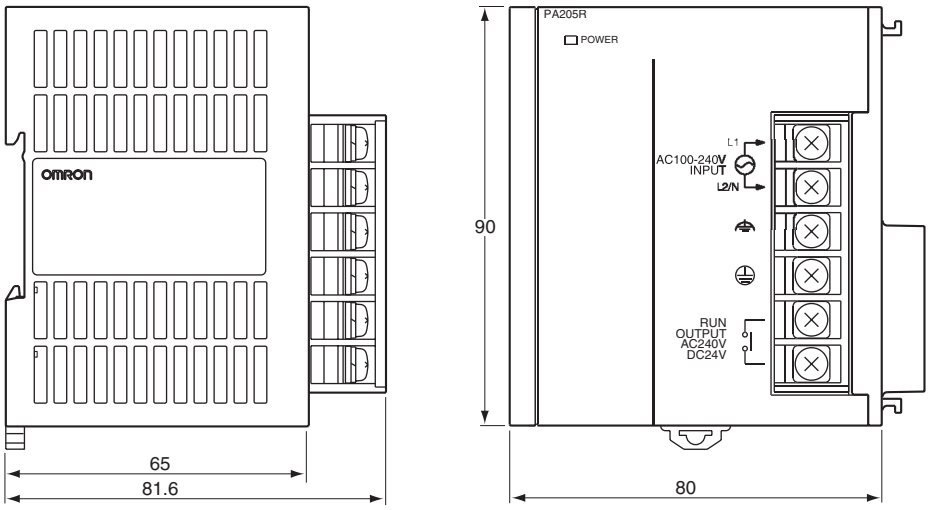
LG Ground to a resistance of 100 Ω or less to increase noise resistance and avoid electric shock.

GR Ground to a resistance of 100 Ω or less to avoid electric shock.

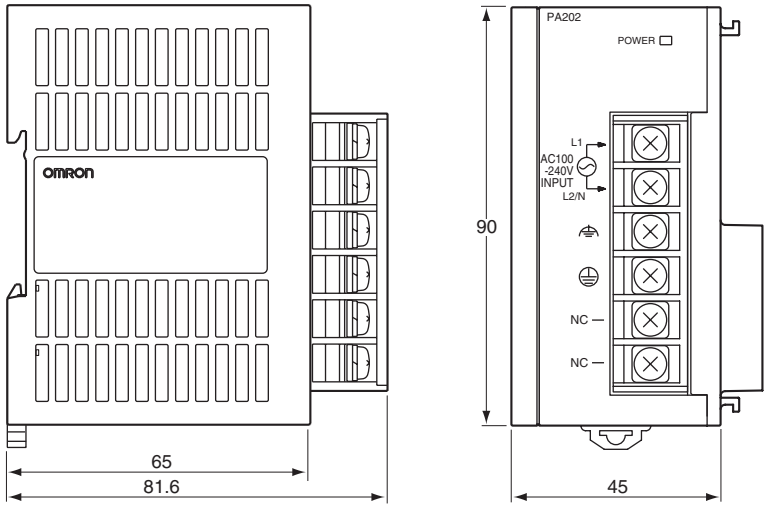
RUN Output (CJ1W-PA205R Only) The internal contact turns ON when the CPU Unit is operating (RUN or MONITOR mode). The Power Supply Unit must be in the CPU Rack to use this output.

3-4-3 Dimensions

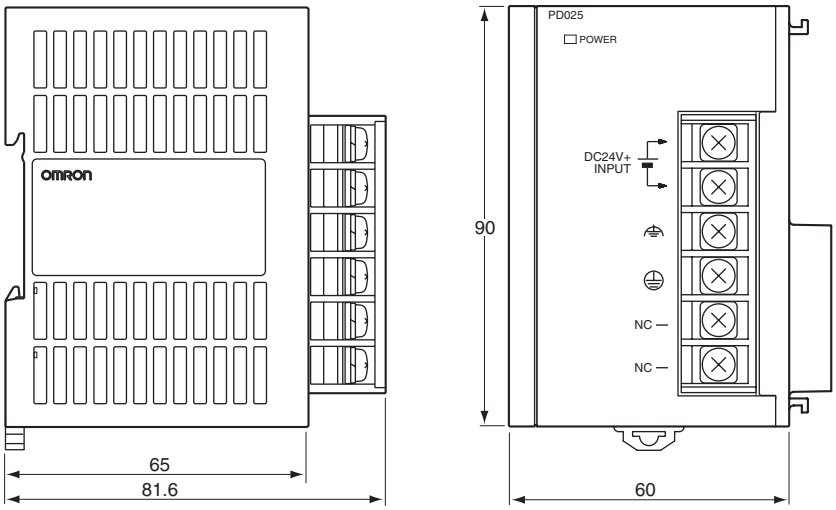
CJ1W-PA205R



CJ1W-PA202



CJ1W-PD025



3-4-4 Power Supply Confirmation

After determining what power supply voltage is required, calculate the current and power requirements for each Rack.

Condition 1: Current Requirements

There are two voltage groups for internal power consumption: 5 V DC and 24 V DC.

Current Consumption at 5 V DC (Internal Logic Power Supply)

The following table shows the current that can be supplied to Units (including the CPU Unit) that use 5-V DC power.

Power Supply Unit	Maximum current at 5 V DC
CJ1W-PA205R	5.0 A
CJ1W-PA202	2.8 A
CJ1W-PA025	5.0 A

Current Consumption at 24 V DC (Relay Driving Power Supply)

The following table shows the current that can be supplied to Units that use 24-V DC power.

Power Supply Unit	Maximum current at 24 V DC
CJ1W-PA205R	0.8 A
CJ1W-PA202	0.4 A
CJ1W-PA025	0.8 A

Condition 2: Power Requirements

The following table shows the maximum total power that can be supplied at 5 V DC and 24 V DC.

Power Supply Unit	Maximum total power output
CJ1W-PA205R	25 W
CJ1W-PA202	14 W
CJ1W-PA025	25 W

Refer to *2-6 Unit Current Consumption* for tables showing the current consumed by each particular Unit as well as example calculations.

3-5 I/O Control Units and I/O Interface Units

An I/O Control Unit and I/O Interface Units are used to connect Expansion Racks to expand the system.

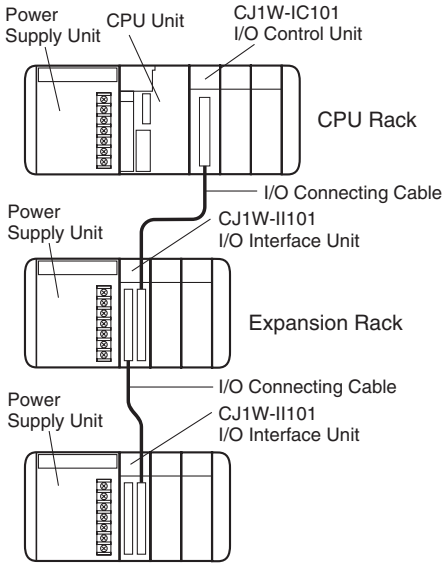
3-5-1 Models

Name	Model number	Number required	Weight
I/O Control Unit	CJ1W-IC101	1 on the CPU Rack	70 g max.
I/O Interface Unit	CJ1W-II101	1 on each Expansion Rack	130 g max. (including End Cover)

3-5-2 System Configuration

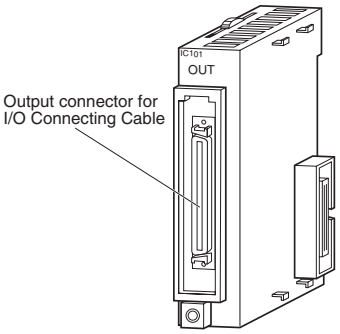
The I/O Control Unit is connected directly to the CPU Unit. If it is not immediately to the right of the CPU Unit, correct operation may not be possible.

The I/O Interface Unit is connected directly to the Power Supply Unit. If it is not immediately to the right of the Power Supply Unit, correct operation may not be possible.

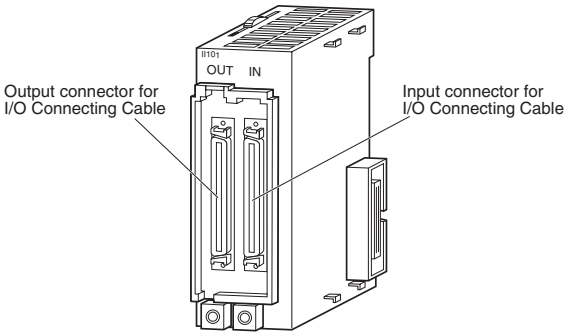


3-5-3 Component Names

CJ1W-IC101 I/O Control Unit

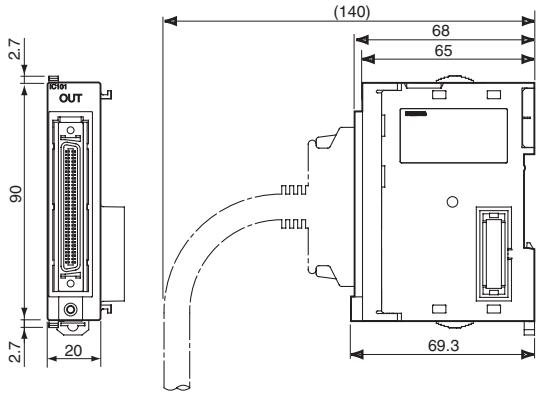


CJ1W-II101 I/O Interface Unit

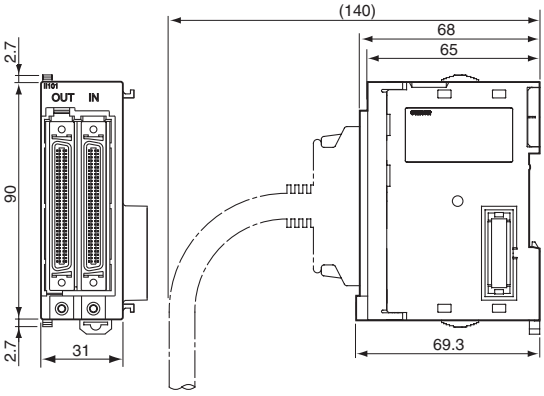


3-5-4 Dimensions

CJ1W-IC101 I/O Control Unit



CJ1W-II101 I/O Interface Unit



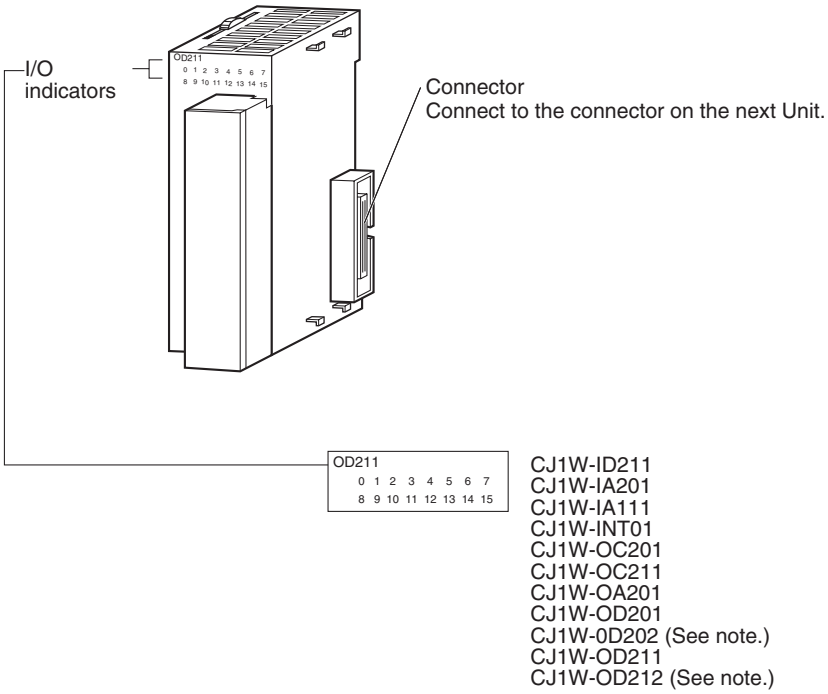
Note Attached the enclosed cover to the I/O Connecting Cable connector on the I/O Interface Unit when it is not being used to protect it from dust.

3-6 CJ-series Basic I/O Units

3-6-1 CJ-series Basic I/O Units with Terminal Blocks

Classification	Name	Specifications	Number of bits allocated	Model	Page
Basic Input Unit with Terminal Block	DC Input Units	24 V DC	16	CJ1W-ID211	358
	AC Input Units	200 to 240 VDC	8	CJ1W-IA201	366
		100 to 120 VDC	16	CJ1W-IA111	367
	Interrupt Input Unit	24 VDC	16	CJ1W-INT01	368
Basic Output Units with Terminal Blocks	Relay Output Units	250 V AC/24 V DC, 2 A; 8 independent contacts	8	CJ1W-OC201	369
		250 V AC/24 V DC, 2 A; 16 outputs	16	CJ1W-OC211	370
	Triac Output Unit	250 V AC, 0.5 A	8	CJ1W-OA201	371
	Transistor Output Unit with Sinking Outputs	12 to 24 V DC, 2.0 A	8	CJ1W-OD201	372
		12 to 24 V DC, 0.5 A	16	CJ1W-OD211	373
	Transistor Output Unit with Sourcing Outputs	24 V DC, 2 A, 8 outputs, load short-circuit protection and line disconnection detection	8	CJ1W-OD202	380
		24 V DC, 0.5 A, 16 outputs, load short-circuit protection	16	CJ1W-OD212	381

Part Names of Units with 18-point Terminal Blocks

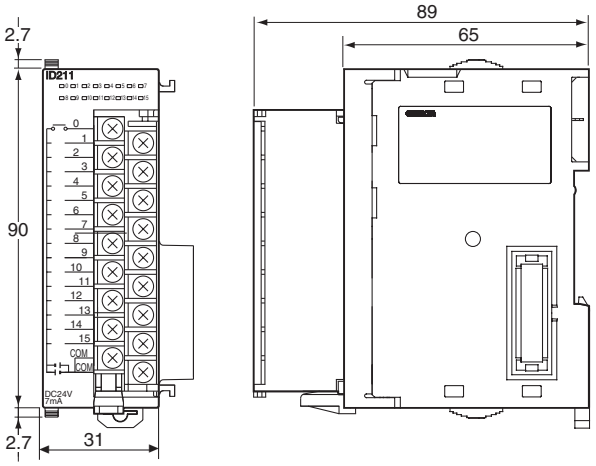


CJ1W-ID211
CJ1W-IA201
CJ1W-IA111
CJ1W-INT01
CJ1W-OC201
CJ1W-OC211
CJ1W-OA201
CJ1W-OD201
CJ1W-0D202 (See note.)
CJ1W-OD211
CJ1W-OD212 (See note.)

Note The CJ1W-OD202 and CJ1W-OD212 also have an ERR indicator for the load short-circuit alarm.

Dimensions of Units with 18-point Terminal Blocks

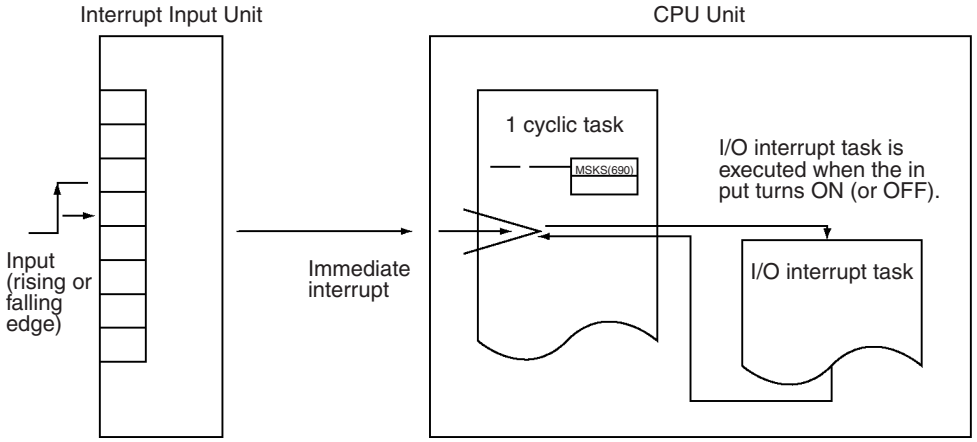
CJ1W-ID211
CJ1W-IA201
CJ1W-IA111
CJ1W-INT01
CJ1W-OC201
CJ1W-OC211
CJ1W-OA201
CJ1W-OD201
CJ1W-OD211
CJ1W-OD202
CJ1W-OD212



Interrupt Input Units

Functions

Interrupt Input Units are used to execute interrupt programs on the rising or falling edge of an input signal. When the specified interrupt input turns ON (or OFF), execution of the cyclic program in the CPU Unit is interrupted and an I/O interrupt task (task number 100 to 131) is executed. When execution of the I/O interrupt task has been completed, the cyclic program is again executed starting from the instruction after which it was interrupted.



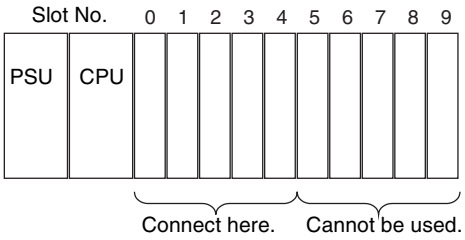
Applicable Units

Either of the following Interrupt Input Units can be used with a CJ1-H CPU Unit. (CJ1 CPU Units do not support interrupt inputs.)

Model	Specifications	No. of Units mountable to CPU Rack	Page
CJ1W-INT01	24 VDC 16 inputs	2 max.	368

Application Precautions

All Interrupt Input Units must be connected in the CPU Rack and it must be connected in one of the 5 positions immediately to the right of the CPU Unit. The interrupt input function will not be supported if an Interrupt Input Unit is mounted to an Expansion Rack. If connected in any other position or to an Expansion Rack, and I/O setting error (fatal) will occur.



If the Interrupt Input Units are not connected in the correct positions, an error will occur when the I/O tables are generated from the CX-Programmer. A40110 will turn ON to indicate an I/O setting error and A40508 will turn ON to indicate that an Interrupt Input Unit is in the wrong position.

Note Even if a Unit is physically in one of the first 5 positions, a Dummy Unit can be registered in the I/O table, causing a Unit to be defined in a position different from its physical position.

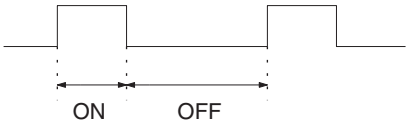
There are limits to the number of Interrupt Input Units that can be mounted. (See table, above.)

The input response time cannot be changed for the CJ1W-INT01, and the related portions of the Basic I/O Unit input time constants in the PC Setup, and the setting status in A220 to A259 will not be valid.

Use CX-Programmer Version 2.0 or later when using the CJ1W-INT01 Interrupt Input Unit. Earlier versions of CX-Programmer do not support this Unit.

Input Signal Width

Input signals must meet the following conditions.



Unit	ON time	OFF time
CJ1W-INT01	0.05 ms min.	0.5 ms min.

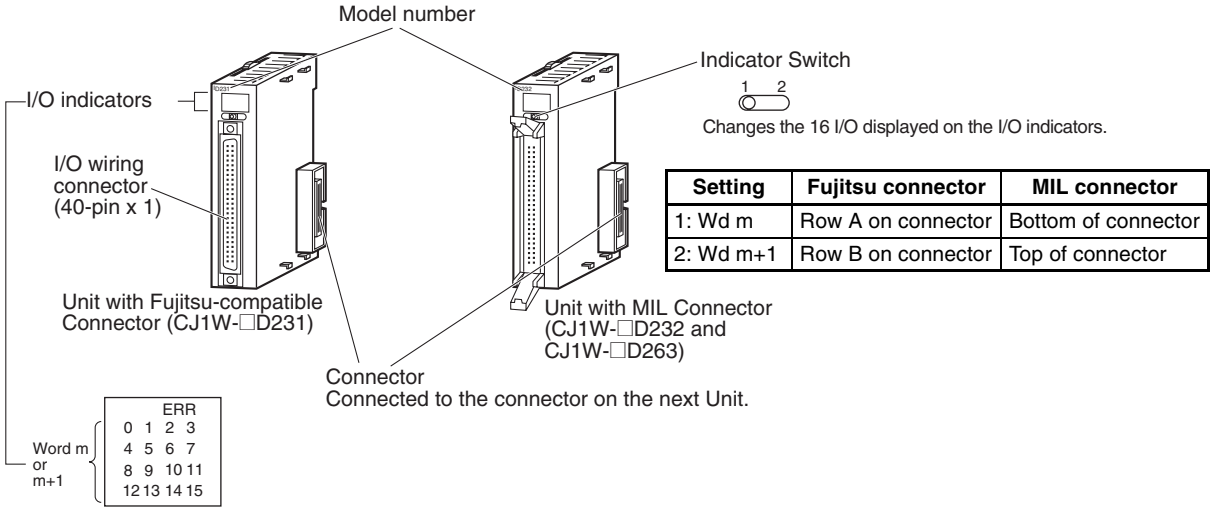
3-6-2 CJ-series 32/64-point Basic I/O Units with Connectors

Units are available with either Fujitsu-compatible connectors (CJ1W-□D□□1) or MIL connectors (CJ1W-□D□□2/3).

Name	Specifications	Model	Number of bits allocated	Page
DC Input Units	Fujitsu-compatible connector 24 V DC, 32 inputs	CJ1W-ID231	32	359
	Fujitsu-compatible connector 24 V DC, 64 inputs	CJ1W-ID261	64	363
	MIL connector 24 V DC, 32 inputs	CJ1W-ID232	32	361
	MIL connector 24 V DC, 64 inputs	CJ1W-ID262	64	364
Transistor Output Units with Sinking Outputs	Fujitsu-compatible connector 12 to 24 V DC, 0.5 A, 32 outputs	CJ1W-OD231	32	374
	Fujitsu-compatible connector 12 to 24 V DC, 0.3 A, 64 outputs	CJ1W-OD261	64	377
	MIL connector 12 to 24 V DC, 0.5 A, 32 outputs	CJ1W-OD233	32	376
	MIL connector 12 to 24 V DC, 0.3 A, 64 outputs	CJ1W-OD263	64	378
Transistor Output Units with Sourcing Outputs	MIL connector 24 V DC, 0.5 A, 32 outputs, load short-circuit protection	CJ1W-OD232	32	382

Part Names

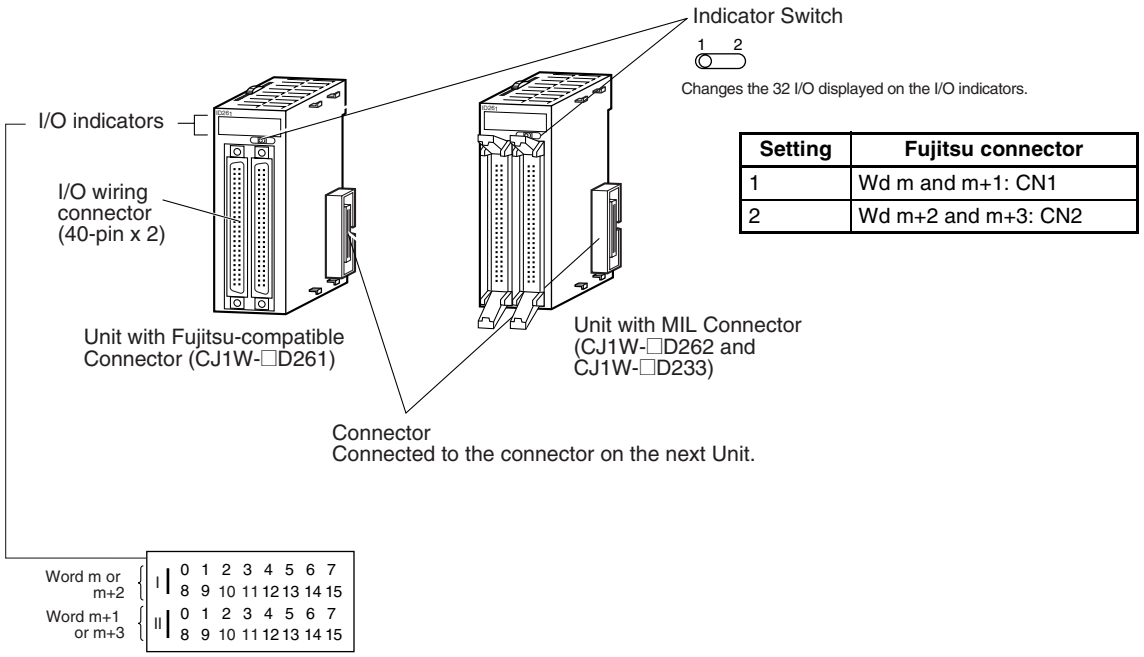
32-point Units (CJ1W-□D23□)



Setting	Fujitsu connector	MIL connector
1: Wd m	Row A on connector	Bottom of connector
2: Wd m+1	Row B on connector	Top of connector

Note: Only the CJ1W-OD232 has an ERR indicator for the load short-circuit alarm.

64-point Units (CJ1W-□D26□)



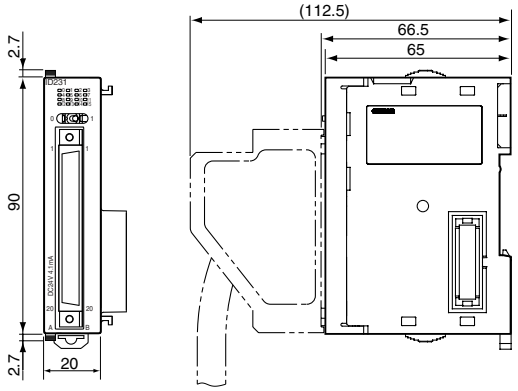
Setting	Fujitsu connector
1	Wd m and m+1: CN1
2	Wd m+2 and m+3: CN2

Dimensions

32-point Units (40-pin x 1)

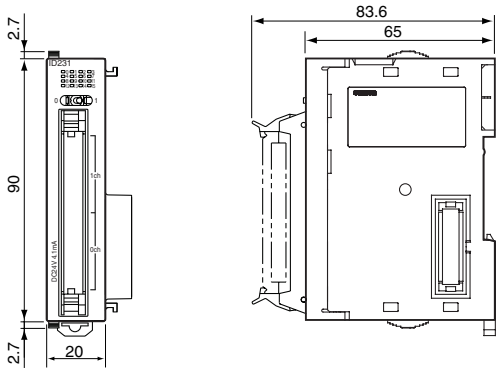
■ **Units with Fujitsu-compatible Connector**

CJ1W-ID231 (32-point Input Unit)
CJ1W-OD231 (32-point Output Unit)



■ **Units with MIL Connector**

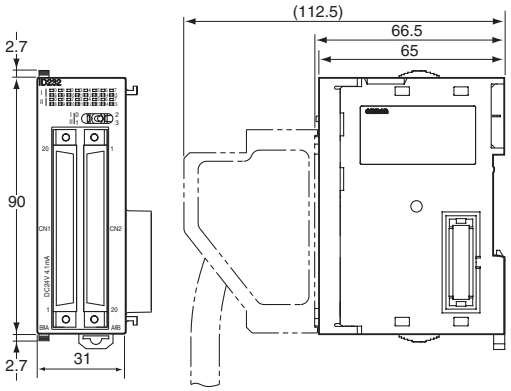
CJ1W-ID232 (32-point Input Unit)
CJ1W-OD232(32-point Output Unit)
CJ1W-OD233 (32-point Output Unit)



64-point Units (40-pin x 2)

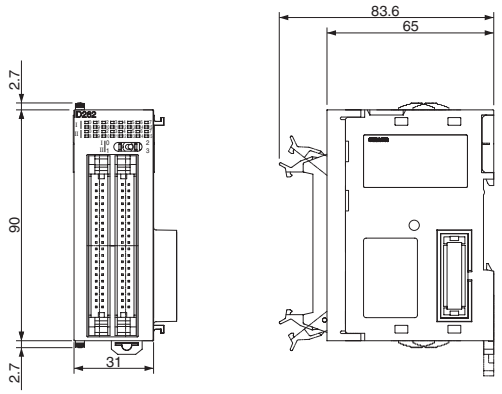
■ **Units with Fujitsu-compatible Connector**

CJ1W-ID261 (64-point Input Unit)
CJ1W-OD261 (64-point Output Unit)



■ **Units with MIL Connector**

CJ1W-ID262 (64-point Input Unit)
CJ1W-OD263 (64-point Output Unit)



Connecting to Connector-Terminal Block Units

The CJ-series 32/64-point Basic I/O Units can be connected to Connector-Terminal Block Conversion Units as shown in the following table.

Units with Fujitsu-compatible Connectors

Basic I/O Unit		Connecting Cable	Connector-Terminal Block Conversion Unit		Required for connection
Model number	Specifications		Model number	Specifications	
CJ1W-ID231	32-point 24-V DC Input Unit	XW2Z-□□□B	XW2B-40G5	Standard, M3.5 screw terminal block	1 Connecting Cable and 1 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
			XW2D-40G6-RF	Slim, M3 screw terminal block, built-in breeder resistor	
		XW2Z-□□□D	XW2C-20G5-IN16	16-point input common, M3.5 screw terminal block	1 Connecting Cable and 2 Conversion Units
CJ1W-ID261	64-point 24-V DC Input Unit	XW2Z-□□□B	XW2B-40G5	Standard, M3.5 screw terminal block	2 Connecting Cables and 2 Conversion Units
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
			XW2D-40G6-RF	Slim, M3 screw terminal block, built-in breeder resistor	
		XW2Z-□□□D	XW2C-20G5-IN16	16-point input common, M3.5 screw terminal block	2 Connecting Cables and 4 Conversion Units
CJ1W-OD231	32-point Transistor Output Unit with Sinking Outputs	XW2Z-□□□B	XW2B-40G5	Standard, M3.5 screw terminal block	1 Connecting Cable and 1 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
CJ1W-OD261	64-point Transistor Output Unit with Sinking Outputs	XW2Z-□□□B	XW2B-40G5	Standard, M3.5 screw terminal block	2 Connecting Cables and 2 Conversion Units
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	

Units with MIL Connectors

Basic I/O Unit		Connecting Cable	Connector-Terminal Block Conversion Unit		Required for connection
Model number	Specifications		Model number	Specifications	
CJ1W-ID232	32-point 24-V DC Input Unit	XW2Z-□□□K	XW2B-40G5	Standard, M3.5 screw terminal block	1 Connecting Cable and 1 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
			XW2D-40G6-RM	Slim, M3 screw terminal block, built-in breeder resistor	
		XW2Z-□□□N	XW2C-20G5-IN16	16-point input common, M3.5 screw terminal block	1 Connecting Cable and 2 Conversion Units
			XW2D-20G6-IO16	Slim, M3 screw terminal block, built-in breeder resistor	
CJ1W-ID262	64-point 24-V DC Input Unit	XW2Z-□□□K	XW2B-40G5	Standard, M3.5 screw terminal block	2 Connecting Cable and 2 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
			XW2D-40G6-RM	Slim, M3 screw terminal block, built-in breeder resistor	
		XW2Z-□□□N	XW2C-20G5-IN16	16-point input common, M3.5 screw terminal block	2 Connecting Cable and 4 Conversion Units
			XW2D-20G6-IO16	Slim, M3 screw terminal block	
CJ1W-OD232	32-point Transistor Output Unit, Sourcing	XW2Z-□□□K	XW2B-40G5	Standard, M3.5 screw terminal block	1 Connecting Cable and 1 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
		XW2Z-□□□N	XW2D-20G6-IO16	Slim, M3 screw terminal block	1 Connecting Cable and 2 Conversion Units
CJ1W-OD233	32-point Transistor Output Unit, Sourcing	XW2Z-□□□K	XW2B-40G5	Standard, M3.5 screw terminal block	1 Connecting Cable and 1 Conversion Unit
			XW2B-40G6	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
		XW2Z-□□□N	XW2D-20G6-IO16	Slim, M3 screw terminal block	1 Connecting Cable and 2 Conversion Units
CJ1W-OD263	64-point Transistor Output Unit, Sinking	XW2Z-□□□K	XW2B-40G5	Standard, M3.5 screw terminal block	2 Connecting Cable and 2 Conversion Unit
			XW2B-40G4	Standard, M3 screw terminal block	
			XW2D-40G6	Slim, M3 screw terminal block	
		XW2Z-□□□N	XW2D-20G6-IO16	Slim, M3 screw terminal block	2 Connecting Cable and 4 Conversion Units

Connecting to I/O Terminals

The CJ-series 32/64-point Basic I/O Units can be connected to I/O Terminals as shown in the following table.

Units with Fujitsu-compatible Connectors

Basic I/O Unit		Connecting Cable	I/O Terminal			Required for connection
Model number	Specifications		Model number	Type	Input voltage/ output type	
CJ1W-ID231	32-point 24-V DC Input Unit	G79-I□C-□	G7TC-ID16	Input Block	Input: 24 V DC Output: Relay	1 Connecting Cable and 2 I/O Terminals
			G7TC-IA16		Input: 100/ 200 V AC Output: Relay	
CJ1W-ID261	64-point 24-V DC Input Unit	G79-I□C-□	G7TC-ID16		Input: 24 V DC Output: Relay	2 Connecting Cables and 4 I/O Terminals
			G7TC-IA16		Input: 100/ 200 V AC Output: Relay	

Basic I/O Unit		Connecting Cable	I/O Terminal			Required for connection
Model number	Specifications		Model number	Type	Input voltage/ output type	
CJ1W-OD231	32-point Transistor Output Unit with Sinking Outputs	G79-O□C-□	G7TC-OC16	Output Block	Input: 24 V DC Output: Relay	1 Connecting Cable and 2 I/O Terminals
			G70D-SOC16	Output Terminal, Slim	Input: 24 V DC Output: Relay	
			G70D-FOM16	Output Terminal	Input: 24 V DC Output: MOS FET	
			G70A-ZOC16-3 + Relays	Relay Terminal Socket (NPN) + Relays	---	
CJ1W-OD261	64-point Transistor Output Unit with Sinking Outputs	G79-O□C-□	G7TC-OC16	Output Block	Input: 24 V DC Output: Relay	2 Connecting Cables and 4 I/O Terminals
			G70D-SOC16	Output Terminal, Slim	Input: 24 V DC Output: Relay	
			G70D-FOM16	Output Terminal	Input: 24 V DC Output: MOS FET	
			G70A-ZOC16-3 + Relays	Relay Terminal Socket + Relays	---	

Units with MIL Connectors

Basic I/O Unit		Connecting Cable	I/O Terminal			Required for connection
Model number	Specifications		Model number	Type	Input voltage/ output type	
CJ1W-ID232	32-point 24-V DC Input Unit	G79-I□-□-DI	G7TC-ID16	Input Block	Input: 24 V DC Output: Relay	1 Connecting Cable and 2 I/O Terminals
			G7TC-IA16		Input: 100/ 200 V AC Output: Relay	
CJ1W-ID262	64-point 24-V DC Input Unit	G79-I□-□-DI	G7TC-ID16	Input Block	Input: 24 V DC Output: Relay	2 Connecting Cables and 4 I/O Terminals
			G7TC-IA16		Input: 100/ 200 V AC Output: Relay	
CJ1W-OD232	32-point Transistor Output Unit, Sourcing	G79-O□-□-DI	G70D-SOC16-1	Output Block	Input: 24 V DC Output: Relay	1 Connecting Cable and 2 I/O Terminals
			G70A-ZOC16-4 + Relays	Relay Terminal Socket (NPN) + Relays	---	
CJ1W-OD233	32-point Transistor Output Unit, Sinking	G79-O□-□-DI	G7TC-OC16	Output Block	Input: 24 V DC Output: Relay	1 Connecting Cable and 2 I/O Terminals
			G70D-SOC16 G70D-VSOC16	Output Block (Slim)	Input: 24 V DC Output: Relay	
			G70A-ZOC16-3 + Relays	Relay Terminal Socket (NPN) + Relays	---	
CJ1W-OD263	64-point Transistor Output Unit, Sinking	G79-O□-□-DI	G7TC-OC16	Output Block	Input: 24 V DC Output: Relay	2 Connecting Cables and 4 I/O Terminals
			G70D-SOC16 G70D-VSOC16	Output Block (Slim)	Input: 24 V DC Output: Relay	
			G70A-ZOC16-3 + Relays	Relay Terminal Socket (NPN) + Relays	---	

SECTION 4
Operating Procedures

This section outlines the steps required to assemble and operate a CJ-series PC system.

4-1 Introduction

The following procedure outlines the recommended steps to follow when preparing CJ-series PCs for operation.

1,2,3...

1. Installation

   Set the DIP switches on the front of each Unit as required.
   Connect the CPU Unit, Power Supply Unit, I/O Units, and End Cover. Install a Memory Card if required.

   See *5-2 Installation* for details.

2. Wiring

   Connect the power supply wiring, I/O wiring, and Programming Device (CX-Programmer or Programming Console). Connect communications wiring as required.

   See *5-3 Wiring* for details on power supply and I/O wiring.
   See *2-3 Basic System Configuration* for details on connecting Programming Devices.

3. Initial Settings (Hardware)

   Set the DIP switches and Rotary switches on the CPU Unit and other Units.

4. Checking Initial Operation

   a) Set the operating mode to PROGRAM mode and connect the Programming Console.

   b) Turn the power ON after checking the power supply wiring and voltage. Check the Power Supply Unit's POWER indicator and Programming Console's display.

5. Registering the I/O Tables (If Required.)

   Check the Units to verify that they are installed in the right slots. With the PC in PROGRAM mode, register the I/O tables from the CX-Programmer (online) or Programming Console. (Another method is to create the I/O tables in CX-Programmer (offline) and transfer them to the CPU Unit.)

   See *8-1 I/O Allocations* for details.

6. PC Setup Settings

   With the PC in PROGRAM mode, change the settings in the PC Setup as necessary from the CX-Programmer (online) or Programming Console. (Another method is to change the PC Setup in CX-Programmer (offline) and transfer it to the CPU Unit.)

7. DM Area Settings

   a) Use a Programming Device (CX-Programmer or Programming Console) to make any necessary settings in the parts of the DM Area that are allocated to Special I/O Units and CPU Bus Units.

   b) Reset the power (ON → OFF → ON) or toggle the Restart Bit for each Unit. See the Unit's operation manual for details.

8. Writing the Program

   Write the program with a Programming Device (CX-Programmer or Programming Console).

9. Transferring the Program (CX-Programmer Only)

   With the PC in PROGRAM mode, transfer the program from CX-Programmer to the CPU Unit.

10. Testing Operation

a) Checking I/O Wiring

Output wiring	With the PC in PROGRAM mode, force-set output bits and check the status of the corresponding outputs.
Input wiring	Activate sensors and switches and either check the status of the indicators on the Input Unit or check the status of the corresponding input bits with the Programming Device's Bit/Word Monitor operation.

b) Auxiliary Area Settings (As Required)
Check operation of special Auxiliary Area Settings such as the following:

Output OFF Bit	When necessary, turn ON the Output OFF Bit (A50015) from the program and test operation with the outputs forced OFF.
Hot Start Settings	When you want to start operation (switch to RUN mode) without changing the contents of I/O memory, turn ON the IOM Hold Bit (A50012).

c) Trial Operation
Test PC operation by switching the PC to MONITOR mode.

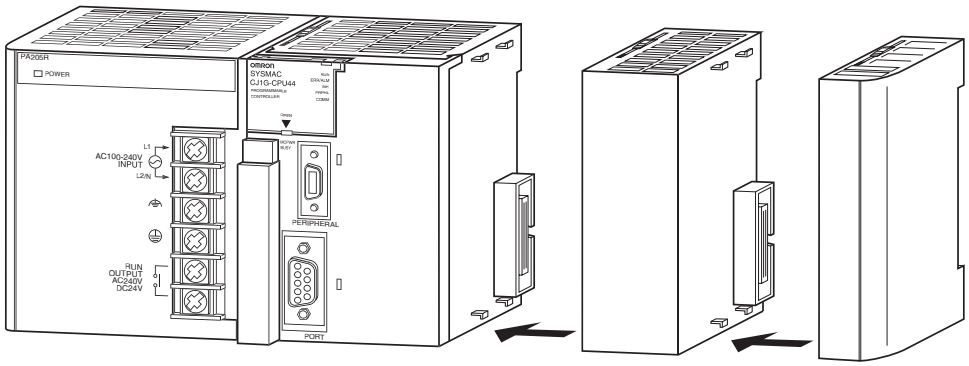
d) Monitoring and Debugging
Monitor operation from the Programming Device. Use functions such as force-setting/force-resetting bits, tracing, and online editing to debug the program.

11. Saving and Printing the Program
12. Running the Program
    Switch the PC to RUN mode to run the program.

4-2 Examples

1. Installation

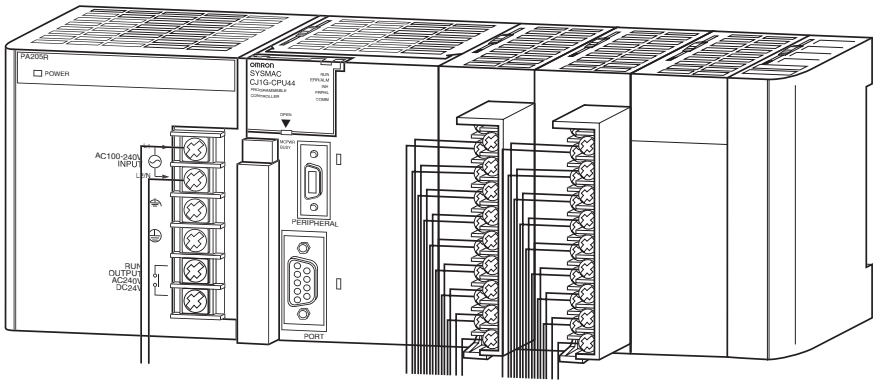
Connect the Units. When necessary, install a Memory Card.



Make sure that the total power consumption of the Units is less than the maximum capacity of the Power Supply Unit.

2. Wiring

Connect the power supply and I/O wiring.

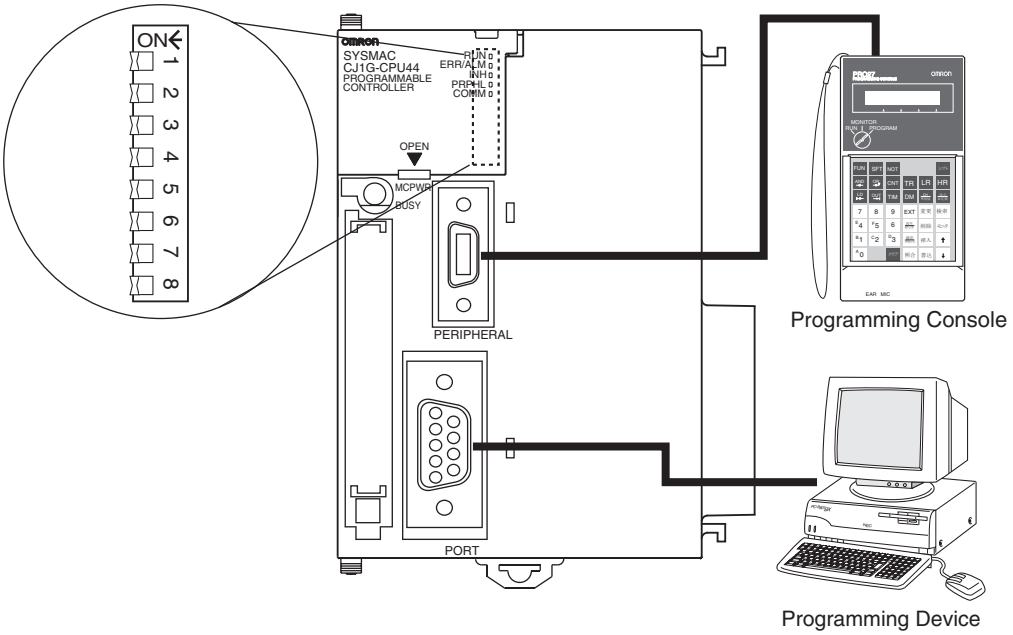


3. Initial Settings (Hardware)

Make necessary hardware settings such as the DIP switch settings on the CPU Unit. In particular, be sure that the settings for the peripheral port and RS-232C port are correct.

In the following example, a Programming Console is connected to the peripheral port so pin 4 is turned OFF. A Programming Device other than a Programming Console is connected to the RS-232C port, so pin 5 is turned ON.

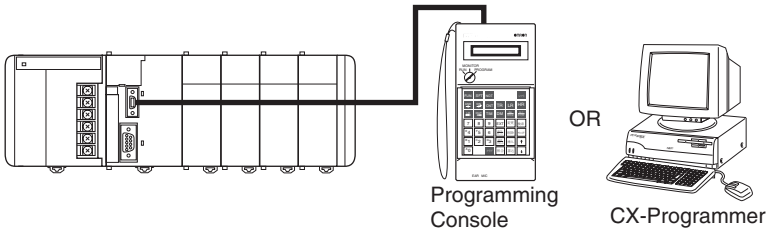
Note When devices other than a Programming Console and Programming Device are connected to the peripheral port and RS-232C port, turn ON pin 4 and turn OFF pin 5.



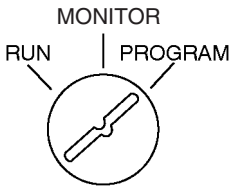
4. Checking Initial Operation

Use the following procedure to turn ON the PC and check initial operation using a Programming Console.

1,2,3... 1. Connect the Programming Console to the CPU Unit's peripheral port (the upper port).



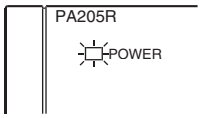
2. Set the Programming Console's Mode Switch to PROGRAM mode.



3. Check the power supply wiring and voltage and turn on the power.

   Note If power is turned ON with a new CPU Unit without connecting a Programming Console, the CPU Unit will attempt to enter RUN mode (the default setting), but an error will occur because there is no program.

4. Check that the Power Supply Unit's POWER indicator is lit.



5. Check that the Programming Console has the following display.

6. Press the password (the Clear and Monitor Keys) and check that the Programming Console has the following display.

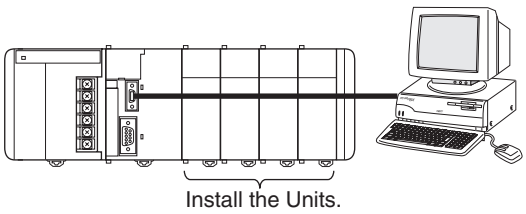
5. Registering the I/O Tables (If Required)

Registering the I/O tables allocates I/O memory to the Units actually installed in the PC. It is not necessary to create I/O tables with CJ-series CPU Units because by default they will be automatically generated when the CPU Unit is started. I/O tables can be created by the user to detect mistakes in connected Units or to enable allocating unused words (such as is possible with CS-series CPU Units).

Note The user program and parameter area data in CJ1-H CPU Units is backed up in the built-in flash memory. The BKUP indicator will light on the front of the CPU Unit when the backup operation is in progress. Do not turn OFF the power supply to the CPU Unit when the BKUP indicator is lit. The data will not be backed up if power is turned OFF.

Using the CX-Programmer Online

Use the following procedure to register the I/O table with the CX-Programmer that is connected to the PC.



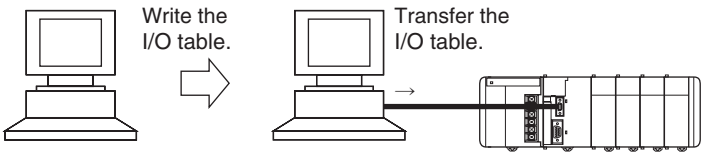
1,2,3...

1. Install all of the Units in the PC.
2. Connect the CX-Programmer to the peripheral port or RS-232C port. (The power must be OFF.)

   Note If the host computer is being connected to the RS-232C port, pin 5 of the CPU Unit's DIP switch must be set to ON.
3. Double-click ***I/O Table*** on the project tree in the main window. The I/O Table Window will be displayed.
4. Select ***Options*** and then ***Create***. The models and positions of Units mounted to the Racks will be written to the Registered I/O Table in the CPU Unit.

Using the CX-Programmer Offline

Use the following procedure to create the I/O table offline with the CX-Programmer and later transfer the I/O table from to the CPU Unit.



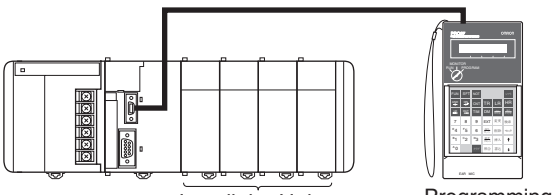
1,2,3...

1. Double-click ***I/O Table*** on the project tree in the main window. The I/O Table Window will be displayed.
2. Double-click the Rack to be edited. The slots for that Rack will be displayed.
3. Right-click the slots to be edited and select the desired Units from the pull-down menu.
4. Select ***Options*** and then ***Transfer to PLC*** to transfer the I/O table to the CPU Unit.

Note The first word allocated to each Rack can be set from the Programming Device.

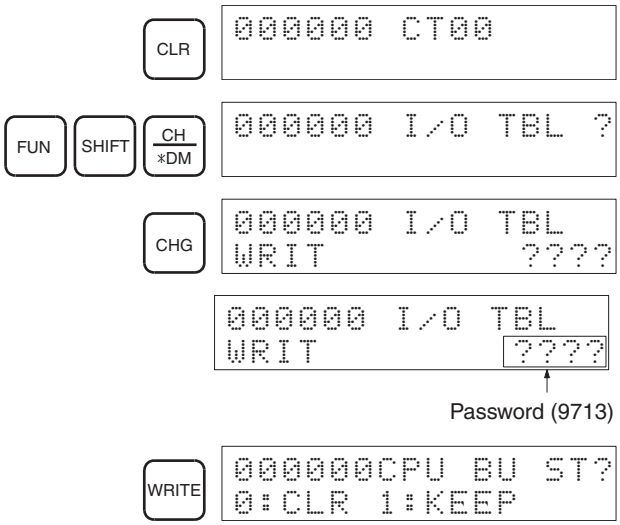
Using a Programming Console

Use the following procedure to register the I/O table with a Programming Console.



1,2,3...

1. Install all of the Units in the PC.
2. Connect the Programming Console to the peripheral port.
(It can be connected with the power on.)
3. Register the I/O table.



Specify holding or clearing CPU Bus Unit information.

```
000000 I/O TBL
WRIT OK
```

CLR

```
000000 CT00
```

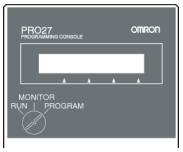
6. PC Setup Settings

These settings are the CPU Unit's software configuration.

The PC Setup settings are arranged by word addresses when a Programming Console is used to make PC Setup settings. This example shows a Programming Console used to make the following settings:

- Set a Minimum Cycle Time in 1-ms units.
- Set a Watch Cycle Time (maximum cycle time) in 10-ms units.

Setting with a Programming Console



Address	Bits	Setting	Setting range
208	0 to 15	Minimum cycle time setting	0001 to 7D00
209	15	Enable for Watch Cycle Time setting	0: Use default 1: Use setting in bits 0 to 14.
	0 to 14	Watch Cycle Time setting	0001 to 0FA0

Note When a host computer or PT is connected to the peripheral port or RS-232C port, the port must be set for Host Link or NT Link communications in the PC Setup. When a standard serial device is connected, the port must be set for no-protocol communications in the PC Setup.

CLR

```
000000 CT00
```

FUN VRFY

```
PC SETUP
0:MODE1:PC SETUP
```

1

```
PC SETUP
+000 0000
```

Specifying a word address in the PC Setup.
(Example: 209)

2 0 9

```
PC SETUP
 +209
```

↓ or ↑

```
PC SETUP
 +209  0000
```

CHG

```
PC SETUP?
 +209  0000 0000
```

Example: Input 8064.

8 0 6 4 WRITE

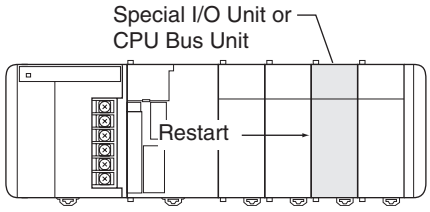
```
PC SETUP
 +209  8064
```

7. DM Area Settings

The following table shows the parts of the DM Area are allocated to Special I/O Units and CPU Bus Units for initial settings. The actual settings depend on the model of Unit being used.

Unit	Allocated words
Special I/O Units	D20000 to D29599 (100 words × 96 Units)
CPU Bus Units	D30000 to D31599 (100 words × 16 Units)

After writing the initial settings to the DM Area, be sure to restart the Units by turning the PC OFF and then ON again or toggling the Restart Bits for the affected Units.



8. Writing the Program

Write the program with a Programming Device (CX-Programmer or Programming Console).

The CJ-series PC's program can be divided into independently executable tasks. A single cyclic task can be written for program execution like earlier PCs or several cyclic tasks can be written for a more flexible and efficient program. The following table shows the differences when programming with CX-Programmer or a Programming Console.

Programming Device	Relationship between Tasks and Program	Writing a new program		Editing an existing program	
		Cyclic tasks	Interrupt tasks	Cyclic tasks	Interrupt tasks
Programming Console	Task = program (Cyclic task 0 is the main program)	Only one can be written. (Cyclic task 0)	Several can be written. (Interrupt tasks 1 to 3, 100 to 131)	All can be edited.	All can be edited.
CX-Programmer	Specify the type of task and task number for each program.	All can be written. (Cyclic tasks 0 to 31)	All can be written. (Interrupt tasks 0 to 255)	All can be edited.	All can be edited.

Note When writing the program with a Programming Console, specify whether there are interrupt tasks during the memory clear operation.

9. Transferring the Program

When the program has been created in the CX-Programmer, it must be transferred to the PC's CPU Unit.

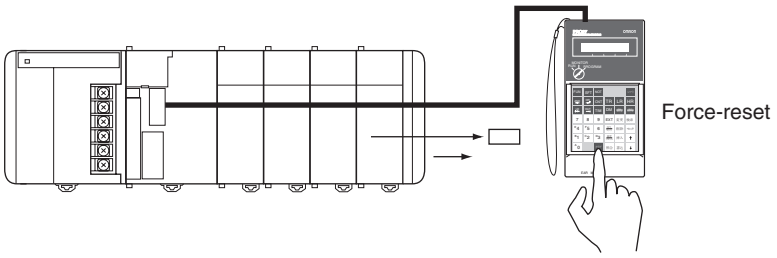
10. Testing Operation

Before performing a Trial Operation in MONITOR mode, check the I/O wiring.

10-a) I/O Wiring Checks

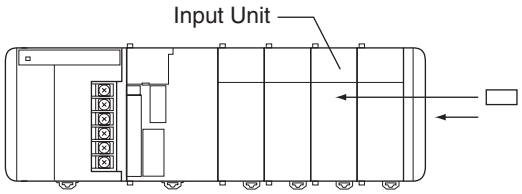
Check Output Wiring

With the PC in PROGRAM mode, force-set and force-reset output bits and verify that the corresponding outputs operate properly.



Check Input Wiring

Activate input devices such as sensors and switches and verify that the corresponding indicators on the Input Units light. Also, use the Bit/Word Monitor operation in the Programming Device to verify the operation of the corresponding input bits.

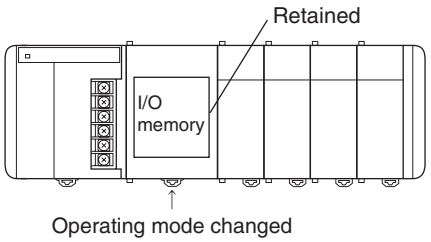


10-b) Auxiliary Area Settings

Make any required Auxiliary Area settings, such as the ones shown below. These settings can be made from a Programming Device (including a Programming Console or the CX-Programmer) or instructions in the program.

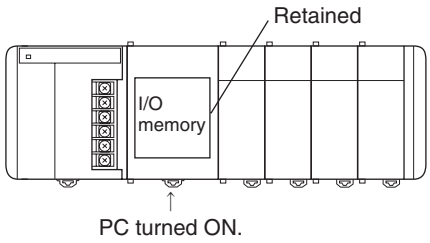
IOM Hold Bit (A50012)

Turning ON the IOM Hold Bit protects the contents of I/O memory (the CIO Area, Work Area, Timer Completion Flags and PVs, Index Registers, and Data Registers) that would otherwise be cleared when the operating mode is switched from PROGRAM mode to RUN/MONITOR mode or vice-versa.



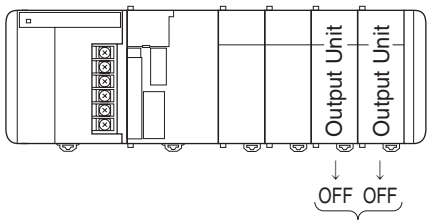
IOM Hold Bit Status at Startup

When the IOM Hold Bit has been turned ON and the PC Setup is set to protect the status of the IOM Hold BIt at startup (PC Setup address 80 bit 15 turned ON), the contents of I/O memory that would otherwise be cleared will be retained when the PC is turned on.



Output OFF Bit (A50015)

Turning ON the Output OFF Bit causes all outputs on Basic I/O Units and Special I/O Units to be turned OFF. The outputs will be turned OFF regardless of the PC's operating mode.

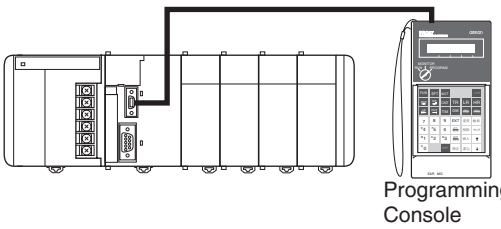


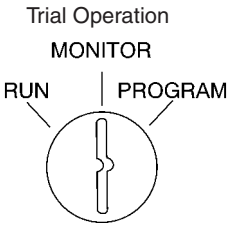
10-c) Trial Operation

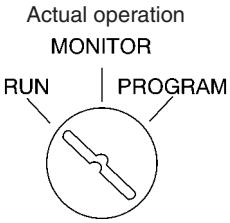
Use the Programming Console or Programming Device (CX-Programmer) to switch the CPU Unit to MONITOR mode.

Using a Programming Console

Turn the Mode Switch to MONITOR for the Trial Operation. (Turn the switch to RUN for full-scale PC operation.)

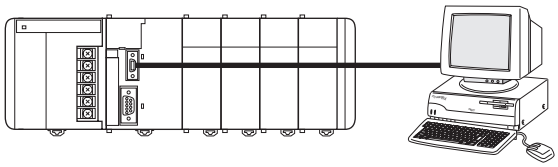






Using a Programming Console

The PC can be put into MONITOR mode with a host computer running CX-Programmer.



CX-Programmer

Trial Operation

Select ***PC, Mode, MONITOR.***

Actual operation

Select ***PC, Mode, RUN.***

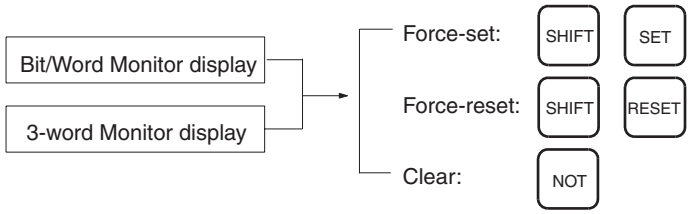
10-d) Monitoring and Debugging

There are several ways to monitor and debug PC operation, including the force-set and force-reset operations, differentiation monitoring, time chart monitoring, data tracing, and online editing.

Force-Set and Force-Reset

When necessary, the force-set and force-reset operations can be used to force the status of bits and check program execution.

When a Programming Console is being used, monitor the bits with Bit/Word Monitor or 3-word Monitor. Press the SHIFT+SET Keys to force-set a bit or press the SHIFT+RESET Keys to force-reset a bit. The forced status can be cleared by pressing the NOT Key.

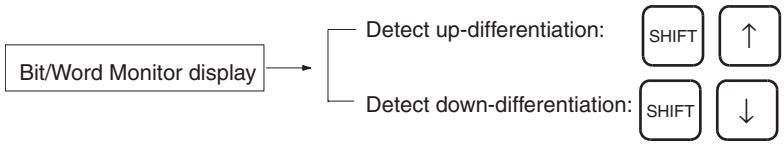


When CX-Programmer is being used, click the bit to be force-set or force-reset and then select ***Force On*** or ***Off*** from the PLC menu.

Differentiation Monitor

The differentiation monitor operation can be used to monitor the up or down differentiation of particular bits.

When a Programming Console is being used, monitor the bit with Bit/Word Monitor. Press the SHIFT+Up Arrow Keys to specify up differentiation or press the SHIFT+Down Arrow Keys to specify down differentiation.



When CX-Programmer is being used, follow the procedure shown below.

1,2,3...

1. Click the bit for differential monitoring.
2. Click ***Differential Monitor*** from the PLC Menu. The Differential Monitor Dialog Box will be displayed.
3. Click ***Rising*** or ***Falling.***
4. Click the **Start** button. The buzzer will sound when the specified change is detected and the count will be incremented.
5. Click the **Stop** button. Differential monitoring will stop.

Time Chart Monitoring

The CX-Programmer's time chart monitor operation can be used to check and debug program execution.

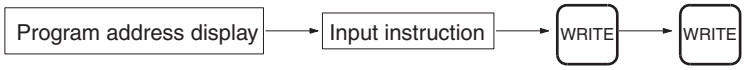
Data Tracing

The CX-Programmer's data trace operation can be used to check and debug program execution.

Online Editing

When a few lines of the program in the CPU Unit have to be modified, they can be edited online with the PC in MONITOR mode or PROGRAM mode from a Programming Console. When more extensive modifications are needed, upload the program from the CPU Unit to the CX-Programmer, make the necessary changes, and transfer the edited program back to the CPU Unit.

When a Programming Console is being used, display the desired program address, input the new instruction, and press the WRITE Key twice. A single program address (instruction) can be edited.



When CX-Programmer is being used, several instruction blocks can be edited.

16. Save and Print the Program

To save the program, select ***File*** and then ***Save*** (or ***Save As***) from the CX-Programmer menus.

To print the program, select ***File*** and then ***Print*** from the CX-Programmer menus.

17. Run the Program

Switch the PC to RUN mode to run the program.

SECTION 5
Installation and Wiring

This section describes how to install a PC System, including mounting the various Units and wiring the System. Be sure to follow the instructions carefully. Improper installation can cause the PC to malfunction, resulting in very dangerous situations.

5-1 Fail-safe Circuits

Be sure to set up safety circuits outside of the PC to prevent dangerous conditions in the event of errors in the PC or external power supply.

Supply Power to the PC before Outputs

If the PC's power supply is turned on after the controlled system's power supply, outputs in Units such as DC Output Units may malfunction momentarily. To prevent any malfunction, add an external circuit that prevents the power supply to the controlled system from going on before the power supply to the PC itself.

Managing PC Errors

When any of the following errors occurs, PC operation will stop and all outputs from Output Units will be turned OFF.

- Operation of the Power Supply Unit's overcurrent protection circuit
- A CPU error (watchdog timer error) or CPU on standby
- A fatal error* (memory error, I/O bus error, duplicate number error, too many I/O points error, program error, cycle time too long error, or FALS(007) error)

Be sure to add any circuits necessary outside of the PC to ensure the safety of the system in the event of an error that stops PC operation.

Note *When a fatal error occurs, all outputs from Output Units will be turned OFF even if the IOM Hold Bit has been turned ON to protect the contents of I/O memory. (When the IOM Hold Bit is ON, the outputs will retain their previous status after the PC has been switched from RUN/MONITOR mode to PROGRAM mode.)

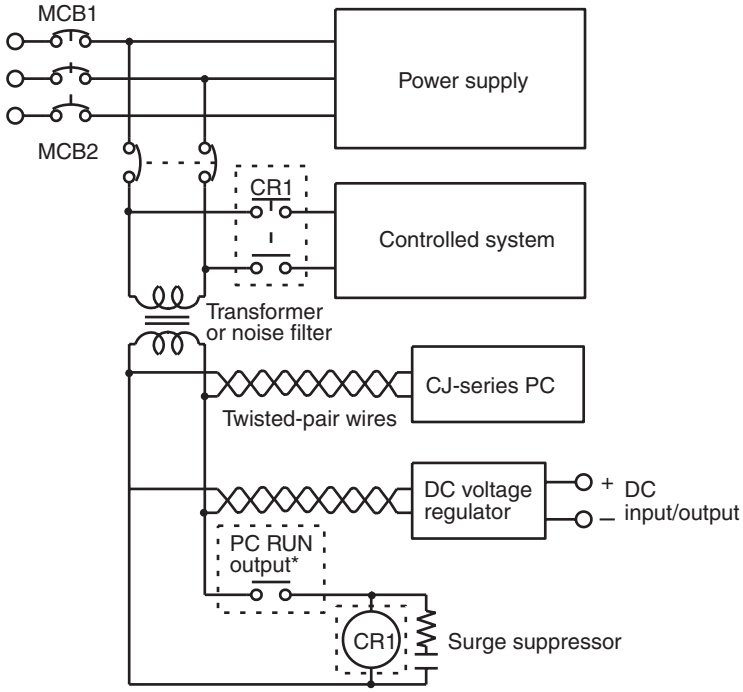
Managing Output Malfunctions

It is possible for an output to remain ON due to a malfunction in the internal circuitry of the Output Unit, such as a relay or transistor malfunction. Be sure to add any circuits necessary outside of the PC to ensure the safety of the system in the event that an output fails to go OFF.

Emergency Stop Circuit

The following emergency stop circuit controls the power supply to the controlled system so that power is supplied to the controlled system only when the PC is operating and the RUN output is ON.

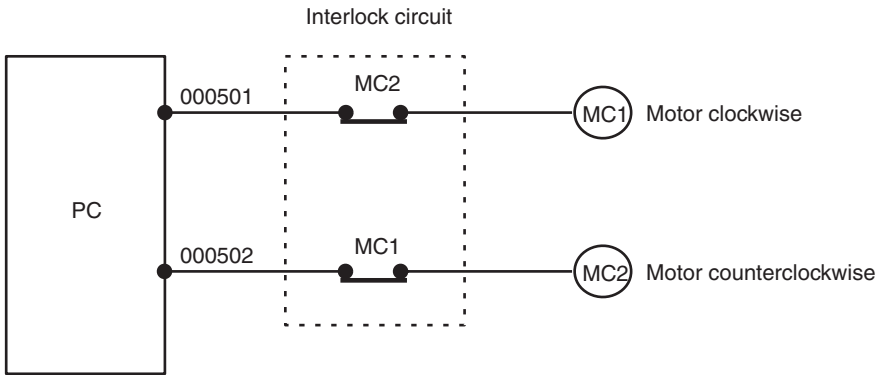
An external relay (CR1) is connected to the RUN output from the Power Supply Unit as shown in the following diagram.



Note When a Power Supply Unit without a RUN output is used, program the Always ON Flag (A1) as the execution condition for an output point from an Output Unit.

Interlock Circuits

When the PC controls an operation such as the clockwise and counterclockwise operation of a motor, provide an external interlock such as the one shown below to prevent both the forward and reverse outputs from turning ON at the same time.



This circuit prevents outputs MC1 and MC2 from both being ON at the same time even if both CIO 000500 and CIO 000501 are both ON, so the motor is protected even if the PC is programmed improperly or malfunctions.

5-2 Installation

5-2-1 Installation and Wiring Precautions

Be sure to consider the following factors when installing and wiring the PC to improve the reliability of the system and make the most of the PC's functions.

Ambient Conditions

Do not install the PC in any of the following locations.

- Locations subject to ambient temperatures lower than 0°C or higher than 55°C.
- Locations subject to drastic temperature changes or condensation.
- Locations subject to ambient humidity lower than 10% or higher than 90%.
- Locations subject to corrosive or flammable gases.
- Locations subject to excessive dust, salt, or metal filings.
- Locations that would subject the PC to direct shock or vibration.
- Locations exposed to direct sunlight.
- Locations that would subject the PC to water, oil, or chemical reagents.

Be sure to enclose or protect the PC sufficiently in the following locations.

- Locations subject to static electricity or other forms of noise.
- Locations subject to strong electromagnetic fields.
- Locations subject to possible exposure to radioactivity.
- Locations close to power lines.

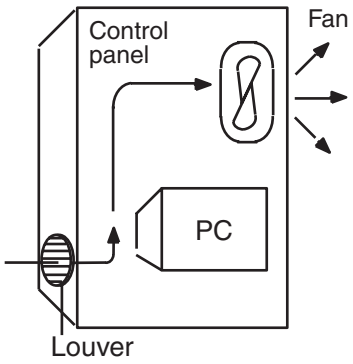
Installation in Cabinets or Control Panels

When the PC is being installed in a cabinet or control panel, be sure to provide proper ambient conditions as well as access for operation and maintenance.

Temperature Control

The ambient temperature within the enclosure must be within the operating range of 0°C to 55°C. When necessary, take the following steps to maintain the proper temperature.

- Provide enough space for good air flow.
- Do not install the PC above equipment that generates a large amount of heat such as heaters, transformers, or high-capacity resistors.
- If the ambient temperature exceeds 55°C, install a cooling fan or air conditioner.



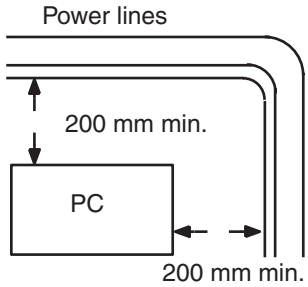
- If a Programming Console will be left on the PC, the ambient temperature must be within the Programming Console's operating range of 0°C to 45°C.

Accessibility for Operation and Maintenance

- To ensure safe access for operation and maintenance, separate the PC as much as possible from high-voltage equipment and moving machinery.
- The PC will be easiest to install and operate if it is mounted at a height of about 1.3 m (4 feet).

Improving Noise Resistance

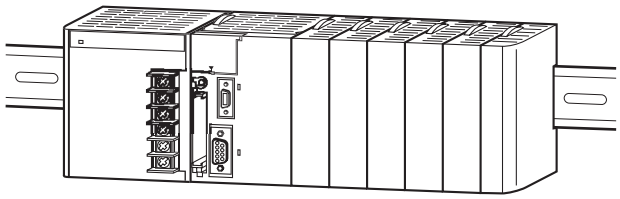
- Do not mount the PC in a control panel containing high-voltage equipment.
- Install the PC at least 200 mm (6.5 feet) from power lines.



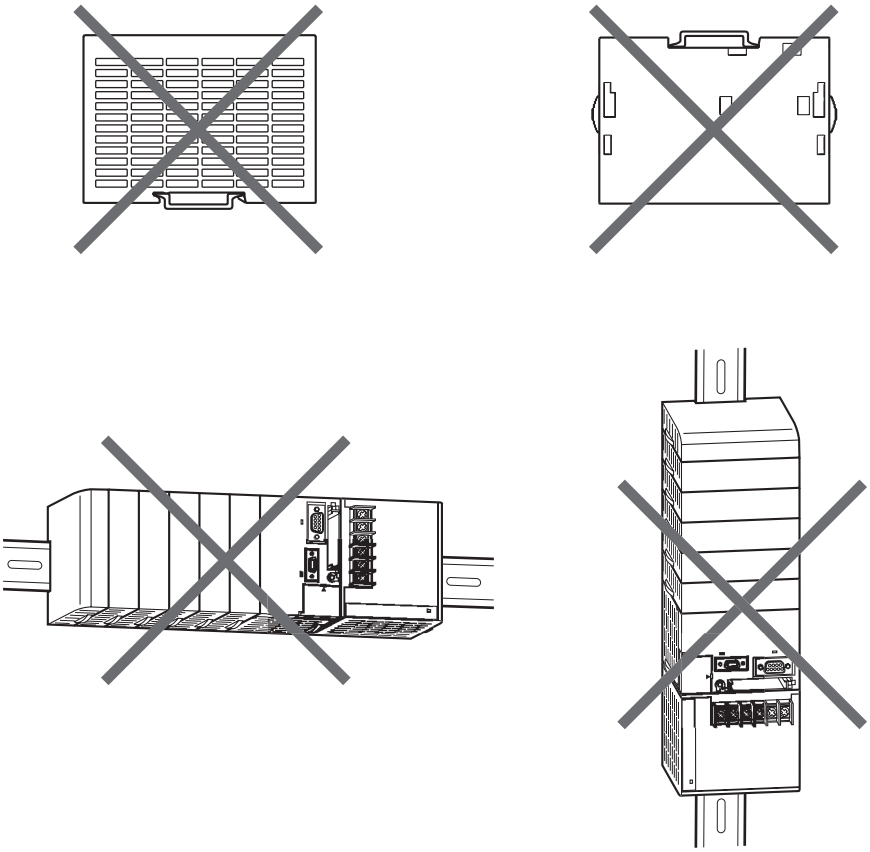
- Ground the mounting plate between the PC and the mounting surface.
- When I/O Connecting Cables are 10 m or longer, connect the control panels in which Racks are mounted with heavier power wires (3 wires at least 2 mm^2 in cross-sectional area).

PC Orientation

- Each Rack must be mounted in an upright position to provide proper cooling.



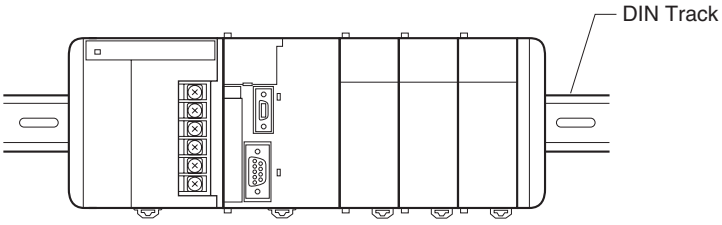
- Do not install a Rack in any of the following positions.



5-2-2 Installation in a Control Panel

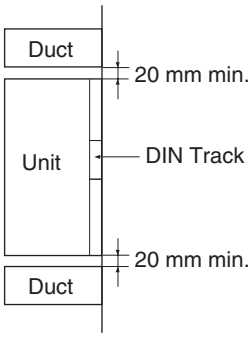
A CJ-series PC must be mounted inside a control panel on DIN Track. Normally the CPU Rack is installed on top and the Expansion Racks under it.

Note ACJ-series PC must be mounted on DIN Track. It cannot be mounted with screws.



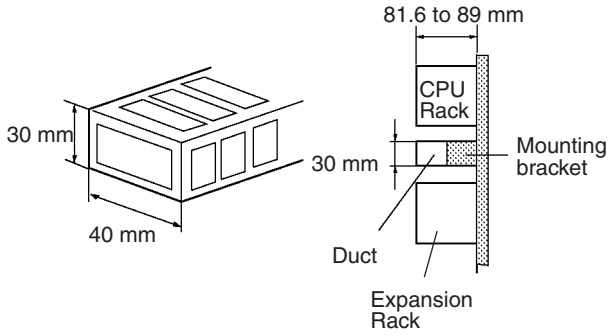
- Consider the width of wiring ducts, wiring, ventilation, and Unit replacement when determining the space between Racks.
- Up to 3 Expansion Racks can be connected.
  Each I/O Connecting Cable can be up to 12 m long, but the sum total of all cables between the CPU Rack and Expansion Racks must be 12 m or less.

- Whenever possible, route I/O wiring through wiring ducts or raceways. Install the duct so that it is easy to fish wire from the I/O Units through the duct. It is handy to have the duct at the same height as the Racks.



Wiring Ducts

The following example shows the proper installation of wiring duct.



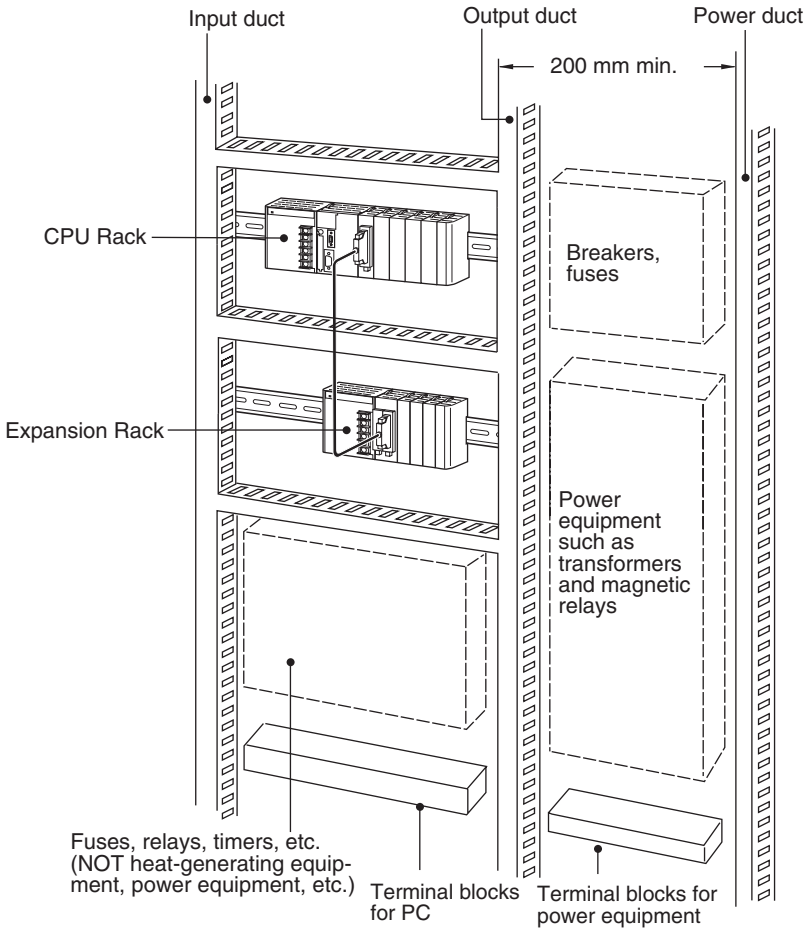
Note Tighten terminal block screws and cable screws to the following torques.

Terminal Screws
M3.5: 0.8 N • m
M3: 0.5 N • m

Cable Connector Screws
M2.6: 0.2 N • m

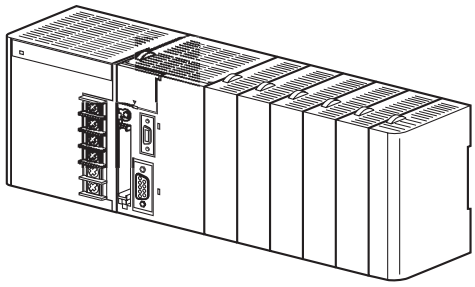
Routing Wiring Ducts

Install the wiring ducts at least 20 mm between the tops of the Racks and any other objects, (e.g., ceiling, wiring ducts, structural supports, devices, etc.) to provide enough space for air circulation and replacement of Units.

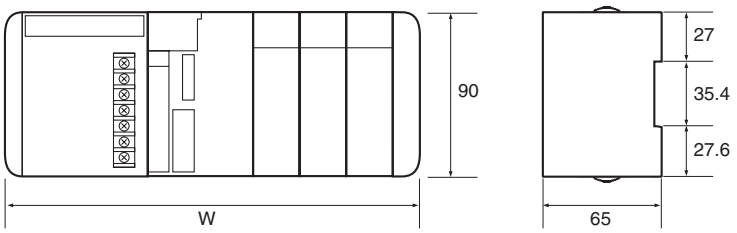


5-2-3 Assembled Appearance and Dimensions

The CJ-series Units, including the Power Supply Unit, the CPU Unit, and I/O Units, are connected to each other and an End Cover is connected to the right end.



Dimensions (Unit: mm)



The width the CJ-series Power Supply Unit depends on the model. The width the Power Supply Unit when computing the width of a Rack, is “a.”

Name	Model number	Specifications	Unit width
Power Supply Units	CJ1W-PA205R	100 to 240 V AC, 25 W	80
	CJ1W-PA202	100 to 240 V AC, 14 W	45
	CJ1W-PD025	100 to 240 V DC, 25 W	60

Other than the CPU Units and Power Supply Units, CJ-series Units come in two widths: 20 mm and 31 mm. When computing the width of a Rack, the number of 20-mm Units is “n.”

Name	Model number	Unit width
I/O Control Unit	CJ1W-IC101	20 mm
32-point Basic I/O Units	CJ1W-ID231/ID232 CJ1W-OD231/OD232	
CompoBus/S Master Unit	CJ1W-SRM21	

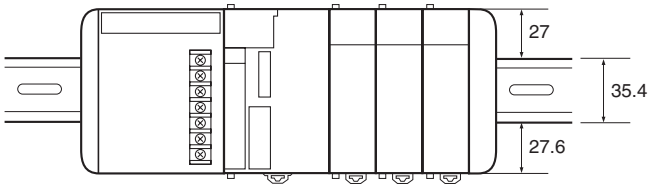
When computing the width of a Rack, the number of 30-mm Units is “m.”

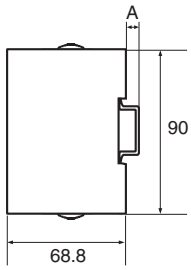
Name	Model number	Unit width
I/O Interface Unit	CJ1W-II101	31 mm
16-point Basic I/O Units	CJ1W-ID211 CJ1W-IA111/201 CJ1W-INT01 CJ1W-OD201/202/211/212 CJ1W-OC201/211 CJ1W-OA201	
64-point Basic I/O Units	CJ1W-ID261/262 CJ1W-OD261/263	
Analog I/O Units	CJ1W-AD081 (-V1) CJ1W-DA021/041	
Temperature Control Units	CJ1W-TC□□□	
Position Control Units	CJ1W-NC□□□	
High-speed Counter Unit	CJ1W-CT021	
DeviceNet Unit	CJ1W-DRM21	
Controller Link Unit	CJ1W-CLK21	
Serial Communications Unit	CJ1W-SCU41	
Ethernet Unit	CJ1W-ETN11	

W = a (Power Supply Unit) + 62 (CPU Unit) + 20 x n + 31 x m + 14.7 (End Cover) mm

Example: CJ1W-PA205R Power Supply Units, two 32-point Basic I/O Units and eight 31-mm Units.
W = 80 + 62 + 20 x 2 + 31 x 8 +14.7 = 444.7 mm

Installation Dimensions (Unit: mm)

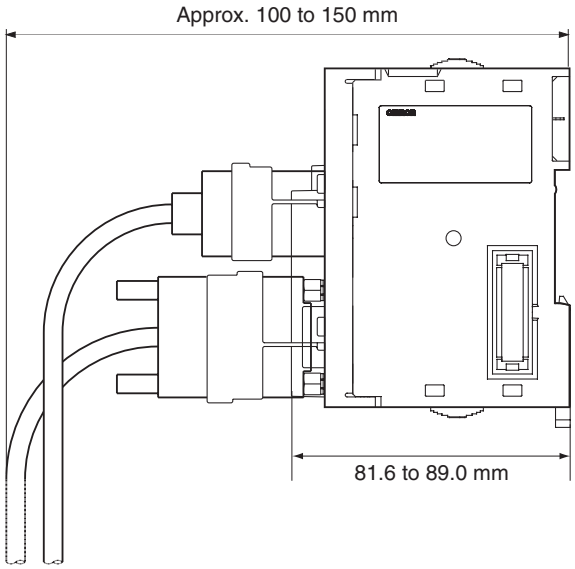




DIN Track	A
PFP-100N2	16 mm
PFP-100N	7.3 mm
PFP-50N	7.3 mm

Installation Height

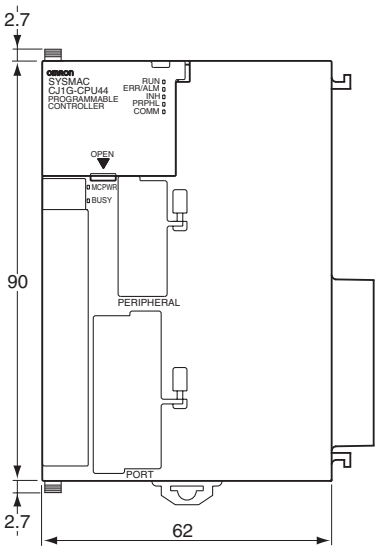
The installation height of the CJ-series CPU Rack and Expansion Racks varies from 81.6 to 89.0, depending on the I/O Units that are mounted. When a Programming Device (CX-Programmer or Programming Console) is connected, however, even greater height is required. Allow sufficient depth in the control panel containing the PC.



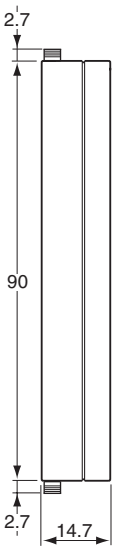
Unit Dimensions

CJ-series CPU Unit

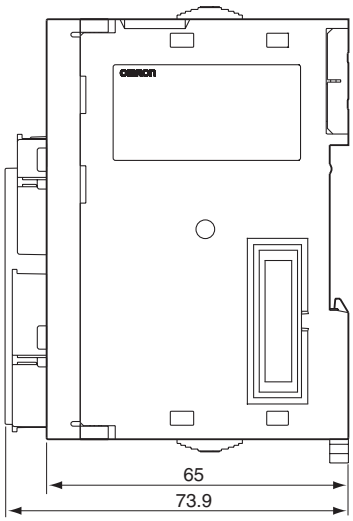
CPU Unit



End Cover



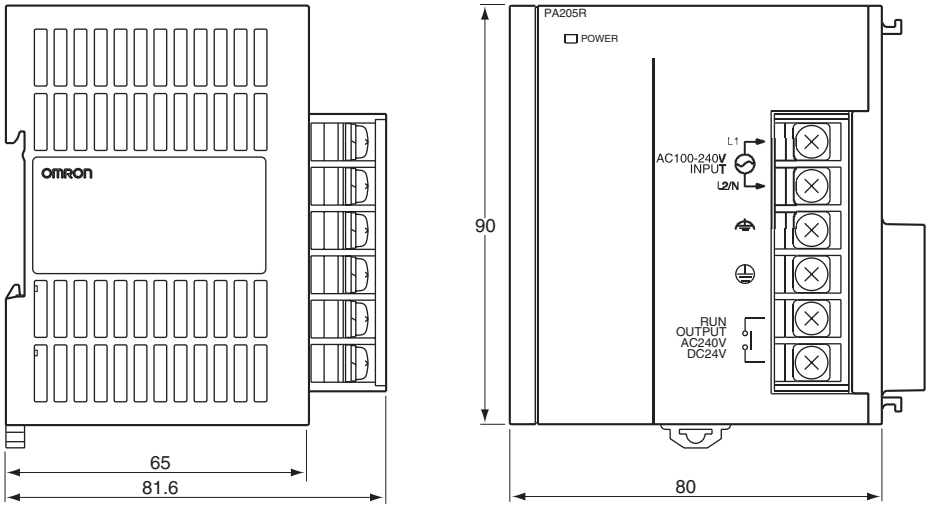
Unit Depth



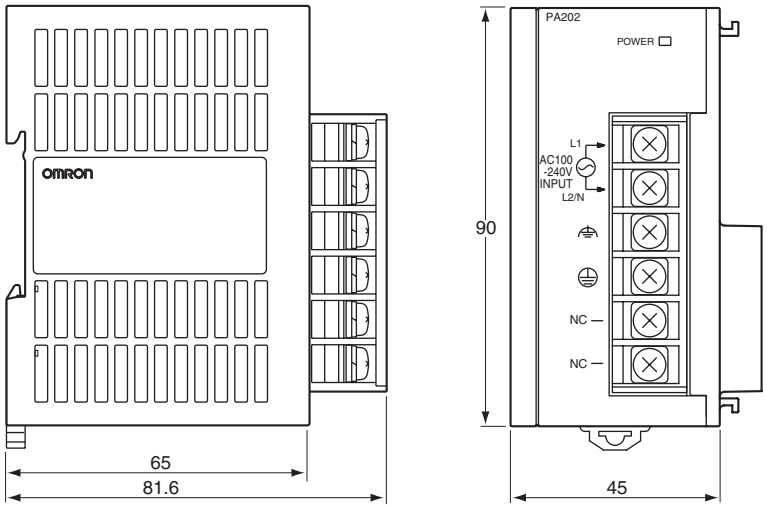
The depth is the same for all Units.

CJ-series Power Supply Units

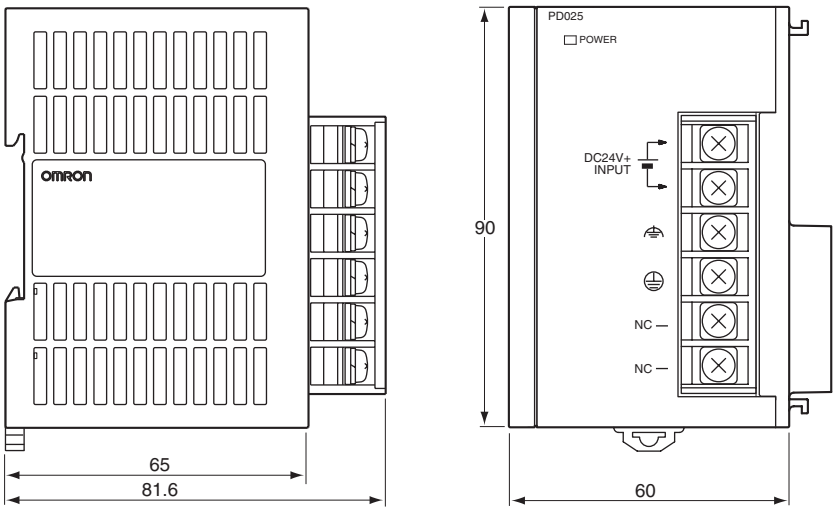
CJ1W-PA205R



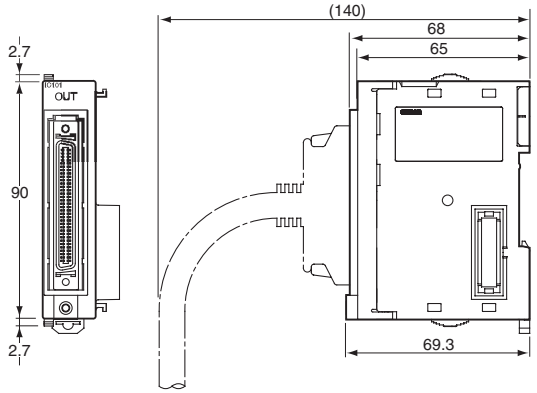
CJ1W-PA202



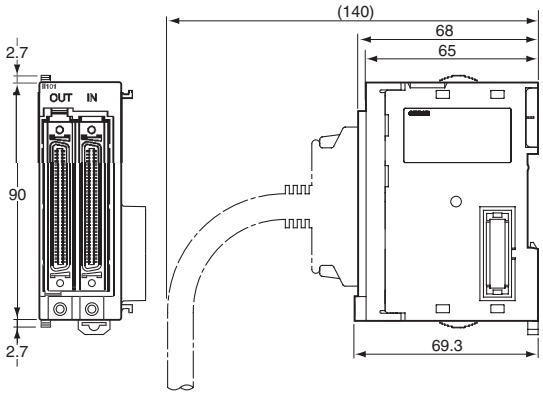
CJ1W-PD025



CJ1W-IC101 I/O Control Unit



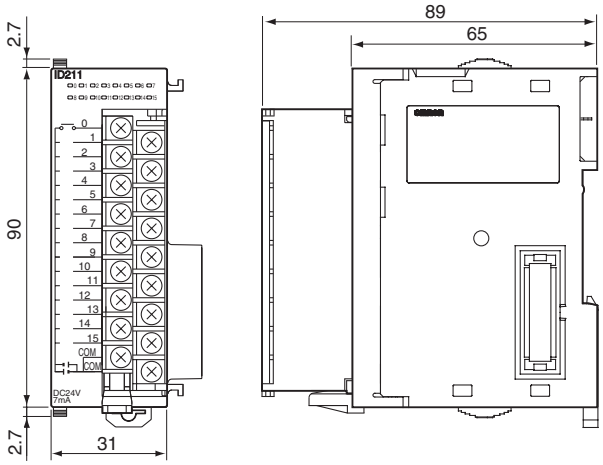
CJ1W-II101 I/O Interface Unit



CJ-series Basic I/O Units

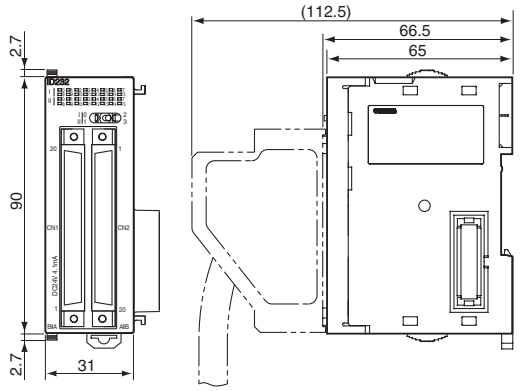
8/16-point Basic I/O Units

CJ1W-ID211 (16-pt input)
CJ1W-IA201 (8-pt input)
CJ1W-IA111 (16-pt input)
CJ1W-INT01 (16-pt interrupt input)
CJ1W-OD201 (8-pt sinking output)
CJ1W-OD202 (8-pt sourcing output)
CJ1W-OD211 (16-pt sinking output)
CJ1W-OD212 (16-pt sourcing output)
CJ1W-OC201 (8-pt relay output)
CJ1W-OC211 (16-pt relay output)
CJ1W-OA201 (8-pt triac output)



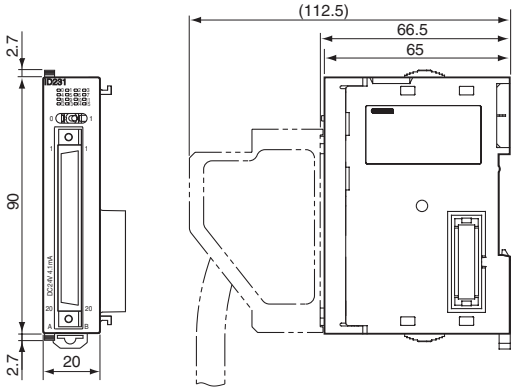
64-point Basic I/O Units, Fujitsu-compatible Connector

CJ1W-ID261 (64-pt input)
CJ1W-OD261 (64-pt output)



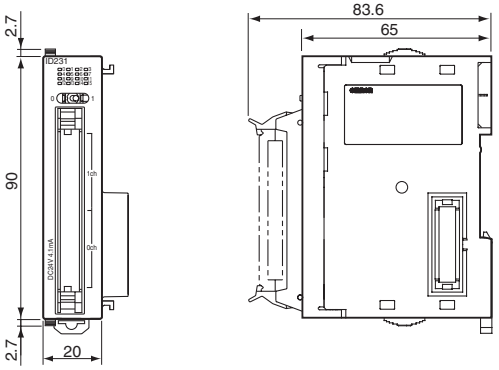
32-point Basic I/O Units, Fujitsu-compatible Connector

CJ1W-ID231 (32-pt input)
CJ1W-OD231 (32-pt output)



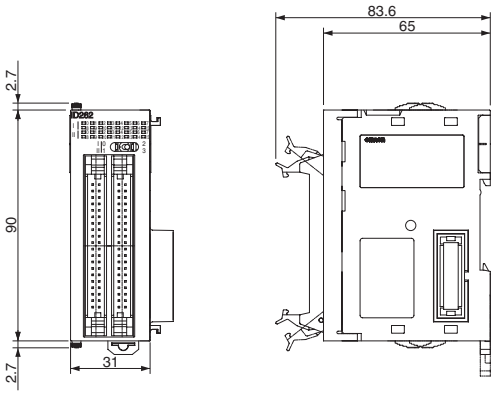
32-point Basic I/O Units, MIL Connector

CJ1W-ID232 (32-pt input)
CJ1W-OD232 (32-pt output)
CJ1W-OD233 (32-pt output)



32-point Basic I/O Units, Fujitsu-compatible Connector

CJ1W-ID262 (64-pt input)
CJ1W-OD263 (64-pt output)



Note Refer to individual Unit operation manuals for the dimensions of CJ-series Special I/O Units and CJ-series CPU Bus Units.

5-2-4 CJ-series Unit Weights

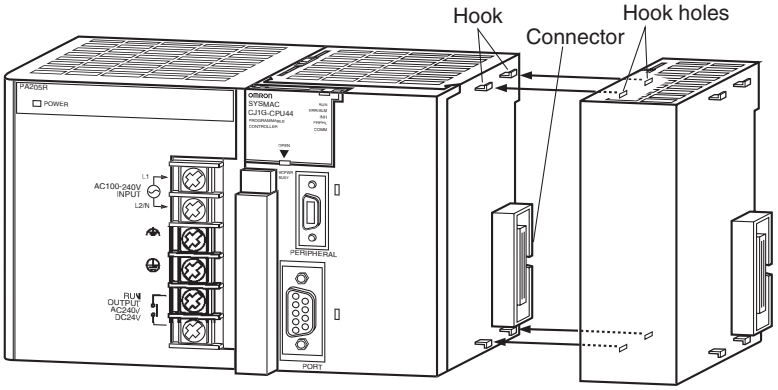
Name		Model number	Weight
CJ-series Power Supply Unit		CJ1W-PA205R	250 g max.
		CJ1W-PA202	200 g max.
		CJ1W-PD025	300 g max.
CJ-series CPU Units		CJ1H-CPU66H	200 g max. (See note.)
		CJ1H-CPU65H	200 g max. (See note.)
		CJ1G-CPU45H	190 g max. (See note.)
		CJ1G-CPU44H	190 g max. (See note.)
		CJ1G-CPU43H	190 g max. (See note.)
		CJ1G-CPU42H	190 g max. (See note.)
		CJ1G-CPU45	200 g max. (See note.)
		CJ1G-CPU44	200 g max. (See note.)
I/O Control Unit		CJ1W-IC101	70 g max.
I/O Interface Unit		CJ1W-II101	130 g max. (See note.)
CJ-series Basic I/O Units	Input Units	CJ1W-ID211	110 g max.
		CJ1W-ID231	70 g max.
		CJ1W-ID232	70 g max.
		CJ1W-ID261	110 g max.
		CJ1W-ID262	110 g max.
		CJ1W-IA201	130 g max.
		CJ1W-IA111	130 g max.
		CJ1W-INT01	110 g max.
	Output Units	CJ1W-OD201	110 g max.
		CJ1W-OD202	120 g max.
		CJ1W-OD211	110 g max.
		CJ1W-OD212	120 g max.
		CJ1W-OD231	70 g max.
		CJ1W-OD232	80 g max.
		CJ1W-OD261	110 g max.
		CJ1W-OD263	110 g max.
		CJ1W-OC201	140 g max.
		CJ1W-OC211	170 g max.
		CJ1W-OA201	150 g max.

Note The CPU Unit and I/O Interface Unit weights include the weight of the End Cover.

5-2-5 Connecting PC Components

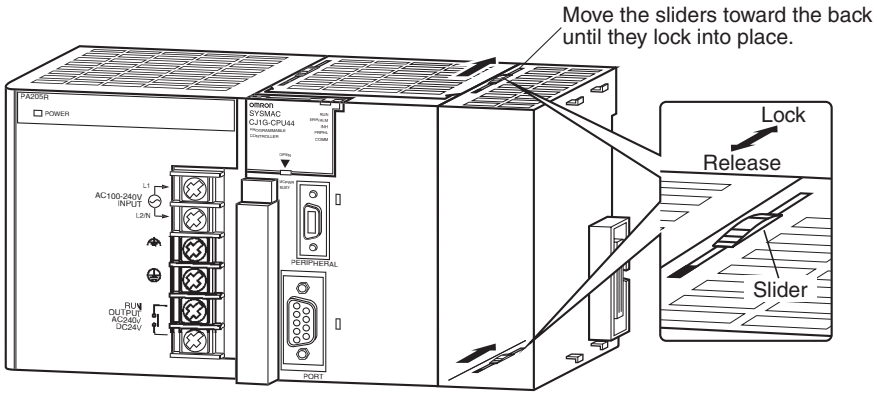
The Units that make up a CJ-series PC can be connected simply by pressing the Units together and locking the sliders by moving them toward the back of the Units. The End Cover is connected in the same way to the Unit on the far right side of the PC. Follow the procedure listed below to connect PC components.

1,2,3... 1. The following diagram shows the connection of two Units that make up a CJ-series PC. Join the Units so that the connectors fit exactly.



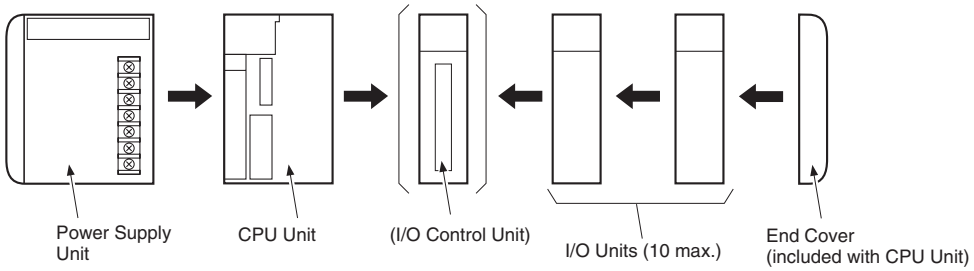
2. The yellow sliders at the top and bottom of each Unit lock the Units together. Move the sliders toward the back of the Units as shown below until they click into place.

   Note If the locking tabs are not secured properly, the CJ-series may not function properly. Be sure to slide the locking tabs until they are securely in place.



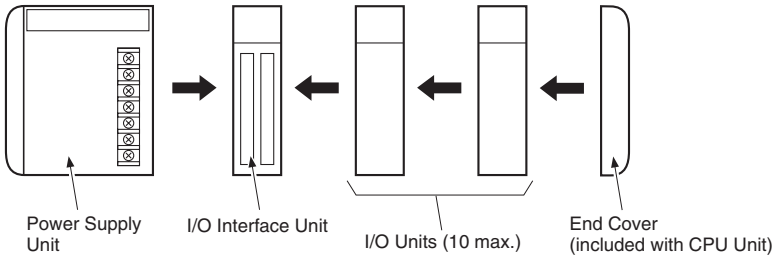
3. Attach the End Cover to the Unit on the far right side of the Rack.

CPU Rack



Note Connect the I/O Control Unit directly to the CPU Unit to enable connecting Expansion Racks.

Expansion Rack



Note Connect the I/O Interface Unit directly to the Power Supply Unit.

There is no Backplane for the CJ-series. The PC is constructed by connecting Units together using the connectors on the sides.

⚠ **Caution** Attach the End Cover to the Unit on the far right side of the Rack. An I/O bus error will occur and the PC will not operate in either RUN or MONITOR mode if the End Cover is not connected. If this occurs, the following information will be set in memory.

Name	Address	Status
I/O Bus Error Flag	A 40114	ON
I/O Bus Error Slot Number	A40400 to A40407	0E Hex
I/O Bus Error Rack Number	A40408 to A40415	0E Hex

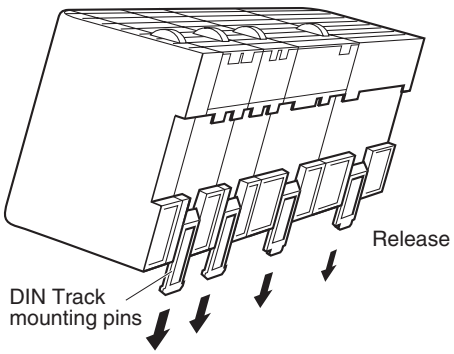
Note

1. Always turn OFF the power supply before connecting Units to each other.
2. Always turn OFF the power supply to the entire system before replacing a Unit.
3. A maximum of 10 I/O Units can be connected to a CPU Rack or an Expansion Rack. If 11 or more I/O Units are connected, and I/O overflow error will occur and the PC will not operate in either RUN or MONITOR mode. If this occurs, The I/O Overflow Flag (A40111) will turn ON and A40713 to A40715 (I/O Overflow Details 2) will turn ON.

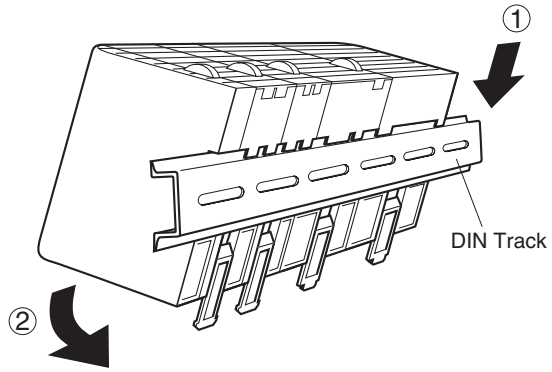
5-2-6 DIN Track Installation

Use the following procedure to install a CJ-series PC on DIN Track.

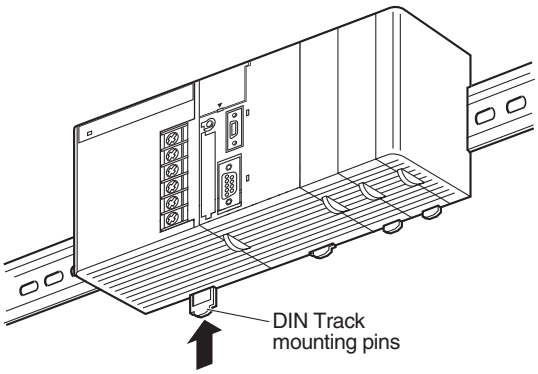
1,2,3... 1. Release the pins on the backs of the CJ-series Units.



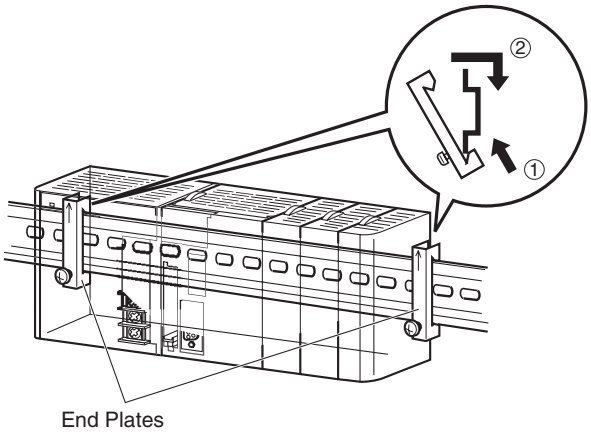
2. Fit the back of the PC onto the DIN Track by inserting the top of the track and then pressing in at the bottom of the PC, as shown below.



3. Lock the pins on the backs of the CJ-series Units.



4. Install a DIN Track End Plate on each end of the PC. To install an End Plate, hook the bottom on the bottom of the track, rotate the Plate to hook the top of the Plate on the top of the track, and then tighten the screw to lock the Plate in place.

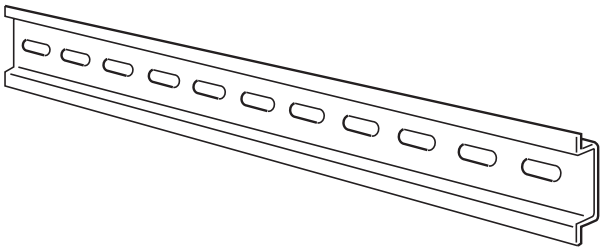


DIN Track and Accessories

Use the DIN Track and DIN Track End Plates shown below.

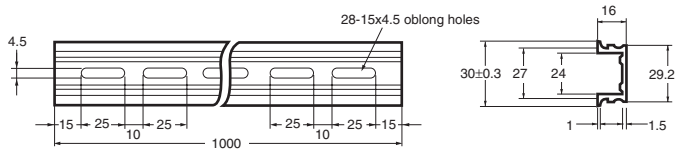
DIN Track

Model numbers: PFP-50N (50 cm), PFP-100N (100 cm), PFP-100N2 (100 cm)

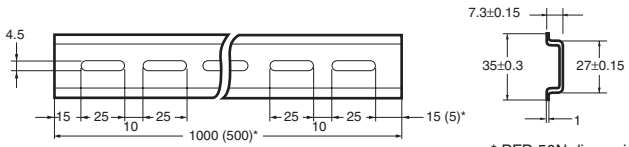


Secure the DIN Track to the control panel using M4 screws separated by 210 mm (6 holes) or less and using at least 3 screws. The tightening torque is 1.2 N·m.

PFP-100N2 DIN Track



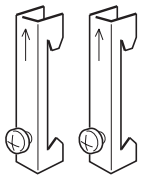
PFP-100N/50N DIN Track



* PFP-50N dimensions are given in parentheses.

DIN Track End Plates (2 required)

Model number: PFP-M



5-2-7 Connecting CJ-series Expansion Racks

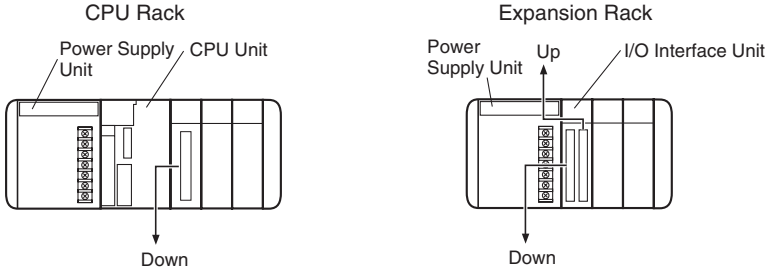
CS/CJ-series I/O Connecting Cables are used to connect the CPU Rack and Expansion Racks.

CS/CJ-series I/O Connecting Cables

The CS/CJ-series I/O Connecting Cables have connectors with a simple lock mechanism are used to connect the CPU Rack to an Expansion Rack or to connect two Expansion Racks.

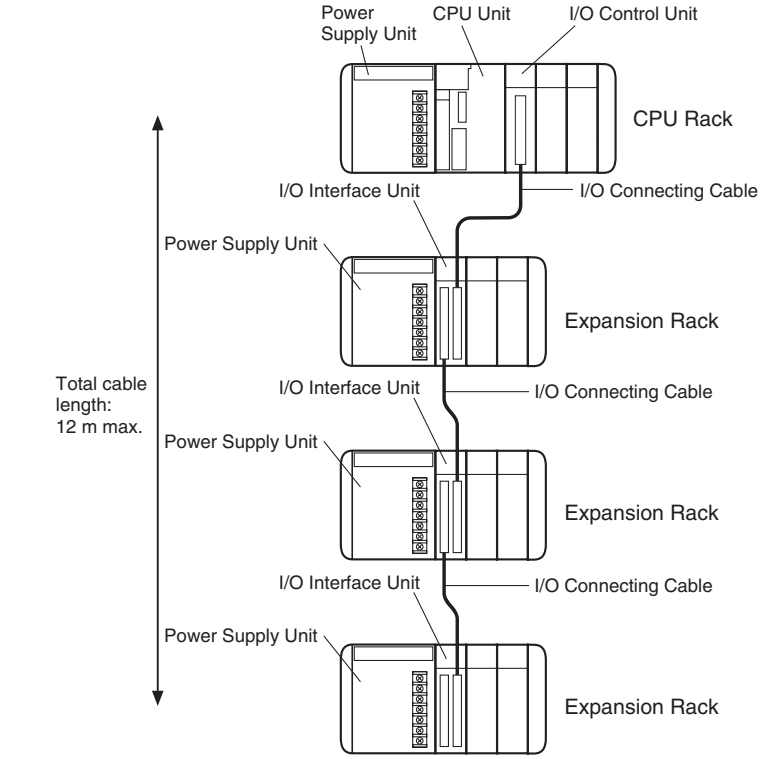
Model number	Cable length
CS1W-CN313	0.3 m
CS1W-CN713	0.7 m
CS1W-CN223	2 m
CS1W-CN323	3 m
CS1W-CN523	5 m
CS1W-CN133	10 m
CS1W-CN133B2	12 m

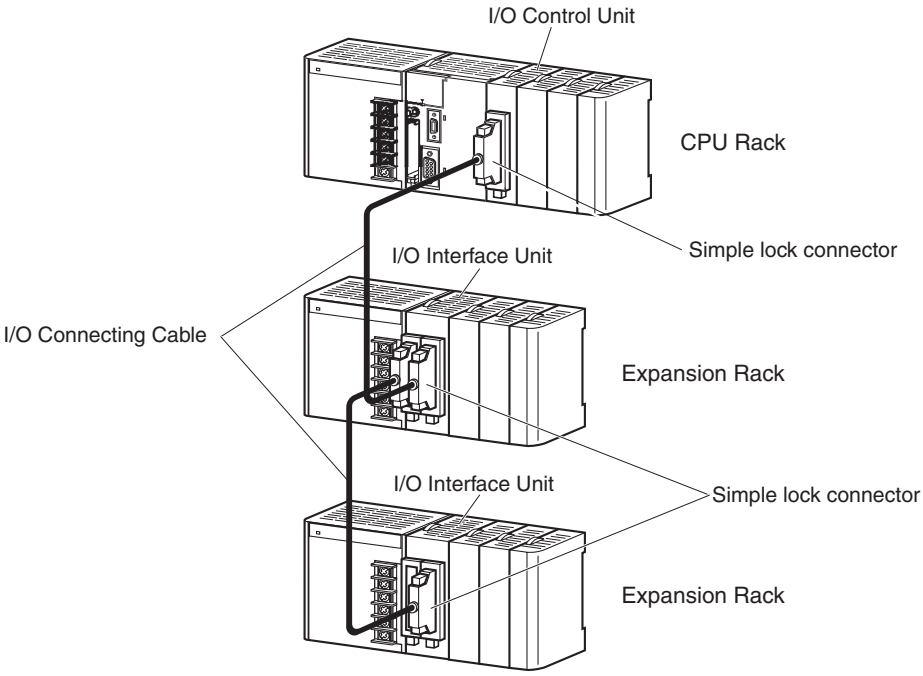
- Install the Racks and select I/O Connecting Cables so that the total length of all I/O Connecting Cables does not exceed 12 m.
- The following diagram shows where each I/O Connecting Cable must be connected on each Rack. The Rack will not operate if the cables aren't connected properly. (The "up" direction is towards the CPU Unit and "down" is away from the CPU Unit.)



- The following diagram shows examples of proper Rack connections. Connect the simple lock connectors to the I/O Control Unit on the CJ-series CPU Rack and the I/O Interface Unit on the CJ-series Expansion Rack.

- The top and bottom of the connector are different. Be sure the connector is facing the correct direction before connecting it.



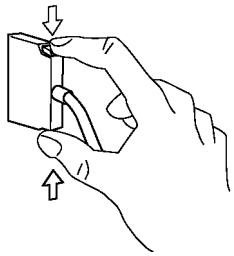


Connecting the Simple Locking Connectors

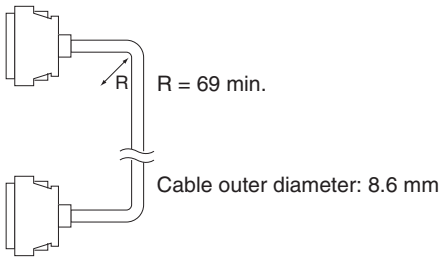
Press the tabs on the end of the connector and insert the connector until it locks in place. The PC will not operate properly if the connector isn't inserted completely.

Note

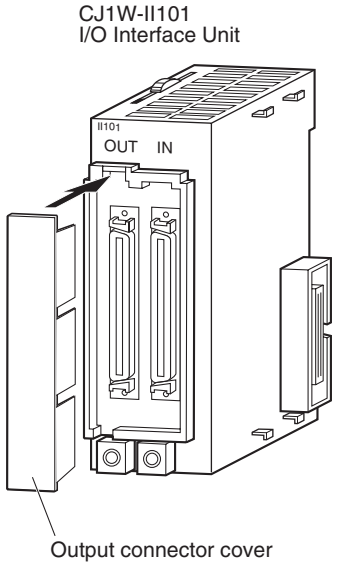
1. When using an I/O Connecting Cable with a locking connector, be sure that the connector is firmly locked in place before using it.



2. Always turn OFF the power supply to the PC before connecting a cable.
3. Do not route the I/O Connecting Cables through ducts that contain the I/O or power wiring.
4. An I/O bus error will occur and the PC will stop if an I/O Connecting Cable's connector separates from the Rack. Be sure that the connectors are secure.
5. A 63-mm hole will be required if the I/O Connecting Cable must pass through a hole when connecting an Expansion Rack.
6. The cables can withstand a pulling force up to 49 N (11 lbs), so be sure that they aren't pulled too forcefully.
7. The I/O Connecting Cables mustn't be bent too severely. The minimum bending radii are shown in the following diagram.



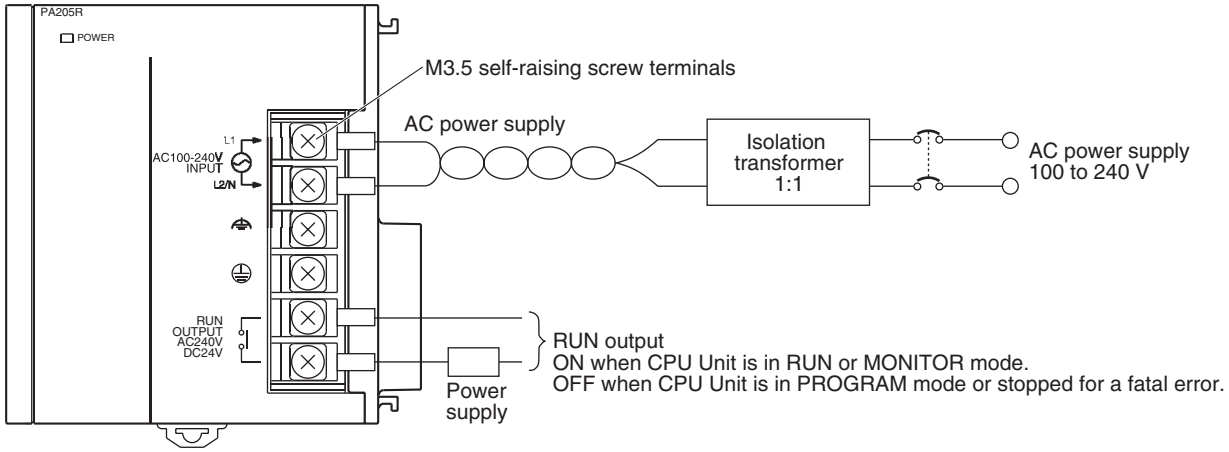
8. Always attach the cover to the output connector (left side) on the last I/O Interface Unit on the last Expansion Rack to protect it from dust.



5-3 Wiring

5-3-1 Power Supply Wiring

CJ1W-PA205R Power Supply Unit (AC)



Note The RUN output function is enabled only when mounted to a CPU Rack.

AC Power Source

- Supply 100 to 240 V AC.
- Keep voltage fluctuations within the specified range:

Supply voltage	Allowable voltage fluctuations
100 to 240 V AC	85 to 264 V AC

- If one power supply phase of the equipment is grounded, connect the grounded phase side to the L2/N terminal.

Isolation Transformer

The PC's internal noise isolation circuits are sufficient to control typical noise in power supply lines, but noise between the PC and ground can be significantly reduced by connecting a 1-to-1 isolation transformer. Do not ground the secondary coil of the transformer.

Power Supply Capacity

The power consumption will be 100 VA max. per Rack for the CJ1W-PA205R and 50 VA for the CJ1W-PA202, but there will be a surge current of at least 5 times the max. current when power is turned ON.

RUN Output

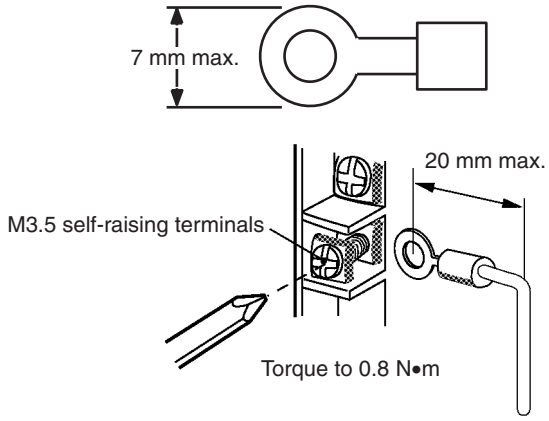
This output is ON whenever the CPU Unit is operating in RUN or MONITOR mode; it is OFF when the CPU Unit is in PROGRAM mode or a fatal error has occurred.

The RUN output can be used to control external systems, such as in an emergency stop circuit that turns off the power supply to external systems when the PC is not operating. (See *5-1 Fail-safe Circuits* for more details on the emergency stop circuit.)

Item	CJ1W-PA205R
Contact form	SPST-NO
Maximum switching capacity	240 V AC: 2 A for resistive loads 120 V AC 0.5 A for inductive loads 24 V DC: 2 A for resistive loads 24 V AC 2 A for inductive loads

Crimp Terminals

The terminals on the Power Supply Unit are M3.5, self-raising terminals with screws. Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Tighten the terminal block screws to the torque of 0.8 N • m. Use round-type crimp terminals (M3.5) having the dimensions shown below.



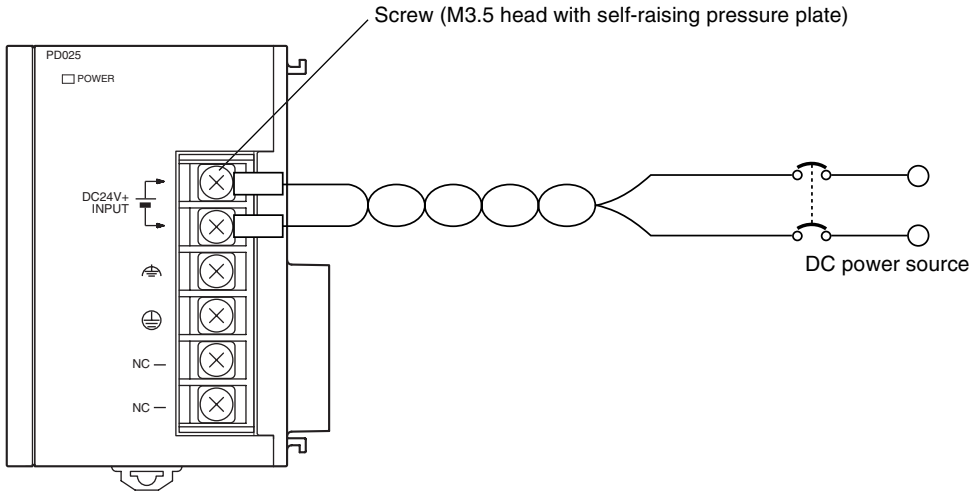
⚠ **Caution** Tighten the AC power supply terminal block screws to the torque of 0.8 N • m. Loose screws may result in short-circuit, malfunction, or fire.

Note

1. Supply power to all of the Power Supply Units from the same source.
2. Do not remove the protective label from the top of the Unit until wiring has been completed. This label prevents wire strands and other foreign matter from entering the Unit during wiring procedures.
3. Do not forget to remove the label from the top of the Power Supply Unit after wiring the Unit. The label will block air circulation needed for cooling.

DC Power Supplies

CJ1W-PD025 Power Supply Unit



DC Power Source

Supply 24 VDC. Keep voltage fluctuations within the specified range (19.2 to 28.8 VDC).

Power Supply Capacity

The maximum power consumption is 50 W per Rack, but there will be a surge current of about 5 times that level when the power is turned on.

Crimp Terminals

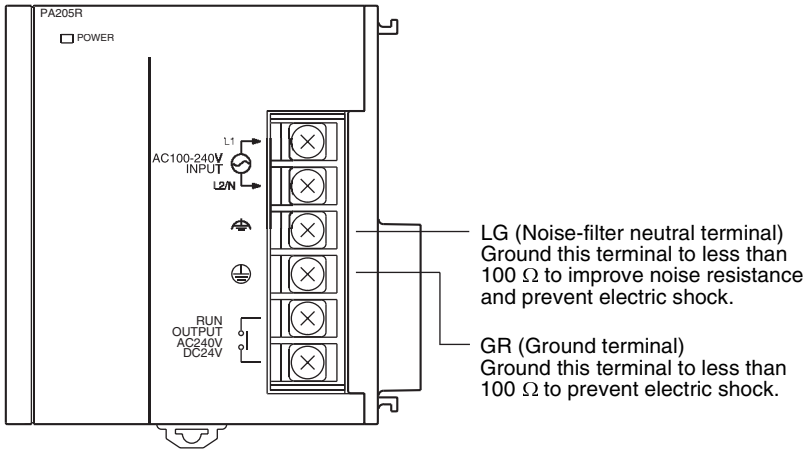
The terminals on the Power Supply Unit are M3.5, self-raising terminals with screws. Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Tighten the terminal block screws to the torque of 0.8 N·m. Use crimp terminals (M3.5) having the dimensions shown below.

Note

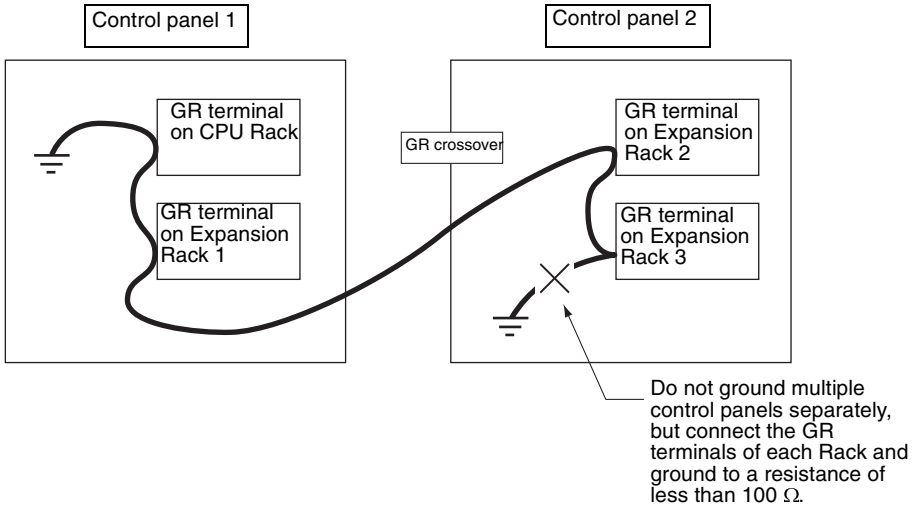
1. Be sure not to reverse the positive and negative leads when wiring the power supply terminals.
2. Supply power to all of the Power Supply Units from the same source.
3. Do not remove the protective label from the top of the Unit until wiring has been completed. This label prevents wire strands and other foreign matter from entering the Unit during wiring procedures.
4. Do not forget to remove the label from the top of the Power Supply Unit after wiring the Unit. The label will block air circulation needed for cooling.

Grounding

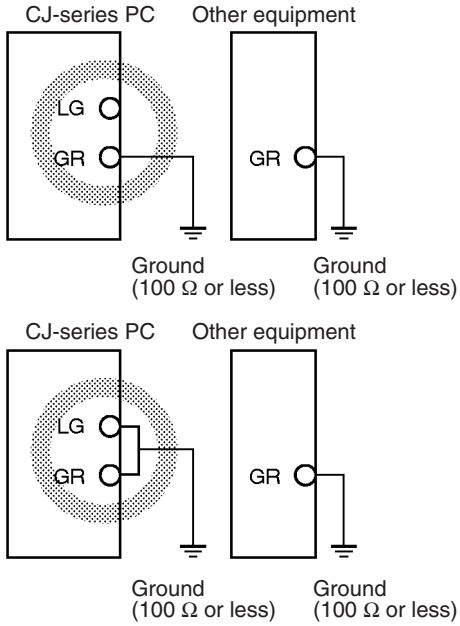
The diagram below shows the location of the ground and line ground terminals.



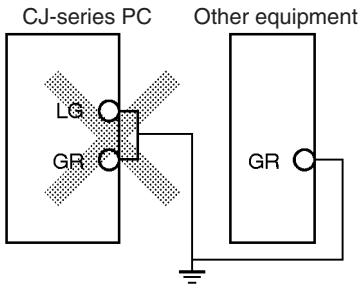
- To help prevent electrical shock, ground the ground terminal (GR: ⏚) with a ground resistance of less than 100 Ω using a 14-gauge wire (minimum cross-sectional area of 2 mm^2).
- The line ground terminal (LG:⏚) is a noise-filtered neutral terminal. If noise is a significant source of errors or electrical shocks are a problem, connect the line ground terminal to the ground terminal and ground both with a ground resistance of less than 100 Ω.
- The ground wire should not be more than 20 m long.
- The following grounding configurations are acceptable.
- The CJ-series PCs are designed to be mounted so that they are isolated (separated) from the mounting surface to protect them from the effects of noise in the installation environment (e.g., the control panel).



- Do not share a ground line with other equipment.



- Do not share the PC's ground with other equipment or ground the PC to the metal structure of a building. The configuration shown in the following diagram may worsen operation.



Crimp Terminals

The terminals on the Power Supply Unit are M3.5, self-raising terminals with screws. Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Tighten the terminal block screws to the torque of 0.8 N• m. Use crimp terminals (M3.5) having the dimensions shown below.

5-3-2 Wiring CJ-series Basic I/O Units with Terminal Blocks

I/O Unit Specifications

Double-check the specifications for the I/O Units. In particular, do not apply a voltage that exceeds the input voltage for Input Units or the maximum switching capacity for Output Units. Doing so may result in breakdown, damage, or fire.

When the power supply has positive and negative terminals, be sure to wire them correctly.

Electric Wires

The following wire gauges are recommended.

Terminal Block Connector	Wire Size
18-terminal	AWG 22 to 18 (0.32 to 0.82 mm^2)

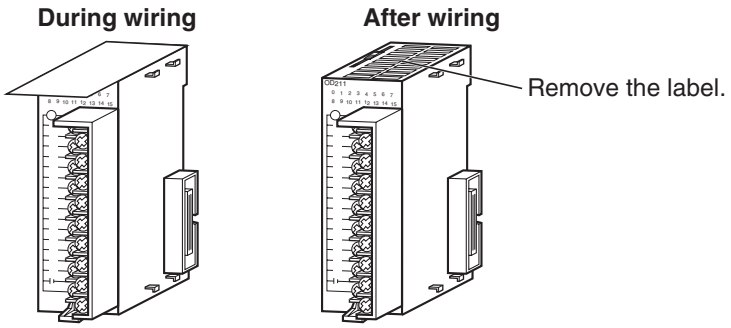
Note The current capacity of electric wire depends on factors such as the ambient temperature and insulation thickness as well as the gauge of the conductor.

Crimp Terminals

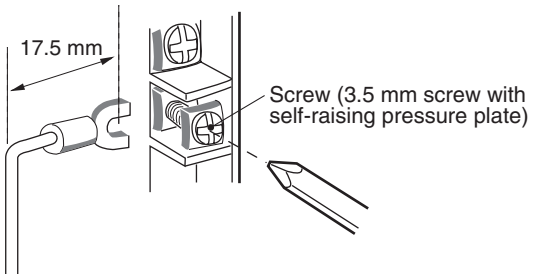
The terminals on the Power Supply Unit are M3, self-raising terminals with screws. Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Tighten the terminal block screws to the torque of 0.5 N·m. Use crimp terminals (M3) having the dimensions shown below.

Wiring

Do not remove the protective label from the top of the Unit until wiring has been completed. This label prevents wire strands and other foreign matter from entering the Unit during wiring procedures. (Remove the label after wiring has been completed to allow air circulation needed for cooling.)

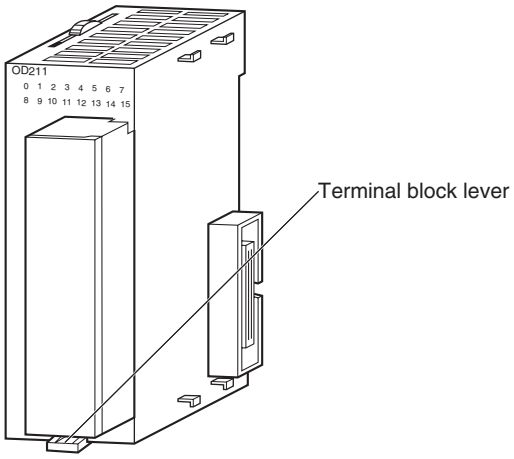


- Wire the Units so that they can be easily replaced. In addition, make sure that the I/O indicators are not covered by the wiring.
- Do not place the wiring for I/O Units in the same duct or raceway as power lines. Inductive noise can cause errors in operation.
- Tighten the terminal screws to the torque of 0.5 N·m.
- The terminals have screws with 3.5-mm diameter heads and self-raising pressure plates. Connect the lead wires to the terminals as shown below.



Terminal Blocks

The I/O Units are equipped with removable terminal blocks. The lead wires do not have to be removed from the terminal block to remove it from an I/O Unit.



CJ-series Basic I/O Unit

5-3-3 Wiring I/O Units with Connectors

This section describes wiring for the following Units:

- CJ-series Basic I/O Units with Connectors (32- and 64-point Units)

CJ-series Basic I/O Units with connectors use special connectors to connector to external I/O devices. The user can combine a special connector with cable or use a preassembled OMRON cable to connect to a terminal block or I/O Terminal. The available OMRON cables are described later in this section.

- Be sure not to apply a voltage that exceeds the input voltage for Input Units or the maximum switching capacity for Output Units.
- When the power supply has positive and negative terminals, be sure to wire them correctly. Loads connected to Output Units may malfunction if the polarity is reversed.
- Use reinforced insulation or double insulation on the DC power supply connected to DC I/O Units when required by EC Directives (low voltage).
- When connecting the connector to the I/O Unit, tighten the connector screws to a torque of 0.2 N • m.
- Turn on the power after checking the connector's wiring. Do not pull the cable. Doing so will damage the cable.
- Bending the cable too sharply can damage or break wiring in the cable.

Note CJ-series Basic I/O Units with connectors have the same connector pin allocations as the C200H High-density I/O Units and CS-series I/O Units with connectors to make them compatible.

Available Connectors

Use the following connectors when assembling a connector and cable.

CJ-series 32- and 64-point I/O Units with Fujitsu-compatible Connectors

Applicable Units

Model	Specifications
CJ1W-ID231	Input Unit, 24 V DC, 32 inputs
CJ1W-ID261	Input Unit, 24 V DC, 64 inputs
CJ1W-OD231	Transistor Output Unit with Sinking Outputs, 32 outputs
CJ1W-OD261	Transistor Output Unit with Sinking Outputs, 32 outputs

Applicable Cable-side Connectors

Connection	Pins	OMRON set	Fujitsu parts
Solder-type	40	C500-CE404	Socket: FCN-361J040-AU Connector bar: FCN-360C040-J2
Crimped	40	C500-CE405	Socket: FCN-363J040 Connector bar: FCN-360C040-J2 Contacts: FCN-363J-AU
Pressure-welded	40	C500-CE403	FCN-367J040-AU

CJ-series 32- and 64-point I/O Units with MIL Connectors

Applicable Units

Model	Specifications
CJ1W-ID232	Input Unit, 24 V DC, 32 inputs
CJ1W-ID262	Input Unit, 24 V DC, 64 inputs
CJ1W-OD232	Transistor Output Unit with sourcing outputs, 32 outputs
CJ1W-OD233	Transistor Output Unit with sinking outputs, 32 outputs
CJ1W-OD263	Transistor Output Unit with sinking outputs, 64 outputs

Applicable Cable-side Connectors

Connection	Pins	OMRON set	Daiichi Denko Industries part
Pressure-welded	40	XG4M-4030-T	FRC5-A040-3T0S

Wire

We recommend using cable with wire gauges of AWG 24 or AWG 28 (0.2 mm^2 to 0.08 mm^2). Use cable with external wire diameters of 1.61 mm max.

Wiring Procedure

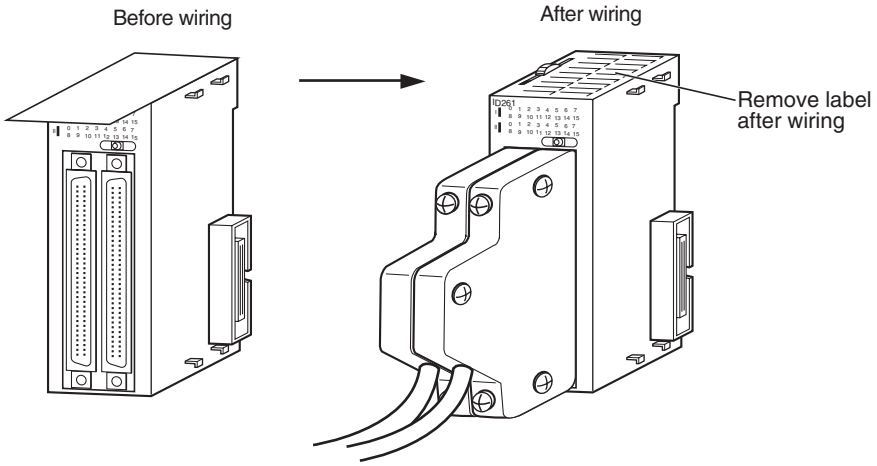
1,2,3...

1. Check that each Unit is installed securely.

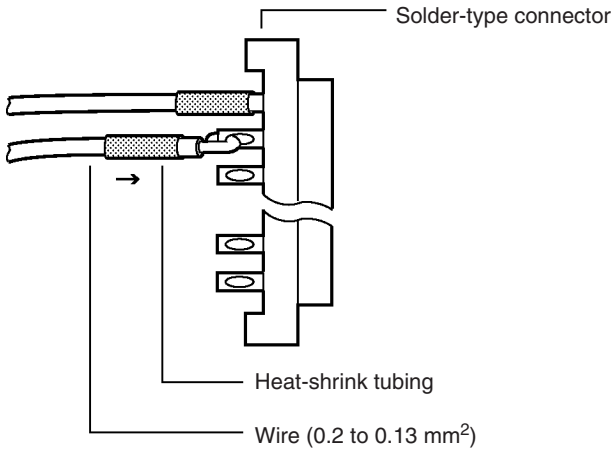
   Note Do not force the cables.

2. Do not remove the protective label from the top of the Unit until wiring has been completed. This label prevents wire strands and other foreign matter

from entering the Unit during wiring. (Remove the label after wiring has been completed to allow air circulation needed for cooling.)

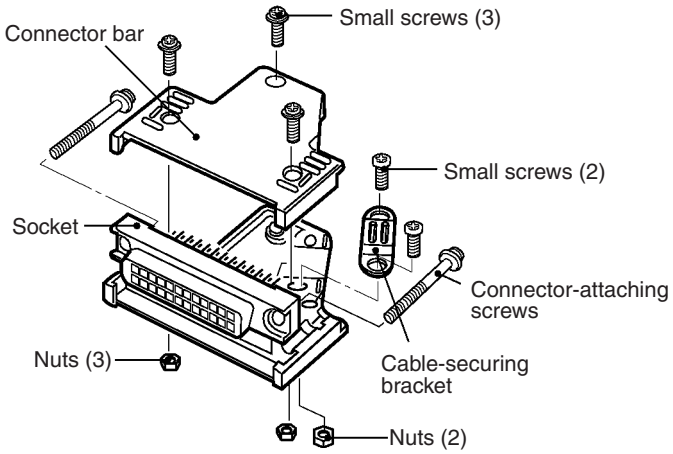


3. When solder-type connectors are being used, be sure not to accidentally short adjacent terminals. Cover the solder joint with heat-shrink tubing.

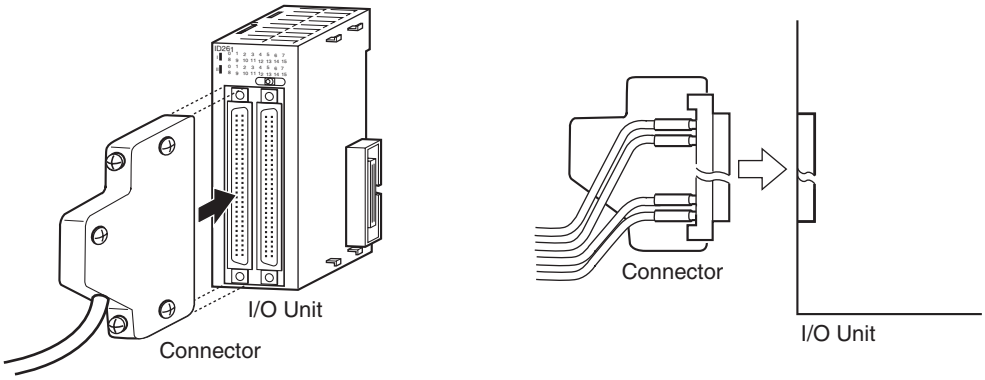


Note Double-check to make sure that the Output Unit's power supply leads haven't been reversed. If the leads are reversed, the Unit's internal fuse will blow and the Unit will not operate.

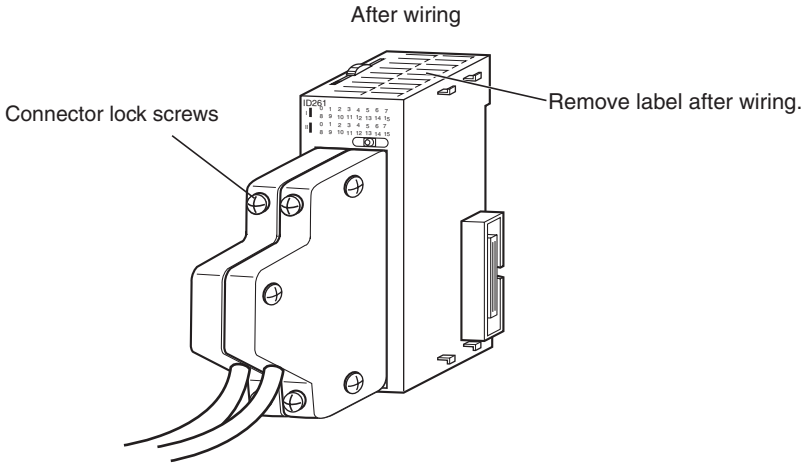
4. Assemble the connector (purchased separately).



5. Insert the wired connector.



6. Remove the protective label after wiring has been completed to allow air circulation needed for cooling.



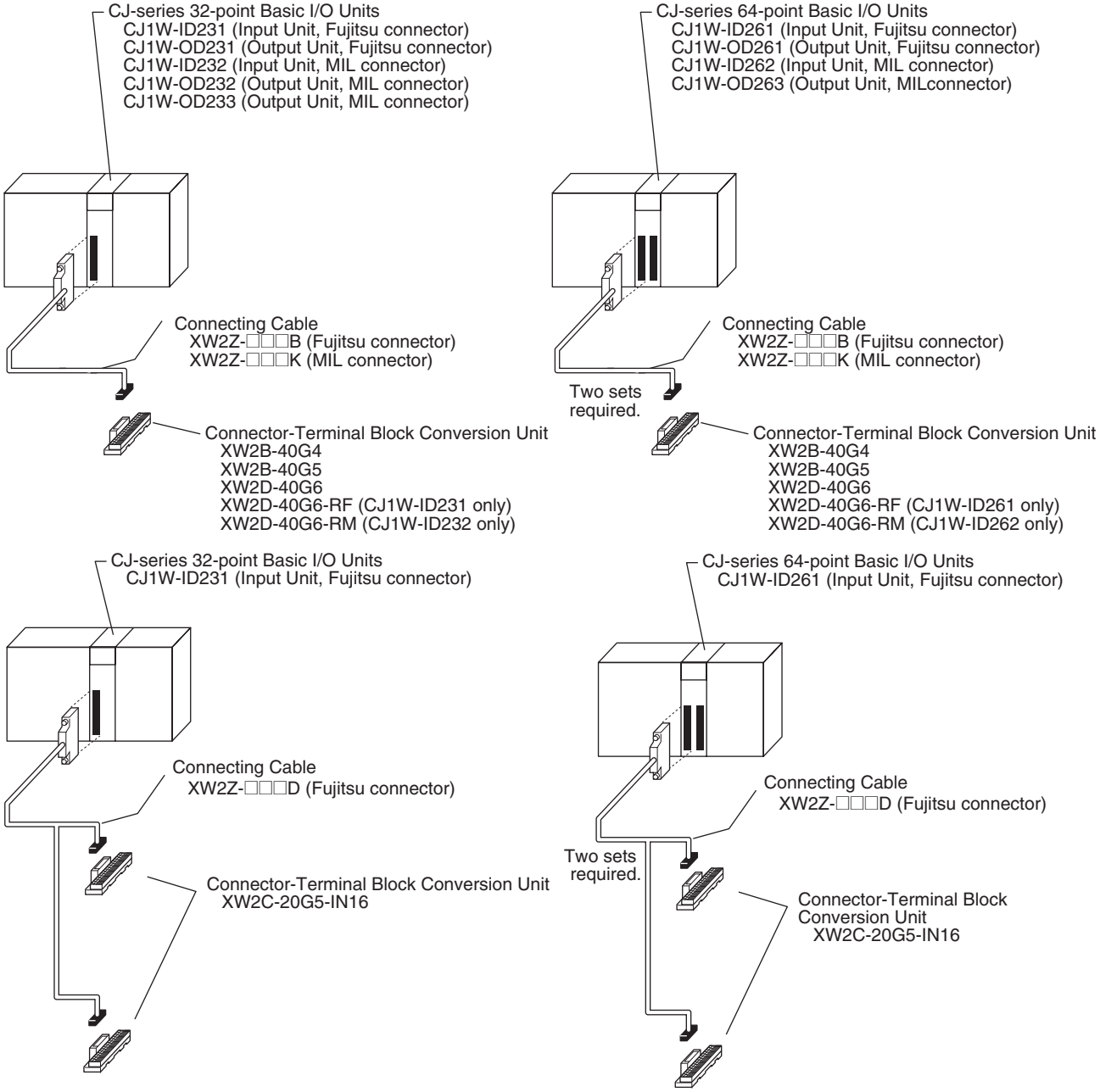
Tighten the connector-attaching screws to a torque of 0.2 N•m.

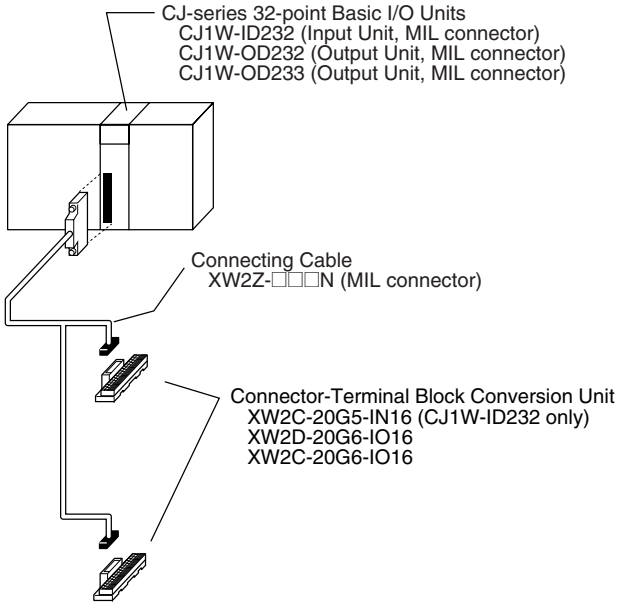
Connecting to Connector-Terminal Block Conversion Units or I/O Terminals

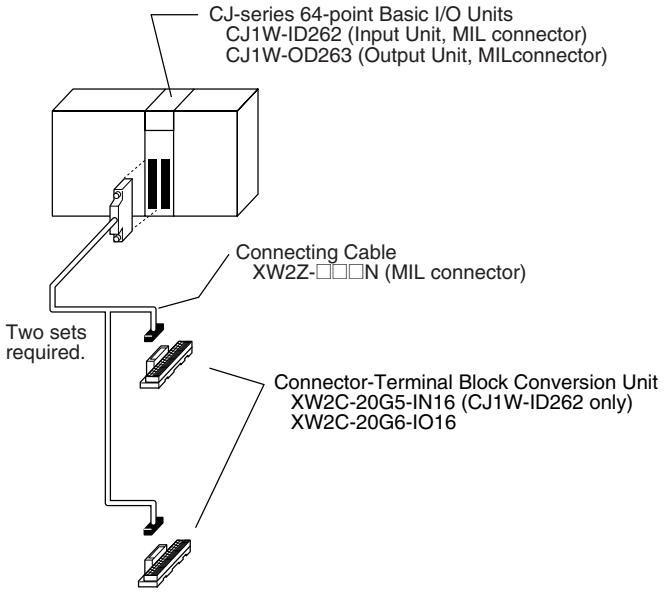
Basic I/O Units with Connectors can be connected to OMRON Connector-Terminal Block Conversion Units or OMRON I/O Terminals. Refer to *CJ-series 32/64-point Basic I/O Units with Connectors* on page 107 for a list of models.

Connecting to Terminal Blocks

The following Connecting Cables and Connector-Terminal Block Conversion Units are required to connect to terminal blocks.

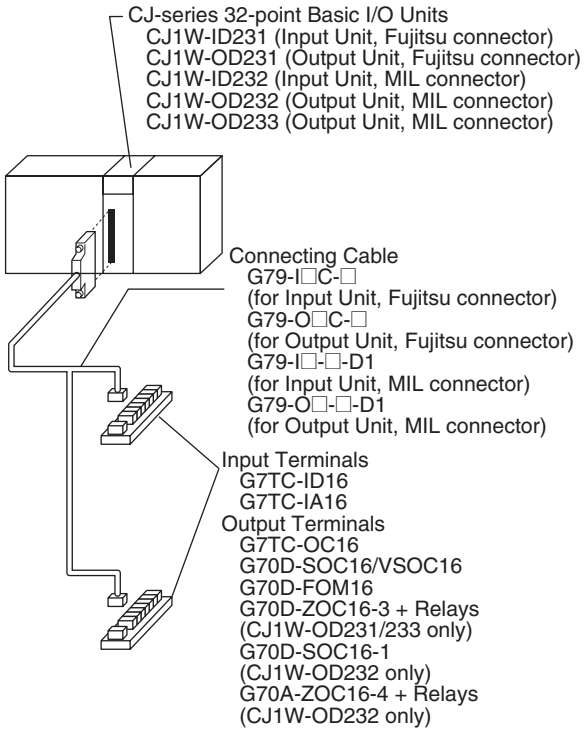


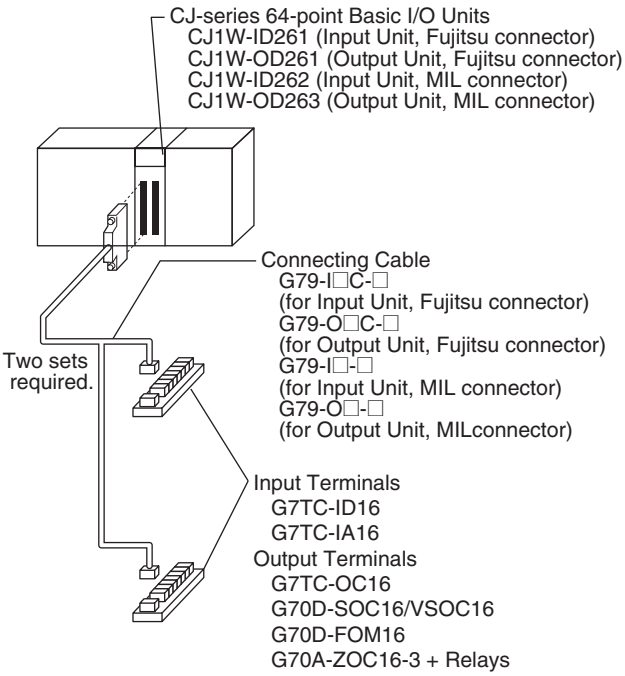




Connecting to I/O Terminals

The following Connecting Cables and I/O Terminals are required to connect to terminal blocks.





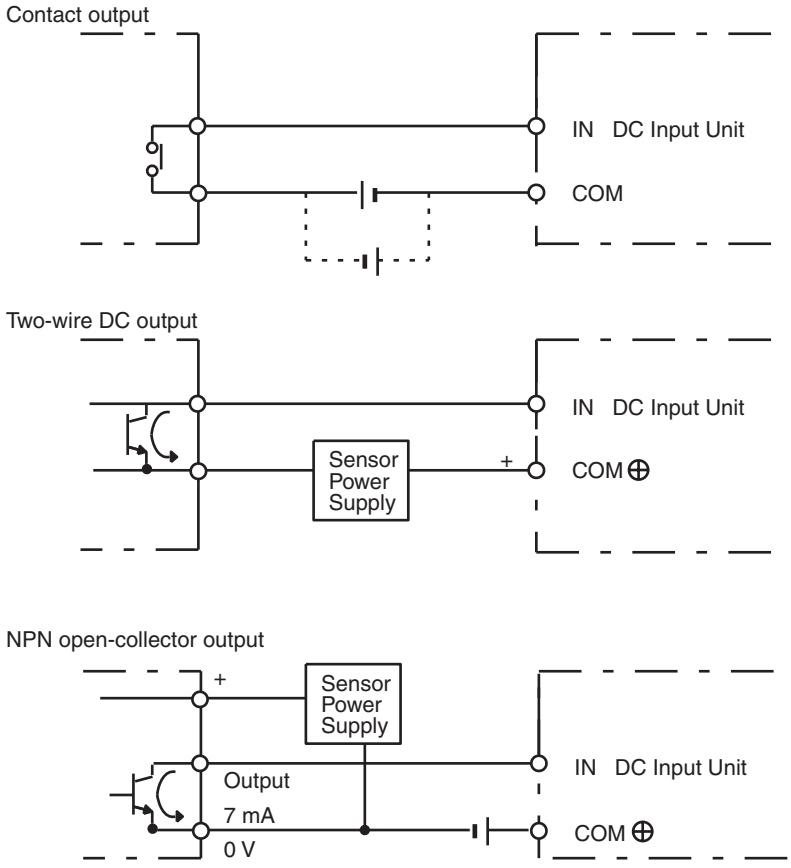
5-3-4 Connecting I/O Devices

Input Devices

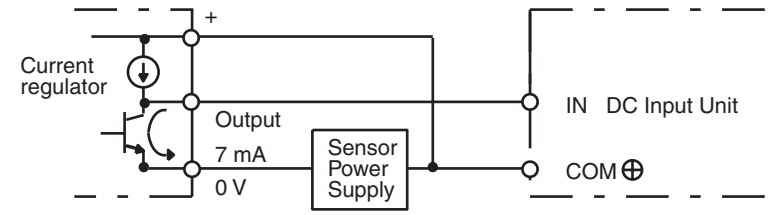
Use the following information for reference when selecting or connecting input devices.

DC Input Units

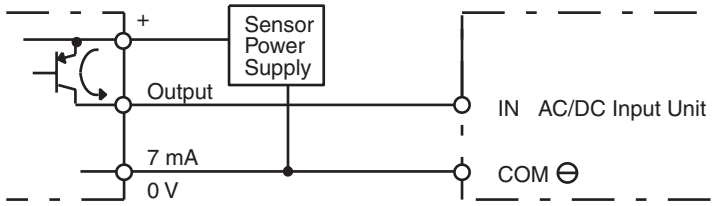
The following types of DC input devices can be connected.



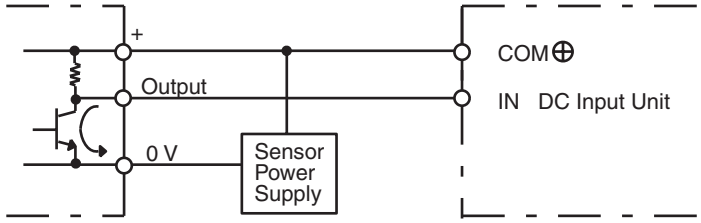
NPN current output



PNP current output

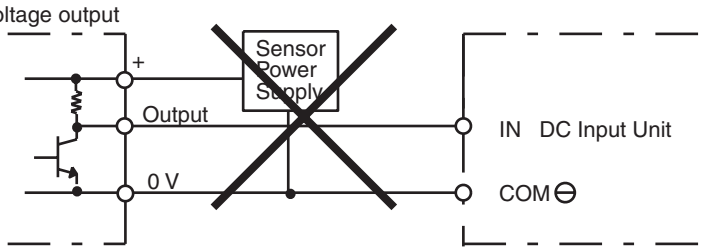


Voltage current output



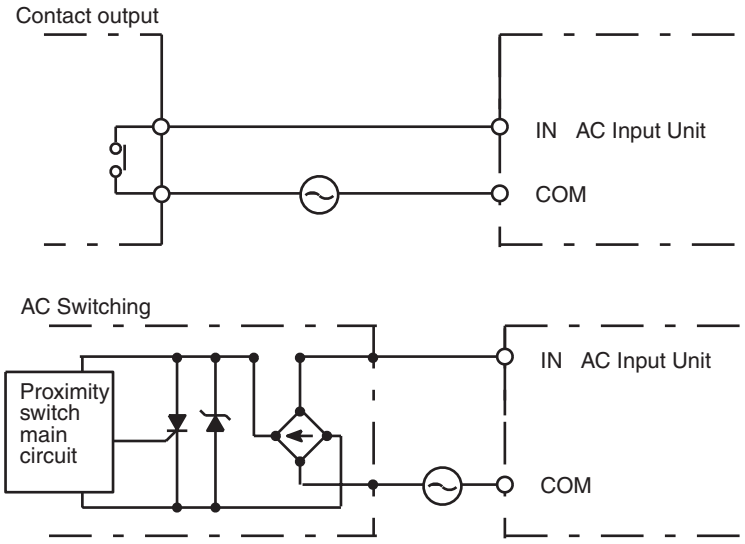
The circuit below should **NOT** be used for I/O devices having a voltage output.

Voltage output



AC Input Units

The following types of AC input devices can be connected.



Note When using a reed switch as the input contact for an AC Input Unit, use a switch with an allowable current of 1 A or greater. If Reed switches with smaller allowable currents are used, the contacts may fuse due to surge currents.

Precautions when Connecting a Two-wire DC Sensor

When using a two-wire sensor with a 12-V DC or 24-V DC input device, check that the following conditions have been met. Failure to meet these conditions may result in operating errors.

1,2,3...

1. Relation between voltage when the PC is ON and the sensor residual voltage:

   $V_{ON} \leq V_{CC} - V_R$

2. Relation between voltage when the PC is ON and sensor control output (load current):

   I_{OUT} (min) $\leq I_{ON} \leq I_{OUT}$ (max.)

   $I_{ON} = (V_{CC} - V_R - 1.5$ [PC internal residual voltage]$)/R_{IN}$

   When I_{ON} is smaller than I_{OUT} (min), connect a bleeder resistor R. The bleeder resistor constant can be calculated as follows:

   $R \leq (V_{CC} - V_R)/(I_{OUT}$ (min.) $- I_{ON})$

   Power $W \geq (V_{CC} - V_R)^2/R \times 4$ [allowable margin]

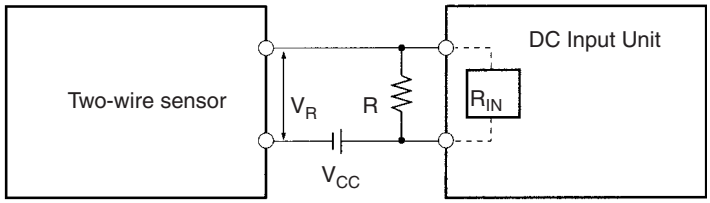
3. Relation between current when the PC is OFF and sensor leakage current:

   $I_{OFF} \geq I_{leak}$

   Connect a breeder resistor if I_{leak} is greater than I_{OFF}. Use the following equation to calculate the breeder resistance constant.

$R \leq (R_{IN} \times V_{OFF})/(I_{leak} \times R_{IN} - V_{OFF})$

Power $W \geq (V_{CC} - V_R)^2/R \times 4$ [allowable margin]



V_{CC}: Power voltage
V_{ON}: PC ON voltage
V_{OFF}: PC OFF voltage
I_{ON}: PC ON current
I_{OFF}: PC OFF current
R_{IN}: PC input impedance

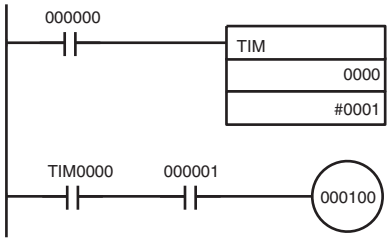
V_R: Sensor output residual current
I_{OUT}: Sensor control current (load current)
I_{leak}: Sensor leakage current
R: Bleeder resistance

4. Precautions on Sensor Surge Current

An incorrect input may occur if a sensor is turned ON after the PC has started up to the point where inputs are possible. Determine the time required for sensor operation to stabilize after the sensor is turned ON and take appropriate measures, such as inserting into the program a timer delay after turning ON the sensor.

Example

In this example, the sensor's power supply voltage is used as the input to CIO 000000 and a 100-ms timer delay (the time required for an OMRON Proximity Sensor to stabilize) is created in the program. After the Completion Flag for the timer turns ON, the sensor input on CIO 000001 will cause output bit CIO 000100 to turn ON.



Output Wiring Precautions

Output Short-circuit Protection

If a load connected to the output terminals is short-circuited, output components and the and printed circuit boards may be damaged. To guard against this, incorporate a fuse in the external circuit. Use a fuse with a capacity of about twice the rated output.

Transistor Output Residual Voltage

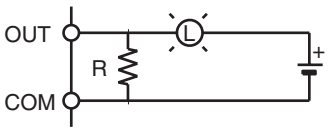
A TTL circuit cannot be connected directly to a transistor output because of the transistor's residual voltage. It is necessary to connect a pull-up resistor and a CMOS IC between the two.

Output Surge Current

When connecting a transistor or triac output to an output device having a high surge current (such as an incandescent lamp), steps must be taken to avoid damage to the transistor or triac. Use either of the following methods to reduce the surge current.

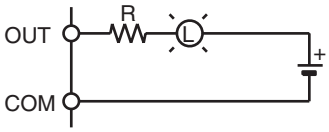
Method 1

Add a resistor that draws about 1/3 of the current consumed by the bulb.



Method 2

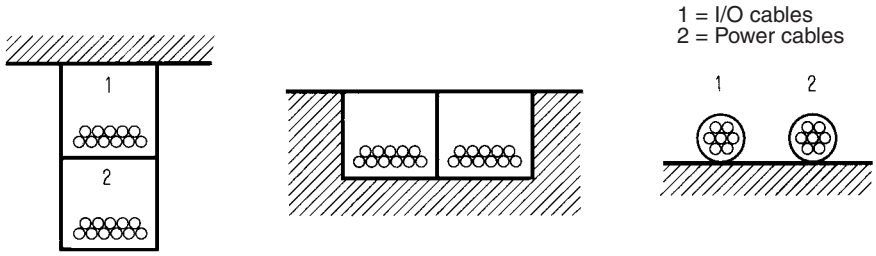
Add a control resistor as shown in the following diagram.



5-3-5 Reducing Electrical Noise

I/O Signal Wiring

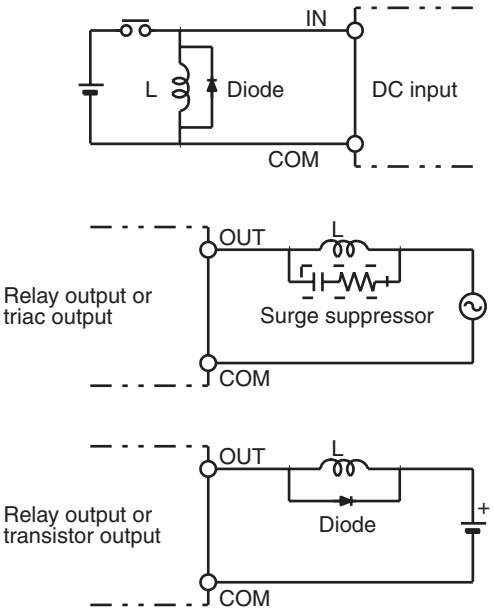
Whenever possible, place I/O signal lines and power lines in separate ducts or raceways both inside and outside of the control panel.



If the I/O wiring and power wiring must be routed in the same duct, use shielded cable and connect the shield to the GR terminal to reduce noise.

Inductive Loads

When an inductive load is connected to an I/O Unit, connect a surge suppressor or diode in parallel with the load as shown below.



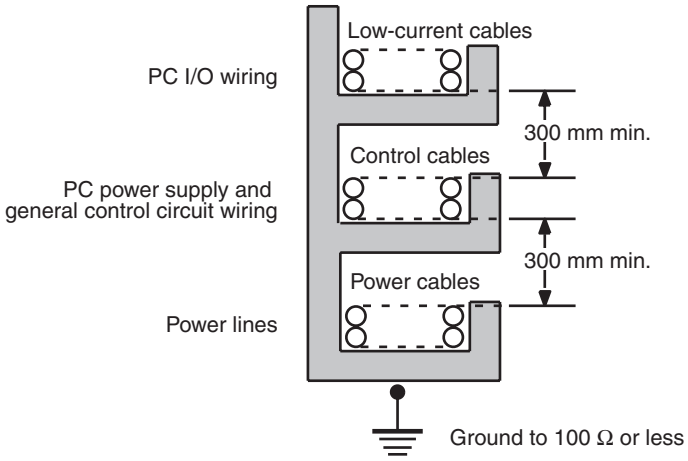
Note Use surge suppressors and diodes with the following specifications.

Surge suppressor specifications	Diode specifications
Resistor: 50 Ω Capacitor: 0.47 μF Voltage: 200 V	Breakdown voltage: 3 times load voltage min. Mean rectification current: 1 A

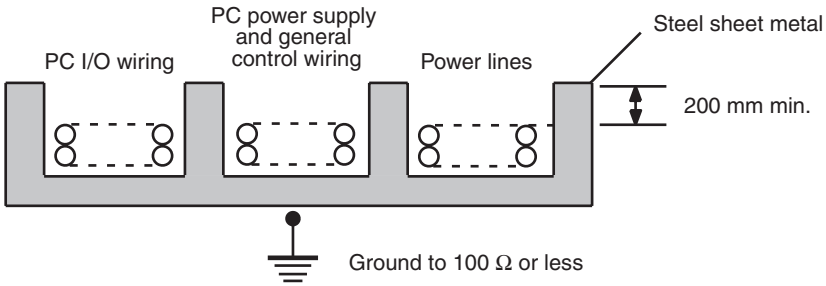
External Wiring

Observe the following precautions for external wiring.

- When multi-conductor signal cable is being used, avoid combining I/O wires and other control wires in the same cable.
- If wiring racks are parallel, allow at least 300 mm (12 inches) between the racks.



If the I/O wiring and power cables must be placed in the same duct, they must be shielded from each other using grounded steel sheet metal.



SECTION 6
DIP Switch Settings

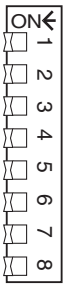
This section describes the initial hardware settings made on the CPU Unit's DIP switch.

6-1 Overview

There are two kinds of initial settings for a CJ-series PC: Hardware settings and software settings. Hardware settings are made with the CPU Unit's DIP switch and software settings are made in the PC Setup (using a Programming Device).

The DIP switch can be reached by opening the battery compartment cover on the front of the CPU Unit.

Note Always turn OFF the PC before changing any DIP switch settings. The PC may malfunction due to static discharge if the settings are changed while the PC is ON.

Appearance	Pin No.	Setting	Function
	1	ON	Writing disabled for user program memory.
		OFF	Writing enabled for user program memory.
	2	ON	The user program is automatically transferred and executed when power is turned ON.
		OFF	The user program is automatically transferred but not executed when power is turned ON.
	3	---	Not used.
	4	ON	Use default peripheral port communications parameters.
		OFF	Use peripheral port communications parameters set in the PC Setup.
	5	ON	Use default RS-232C port communications parameters.
		OFF	Use RS-232C port communications parameters set in the PC Setup.
	6	ON	User-defined pin. Turns OFF the User DIP Switch Pin Flag (A39512).
		OFF	User-defined pin. Turns ON the User DIP Switch Pin Flag (A39512).
	7	ON	Writing data from the CPU Unit to the Memory Card or restoring data from the Memory Card to the CPU Unit.
		OFF	Verifying contents of Memory Card.
	8	OFF	Always OFF.

Note The display language for the Programming Console is not set on the DIP switch for CJ-series CPU Units, but rather is set using a Programming Console key sequence.

6-2 Details

Pin	Function	Setting		Description
1	Write-protection for user program memory (UM) (See note 1.)	ON	Write-protected	User program memory is write-protected when this pin is ON. Turn ON to prevent the program from being changed accidentally.
		OFF	Read/write	
2	Automatic transfer of the program at start-up	ON	Yes	The program (AUTOEXEC.OBJ) and PC Setup (AUTOEXEC.STD) will be transferred from the Memory Card to the CPU Unit automatically at start-up when this pin is ON. (See note 4.) A PC's software (program and PC Setup) can be completely initialized just by inserting a new Memory Card and turning on the power. This can be used to switch the system to a new arrangement very quickly. **Note** When pin 7 is ON and pin 8 is OFF, reading from the Memory Card for easy backup is given priority; even if pin 2 is ON, the program will not be automatically transferred.
		OFF	No	
3	Not used.	---	---	---
4	Peripheral port communications parameters	ON	Use parameters set in the PC Setup.	• Leave this pin OFF when using a Programming Console or CX-Programmer (peripheral bus setting) connected to the peripheral port. • Turn this pin ON when the peripheral port is being used for a device other than a Programming Console or CX-Programmer (peripheral bus setting).
		OFF (default)	Auto-detect Programming Device (See note 2.)	
5	RS-232C port communications parameters	ON	Auto-detect Programming Device (See note 3.)	• Leave this pin OFF when the RS-232C port is being used for a device other CX-Programmer (peripheral bus setting) such as a Programmable Terminal or host computer. • Turn this pin ON when using CX-Programmer (peripheral bus setting) connected to the RS-232C port.
		OFF (default)	Use parameters set in the PC Setup.	
6	User-defined pin	ON	A39512 ON	The ON/OFF status of this pin is reflected in A39512. Use this function when you want to create an Always-ON or Always-OFF condition in the program without using an Input Unit.
		OFF (default)	A39512 OFF	
7	Easy backup setting	ON	Writing from the CPU Unit to the Memory Card	Press and hold the Memory Card Power Supply Switch for three seconds.
			Restoring from the Memory Card to the CPU Unit.	To read from the Memory Card to the CPU Unit, turn ON the PC power. This operation is given priority over automatic transfer (pin 2 is ON) when power is ON.
		OFF (default)	Verifying contents of Memory Card.	Press and hold the Memory Card Power Supply Switch for three seconds.
8	Not used	OFF (default)	Always OFF.	

Note

1. The following data is write-protected when pin 1 is ON: the user program and all data in the parameter area such as the PC Setup and registered I/O table. Furthermore when pin 1 is ON, the user program and parameter area won't be cleared even when the memory clear operation is performed from a Programming Device.
2. The auto-detect goes through baud rates in the following order: Programming Console → Peripheral bus at 9,600 bps, 19,200 bps, 38,400 bps, and 115,200 bps. Programming Devices that aren't in peripheral bus mode and devices in peripheral bus mode operating at 51,200 bps will not be detected.

3. The auto-detect operation goes through baud rates in the following order: Peripheral bus at 9,600 bps, 19,200 bps, 38,400 bps, and 115,200 bps. Programming Devices that aren't in peripheral bus mode and devices in peripheral bus mode operating at any other speeds will not be detected.
4. When pin 2 is ON and the power is turned ON, any I/O Memory file (AUTOEXEC.IOM, ATEXEC□□.IOM) (refer to Section 12) will also be transferred automatically. Both the program (AUTOEXEC.OBJ) and the parameter area (AUTOEXEC.STD) must exist in the Memory Card. I/O Memory files (AUTOEXEC.IOM, ATEXEC□□.IOM) are optional.
5. A CJ1-H CPU Unit will remain in PROGRAM mode after the simple backup operation has been performed and cannot be changed to MONITOR or RUN mode until the power supply has been cycled. After completing the backup operation, turn OFF the power supply to the CPU Unit, change the settings of pin 7, and then turn the power supply back ON.

DIP switch settings		PC Setup settings								
		Peripheral port settings (Address 144 bits 8 to 11)				RS-232C port settings (Address 160 bits 8 to 11)				
		Default (0)	NT Link (2)	Peripheral bus (4)	Host Link (5)	Default (0)	NT Link (2)	No-protocol (3)	Peripheral bus (4)	Host Link (5)
Pin 4	OFF	Programming Console or CX-Programmer in peripheral bus mode (Auto-detect connected device's baud rate)				---				
	ON	Host computer or CX-Programmer in host link mode	PT (NT Link)	CX-Programmer in peripheral bus mode	Host computer or CX-Programmer in host link mode	---				
Pin 5	OFF	---				Host computer or CX-Programmer in host link mode	PT (NT Link)	Standard external device	CX-Programmer in peripheral bus mode	Host computer or CX-Programmer in host link mode
	ON	---				CX-Programmer in peripheral bus mode (Auto-detect connected device's baud rate)				

Note Use the following settings for the network on the CX-Programmer and pin 4 on the DIP switch when connecting the CX-Programmer via the peripheral or RS-232C port.

CX-Programmer network setting	Peripheral port connections	RS-232C port connection	PC Setup
Toolbus (peripheral bus)	Turn OFF pin 4.	Turn ON pin 5.	None
SYSMAC WAY (Host Link)	Turn ON pin 4.	Turn OFF pin 5.	Set to Host Link.

When CX-Programmer is set to host link mode, it won't be possible to communicate (go online) in the following cases:

- The computer is connected to the CPU Unit's peripheral port and pin 4 is OFF.
- The computer is connected to the CPU Unit's RS-232C port and pin 5 is ON.

To go online, set CX-Programmer to peripheral bus mode, turn pin 4 ON (turn pin 5 OFF for the RS-232C port), and set the communications mode to host link mode in the PC Setup.

SECTION 7
PC Setup

This section describes initial software settings made in the PC Setup.

7-1 PC Setup

7-1-1 Overview of the PC Setup

The PC Setup contains basic CPU Unit software settings that the user can change to customize PC operation. These settings can be changed from a Programming Console or other Programming Device.

The following table lists cases in which the PC Setup must be changed. In other cases, the PC can be operated with the default settings.

Cases when settings must be changed	Setting(s) to be changed
The input response time settings for CJ-series Basic I/O Units must be changed in the following cases: • Chattering or noise occur in Basic I/O Units. • Short pulse inputs are being received for intervals longer than the cycle time.	Basic I/O Unit Input Response Time
Data in all regions of I/O Memory (including the CIO Area, Work Areas, Timer Flags and PVs, Task Flags, Index Registers, and Data Registers) must be retained when the PC's power is turned on.	IOM Hold Bit Status at Startup
The status of bits force-set or force-reset from a Programming Device (including Programming Consoles) must be retained when the PC's power is turned on.	Forced Status Hold Bit Status at Startup
• You do not want the operating mode to be determined by the Programming Console's mode switch setting at startup. • You want the PC to go into RUN mode or MONITOR mode and start operating immediately after startup. • You want the operating mode to be other than PROGRAM mode when the power is turned ON.	Startup Mode
Detection of low-battery errors is not required when using battery-free operation.	Detect Low Battery
Detection of interrupt-task errors is not required.	Detect Interrupt Task Error
Data files are required but a Memory Card cannot be used or the files are written frequently. (Part of the EM Area will be used as file memory.)	EM File Memory
The peripheral port will not be used with the Programming Console or CX-Programmer (peripheral bus) communications speed auto-detection and will not used the default host link communications settings such as 9,600 bps. **Note** Pin 4 of the DIP switch on the front of the CPU Unit must be OFF to change the PC Setup settings.	Peripheral Port Settings
The RS-232C port will not be used with the Programming Console or CX-Programmer (peripheral bus) communications speed auto-detection and will not use the default host link communications settings such as 9,600 bps. **Note** Pin 5 of the DIP switch on the front of the CPU Unit must be OFF to change the PC Setup settings.	RS-232C Port Settings
You want to speed up communications with a PT via an NT Link.	Set the peripheral port or the RS-232C port communications port baud rate to "high-speed NT Link."
You want the intervals for scheduled interrupts to be set in units of 1 ms rather than 10 ms.	Scheduled Interrupt Time Units
You want CPU Unit operation to be stopped for instruction errors, i.e., when the ER Flag or AER Flag is turned ON. (You want instruction errors to be fatal errors.) You want to find the instructions where instruction errors are occurring (where the ER Flag is turning ON.	Instruction Error Operation
You want a minimum cycle time setting to create a consistent I/O refresh cycle.	Minimum Cycle Time
You want to set a maximum cycle time other than 1 second (10 ms to 40,000 ms).	Watch Cycle Time

Cases when settings must be changed	Setting(s) to be changed
You want to delay peripheral servicing so that it is executed over several cycles.	Fixed Peripheral Servicing Time
You want to give priority to servicing peripherals over program execution. Here, “peripherals” include CPU Bus Units, Special I/O Units, the built-in RS-232C port, and the peripheral port.	Peripheral Servicing Priority Mode
Performing special processing when power is interrupted.	Power OFF Interrupt Task
You want to delay the detection of a power interruption.	Power OFF Detection Delay Time
You want to execute IORF in an interrupt task. You want to shorten the average cycle time when a lot of Special I/O Units are being used. You want to extend the I/O refreshing interval for Special I/O Units.	Special I/O Unit Cyclic Refreshing
You want to improve both program execution and peripheral servicing response.	CPU Processing Mode (CJ1-H CPU Units only)
You do not want to record user-defined errors for FAL(006) and FPD(269) in the error log.	FAL Error Log Registration (CJ1-H CPU Units only)
You want to reduce fluctuation in the cycle time caused by text string processing	Background Execution for Table Data, Text String, and Data Shift Instructions (CJ1-H CPU Units only)
You do not want to wait for Units to complete startup processing to start CPU Unit operation.	Startup Condition (CJ1-H CPU Units only)

7-1-2 PC Setup Settings

All non-binary settings in the following tables are hexadecimal unless otherwise specified.

7-1-2-1 Startup Tab (on CX-Programmer)

Startup Hold Settings

Forced Status Hold Bit

Address in Programming Console		Settings	Function	Related flags and words	New setting’s effectiveness
Word	Bit(s)				
80	14	0: Cleared 1: Retained Default: 0	This setting determines whether or not the status of the Forced Status Hold Bit (A50013) is retained at startup. When you want all of the bits that have been force-set or force-reset to retain their forced status when the power is turned on, turn ON the Forced Status Hold Bit and set this setting to 1 (ON).	A50013 (Forced Status Hold Bit)	Takes effect at startup

IOM Hold Bit

Address in Programming Console		Settings	Function	Related flags and words	New setting’s effectiveness
Word	Bit(s)				
80	15	0: Cleared 1: Retained Default: 0	This setting determines whether or not the status of the IOM Hold Bit (A50012) is retained at startup. When you want all of the data in I/O Memory to be retained when the power is turned on, turn ON the IOM Hold Bit and set this setting to 1 (ON).	A50012 (IOM Hold Bit)	Takes effect at startup

Mode Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
81	---	Program: PROGRAM mode Monitor: MONITOR mode Run: RUN mode Use programming console: Programming Console's mode switch Default: Program	This setting determines whether the Startup Mode will be the mode set on the Programming Console's mode switch or the mode set here in the PC Setup. If this setting is PRCN and a Programming Console isn't connected, startup mode will be RUN mode.	---	Takes effect at startup

Execution Settings

Startup Condition (CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
83	15	0: Wait for Units. 1: Don't wait. Default: 0	To start the CPU Unit in MONITOR or PROGRAM mode even if there is one or more Units that has not completed startup processing, set this setting to 1 (Don't wait for Units). To wait for all Units to finish startup processing, set this setting to 0 (Wait for Units).	---	Takes effect at startup

Note This setting applies only to specific Units.

7-1-2-2 CPU Settings Tab (on CX-Programmer)

Execute Process

Detect Low Battery

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
128	15	0: Detect 1: Do not detect Default: 0	This setting determines whether CPU Unit battery errors are detected. If this setting is set to 0 and a battery error is detected, the ERR/ALM indicator on the CPU Unit will flash and the Battery Error Flag (A40204) will be turned ON, but CPU Unit operation will continue.	A40204 (Battery Error Flag)	Takes effect the next cycle

Detect Interrupt Task Error

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
128	14	0: Detect 1: Do not detect Default: 0	This setting determines whether interrupt task errors are detected. If this setting is set to 0 and an interrupt task error is detected, the ERR/ALM indicator on the CPU Unit will flash and the Interrupt Task Error Flag (A40213) will be turned ON, but CPU Unit operation will continue.	A40213 (Interrupt Task Error Flag)	Takes effect the next cycle

Stop CPU on Instruction Error (Instruction Error Operation)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
197	15	0: Continue 1: Stop Default: 0	This setting determines whether instruction errors (instruction processing errors (ER) and illegal access errors (AER)) are treated as non-fatal or fatal errors. When this setting is set to 1, CPU Unit operation will be stopped if the ER or AER Flags is turned ON (even when the AER Flag is turned ON for an indirect DM/EM BCD error). Related Flags: A29508 (Instruction Processing Error Flag) A29509 (Indirect DM/EM BCD Error Flag) A29510 (Illegal Access Error Flag)	A29508, A29509, A29510 (If this setting is set to 0, these flags won't be turned ON even if an instruction error occurs.)	Takes effect at the start of operation

Don't Register FAL to Error Log (User-defined FAL Error Storage, CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
129	15	0: Record user-defined FAL errors in error log. 1: Don't record user-defined FAL errors in error log. Default: 0	This setting determines if user-defined FAL errors created with FAL(006) and time monitoring for FPD(269) will be recorded in the error log (A100 to A199). Set it to 1 so prevent these errors from being recorded.	---	Whenever FAL(006) is executed (every cycle)

Memory Allocation Settings

EM File Setting Enabled

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
136	7	0: None 1: EM File Memory Enabled Default: 0	This setting determines whether part of the EM Area will be used for file memory.	---	After initialization from Programming Device or via FINS command.

EM Start File No. (Starting Memory Starting Bank)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
136	0 to 3	0 to 6 Default: 0	If bit 7 (above) is set to 1, the setting here specifies the EM bank where file memory begins. The specified EM bank and all subsequent banks will be used as file memory. This setting will be disabled if bit 7 is set to 0.	A344 (EM File Memory Starting Bank)	After initialization from Programming Device or via FINS command.

Background Execution Settings

Table Data Process Instructions (CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	15	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Table Data Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

String Data Process Instructions (CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	14	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Text String Data Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

Data Shift Process Instructions (CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	13	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Data Shift Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

Communications Port Number for Background Execution (CJ1-H CPU Units Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	0 to 3	0 to 7: Communications ports 0 to 7 (internal logical ports)	The communications port number (internal logical port) that will be used for background execution.	---	Start of operation

7-1-2-3 Timings Tab (on CX-Programmer)

Enable Watch Cycle Time Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
209	15	0: Default 1: Bits 0 to 14 Default: 0	Set to 1 to enable the Watch Cycle Time Setting in bits 0 to 14. Leave this setting at 0 for a maximum cycle time of 1 s.	A40108 (Cycle Time Too Long Flag)	Takes effect at the start of operation (Can't be changed during operation.)

Watch Cycle Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
209	0 to 14	001 to FA0: 10 to 40,000 ms (10-ms units) Default: 001 (1 s)	This setting is valid only when bit 15 of 209 is set to 1. The Cycle Time Too Long Flag (A40108) will be turned ON if the cycle time exceeds this setting.	A264 and A265 (Present Cycle Time)	Takes effect at the start of operation (Can't be changed during operation.)

Cycle Time (Minimum Cycle Time)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
208	0 to 15	0001 to 7D00: 1 to 32,000 ms (1-ms units) Default: 0000 (No minimum)	Set to 0001 to 7D00 to specify a minimum cycle time. If the cycle time is less than this setting, it will be extended until this time passes. Leave this setting at 0000 for a variable cycle time. (Can't be changed during operation.) This cycle time will apply to the program execution cycle when a parallel processing mode is used.	---	Takes effect at the start of operation

Scheduled Interrupt Interval

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
195	0 to 3	0: 10 ms 1: 1.0 ms Default: 0	This setting determines the time units used in scheduled interrupt interval settings. (This setting cannot be changed during operation.)	---	Takes effect at the start of operation

Power OFF Detection Time (Power OFF Detection Delay Time)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
225	0 to 7	00 to 0A: 0 to 10 ms (1-ms units) Default: 00	This setting determines how much of a delay there will be from the detection of a power interruption (approximately 10 to 25 ms for AC power and 2 to 5 ms for DC power after the power supply voltage drops below 85% of the rated value) to the confirmation of a power interruption. The default setting is 0 ms. When the power OFF interrupt task is enabled, it will be executed when the power interruption is confirmed. If the power OFF interrupt task is disabled, the CPU will be reset and operation will be stopped.	---	Takes effect at startup or at the start of operation. (Can't be changed during operation.)

Power OFF Interrupt Disable

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
225	15	0: Disabled 1: Enabled Default: 0	When this setting is set to 1, the power OFF interrupt task will be executed when power is interrupted.	---	Takes effect at startup or at the start of operation. (Can't be changed during operation.)

7-1-2-4 SIOU Refresh Tab (on CX-Programmer)

Special I/O Unit Cyclic Refreshing

Item	Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
	Word	Bit(s)				
Cyclic Refreshing of Units 0 to 15	226	0 to 15	0: Enabled 1: Disabled Default: 0	These settings determine whether data will be exchanged between the specified Unit and the Special I/O Unit's allocated words (10 words/Unit) during cyclic refreshing for Special I/O Units. Turn ON the corresponding bit to disable cyclic refreshing when the Unit will be refreshed in an interrupt task by IORF(097), several Special I/O Units are being used and you don't want to extend the cycle time, or the cycle time is so short that the Special I/O Unit's internal processing can't keep up. (Special I/O Units can be refreshed from the program with IORF(097).)	---	Takes effect at the start of operation
Cyclic Refreshing of Units 16 to 31	227	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 32 to 47	228	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 48 to 63	229	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 64 to 79	230	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 80 to 95	231	0 to 15	0: Enabled 1: Disabled Default: 0			

7-1-2-5 Unit Settings Tab (on CX-Programmer)

Basic I/O Unit Input (Rack) Response Times

Item	Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
	Word	Bit(s)				
Rack 0, Slot 0	10	0 to 7	00: 8 ms 10: 0 ms 11: 0.5 ms 12: 1 ms 13: 2 ms 14: 4 ms 15: 8 ms 16: 16 ms 17: 32 ms Default: 00 (8 ms)	Sets the input response time (ON response time = OFF response time) for CJ-series Basic I/O Units. The default setting is 8 ms and the setting range is 0 ms to 32 ms. This value can be increased to reduce the effects of chattering and noise, or it can be reduced to allow reception of shorter input pulses.	A220 to A259: Actual input response times for Basic I/O Units	Takes effect at startup
Rack 0, Slot 1		8 to 15				
Rack 0, Slot 2	11	0 to 7				
Rack 0, Slot 3		8 to 15				
Rack 0, Slot 4	12	0 to 7				
Rack 0, Slot 5		8 to 15				
Rack 0, Slot6	13	0 to 7				
Rack 0, Slot 7		8 to 15				
Rack 0, Slot 8	14	0 to 7				
Rack 0, Slot 9		8 to 15				
Rack 1, Slots 0 to 9	15 to 19	See Rack 0.				
Rack 2, Slots 0 to 9	20 to 24					
Rack 3, Slots 0 to 9	25 to 29					
Rack 4, Slots 0 to 9	30 to 34					
Rack 5, Slots 0 to 9	35 to 39					
Rack 6, Slots 0 to 9	40 to 44					
Rack 7, Slots 0 to 9	45 to 49					

7-1-2-6 Host Link Port Tab (on CX-Programmer)

The following settings are valid when pin 5 on the DIP switch on the CPU Unit is ON.

Host Link Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	15	0: Default (standard)* 1: PC Setup (custom) Default: 0	*The default settings are for 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
161	0 to 7	00: 9,600 bps 01: 300 bps 02: 600 bps 03: 1,200 bps 04: 2,400 bps 05: 4,800 bps 06: 9,600 bps 07: 19,200 bps 08: 38,400 bps 09: 57,600 bps 0A: 115,200 bps Default: 00	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Data Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	3	0: 7 bits 1: 8 bits Default: 0	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Stop Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	2	0: 2 bits 1: 1 bit Default: 0	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Parity

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	0 to 1	00: Even 01: Odd 10: None Default: 00	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	00: Host link 05: Host link Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05.) The Peripheral bus mode is for communications with Programming Devices other than the Programming Console.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Unit Number (for CPU Unit in Host Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
163	0 to 7	00 to 1F: (0 to 31) Default: 00	This setting determines the CPU Unit's unit number when it is connected in a 1-to-N (N=2 to 32) Host Link.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Settings

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	02: 1:N NT Link Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. **Note** Communications will not be possible with PTs set for 1:1 NT Links.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
161	0 to 7	00: Standard 0A: High-speed NT Link* Default: 00	* Set to 115,200 bps when setting this value from the CX-Programmer. To return to the standard setting, leave the setting set to "PC Setup" and set the baud rate to 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Max. (Maximum Unit Number in NT Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
166	0 to 3	0 to 7 Default: 0	This setting determines the highest unit number of PT that can be connected to the PC.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Peripheral Bus Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	15	0: Default (standard)* 1: PC Setup (custom) Default: 0	*The default settings are for a baud rate of 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	04: Peripheral bus Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05.) The Peripheral Bus mode is for communications with Programming Devices other than the Programming Console.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	**Bit(s)**				
161	0 to 7	00: 9,600 bps 06: 9,600 bps 07: 19,200 bps 08: 38,400 bps 09: 57,600 bps 0A: 115,200 bps Default: 00	Settings 00 and 06 through 0A are valid when the communications mode is set to peripheral bus.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

No-protocol Settings

Start Code/End Code

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	**Bit(s)**				
164	8 to 15	00 to FF Default: 00	Start code: Set this start code only when the start code is enabled (1) in bits 12 to 15 of 165.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)
	0 to 7	00 to FF Default: 00	End code: Set this end code only when the end code is enabled (1) in bits 8 to 11 of 165.		
165	12	0: None 1: Code in 164 Default: 0	Start code setting: A setting of 1 enables the start code in 164 bits 8 to 15.		
	8 to 9	0: None 1: Code in 164 2: CR+LF Default: 0	End code setting: With a setting of 0, the amount of data being received must be specified. A setting of 1 enables the end code in bits 0 to 7 of 164. A setting of 2 enables an end code of CR+LF.		
	0 to 7	00: 256 bytes 01 to FF: 1 to 255 bytes Default: 00	Set the data length to be sent and received with no-protocol communications. The end code and start code are not included in the data length. Set this value only when the end code setting in bits 8 to 11 of 165 is "0: None." This setting can be used to change the amount of data that can be transferred at one time by TXD(236) or RXD(235). The default setting is the maximum value of 256 bytes.		

Delay

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	**Bit(s)**				
162	0 to 15	0000 to 270F: 0 to 99990 ms (10-ms units) Default: 0000	This setting determines the delay from execution of TXD(236) until the data is actually transmitted from the specified port.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

7-1-2-7 Peripheral Port Tab (on CX-Programmer)

The following settings are valid when pin 4 on the DIP switch on the CPU Unit is ON.

Host Link Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	15	0: Default (standard)* 1: PC Setup (Custom) Default: 0	*The default settings are for 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
145	0 to 7	00: 9,600 bps 01: 300 bps 02: 600 bps 03: 1,200 bps 04: 2,400 bps 05: 4,800 bps 06: 9,600 bps 07: 19,200 bps 08: 38,400 bps 09: 57,600 bps 0A: 115,200 bps Default: 00	This setting is valid only when the communications mode is set to the Host Link mode. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Data Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	3	0: 7 bits 1: 8 bits Default: 0	These settings are valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Stop Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	2	0: 2 bits 1: 1 bit Default: 0	These settings are valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Parity

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	0 and 1	00: Even 01: Odd 10: None Default: 00	These setting is valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	00: Host Link 05: Host link Default: 0	This setting determines whether the peripheral port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05.) The peripheral bus mode is for communications with Programming Devices other than the Programming Console.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Unit Number (for CPU Unit in Host Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
147	0 to 7	00 to 1F (0 to 31) Default: 00	This setting determines the CPU Unit's unit number when it is connected in a 1-to-N (N=2 to 32) Host Link.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Settings

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	02: 1:N NT Link Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. **Note** Communications will not be possible with PTs set for 1:1 NT Links.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
145	0 to 7	00: Standard 0A: High-speed NT Link* Default: 00	* Set to 115,200 bps when setting this value from the CX-Programmer.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Max. (Maximum Unit Number in NT Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
150	0 to 3	0 to 7 Default: 0	This setting determines the highest unit number of PT that can be connected to the PC in NT Link mode.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Peripheral Bus Settings

Communications Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	15	0: Default (standard)* 1: PC Setup (custom) Default: 0	*The default settings are for a baud rate of 9,600 bps.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	4: Peripheral bus Default: 0	This setting determines whether the communications mode for the peripheral port. The peripheral bus mode is used for all Programming Devices except for Programming Consoles.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	0 to 7	00: 9,600 bps 06: 9,600 bps 07: 19,200 bps 08: 38,400 bps 09: 57,600 bps 0A: 115,200 bps Default: 00	The following settings are valid for the peripheral bus mode: 00 and 06 to 0A Hex.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

7-1-2-8 Peripheral Service Tab (CPU Processing Mode Settings)

Peripheral Service Mode (Peripheral Servicing Priority Mode)

Instruction Execution Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	08 to 15	00 05 to FF (Hex) Default: 00 (Hex)	00: Disable priority servicing 05 to FF: Time slice for instruction execution (5 to 255 ms in 1-ms increments)	A266 and A267	Takes effect at the start of operation (Can't be changed during operation.)

Peripheral Service Execution Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	00 to 07	00 to FF (Hex) Default: 00 (Hex)	00: Disable priority servicing 01 to FF: Time slice for peripheral servicing (0.1 to 25.5 ms in 0.1-ms increments)	A266 and A267	Takes effect at the start of operation (Can't be changed during operation.)

Target Units (Units for Priority Servicing)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
220	08 to 15	00 10 to 1F 20 to 2F E1 FC FD Default: 00	Up to five Units can be specified for priority servicing. 00: Disable priority servicing 10 to 1F: CPU Bus Unit unit number (0 to 15) + 10 (Hex) 20 to 2F: CJ-series Special I/O Unit unit number (0 to 96) + 20 (Hex) FC: RS-232C port FD: Peripheral port	---	Takes effect at the start of operation (Can't be changed during operation.)
	00 to 07				
221	08 to 15				
	00 to 07				
222	08 to 15				

Sync/Async Comms (Parallel Processing Modes)

The following setting is supported only by the CJ1-H CPU Units

Execution Mode (Parallel Processing Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	08 to 15	00 01 02 Default: 00	00: Not specified (disable parallel processing) 01: Synchronous (Synchronous Memory Access 02: Asynchronous (Asynchronous Memory Access)	---	Takes effect at the start of operation (Can't be changed during operation.)

Set Time to All Events (Fixed Peripheral Servicing Time)

Enable Fixed Servicing Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
218	15	0: Default* 1: Bits 0 to 7 Default: 0	Set to 1 to enable the fixed peripheral servicing time in bits 0 to 7. *Default: 4% of the cycle time	---	Takes effect at the start of operation (Can't be changed during operation.)

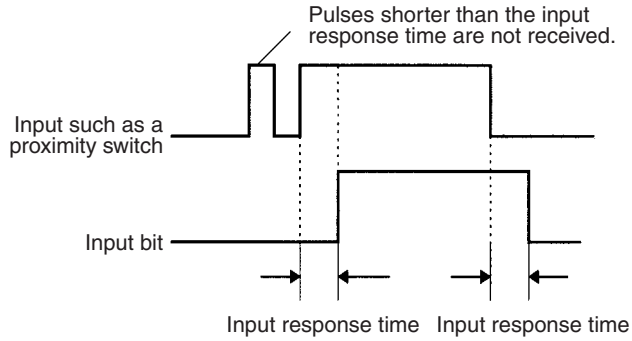
Fixed Servicing Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
218	0 to 7	00 to FF: 0.0 to 25.5 ms (0.1-ms units) Default: 00	Set the peripheral servicing time. This setting is valid only when bit 15 of 218 is set to 1.	---	Takes effect at the start of operation (Can't be changed during operation.)

7-2 Explanations of PC Setup Settings

Basic I/O Unit Input Response Time

The input response time can be set for Basic I/O Units by Rack and Slot number. Increasing this value reduces the effects of chattering and noise. Decreasing this value allows reception of shorter input pulses, (but do not set the ON response time or OFF response time to less than the cycle time).



The default setting for the input response time is 8 ms and the setting range is 0 to 32 ms. When the input response time is set to 0 ms, the only delay will be the delays in the Unit's internal elements. For information on the Unit's internal elements, refer to *Appendix A Specifications of Basic I/O Units and High-density I/O Units* and check the input response time for the Unit that you are using.

The input response time settings are transferred to the Basic I/O Units when the PC is turned ON.

When the Unit's settings are changed, they are stored in A220 to A259 (Actual Input Response Times for Basic I/O Units). When the settings in the PC Setup have been changed with the PC in PROGRAM mode, the PC Setup settings will differ from the actual settings in the Units. In this case, the values in A220 to A259 can be checked to see the input response times actually set in the Units.

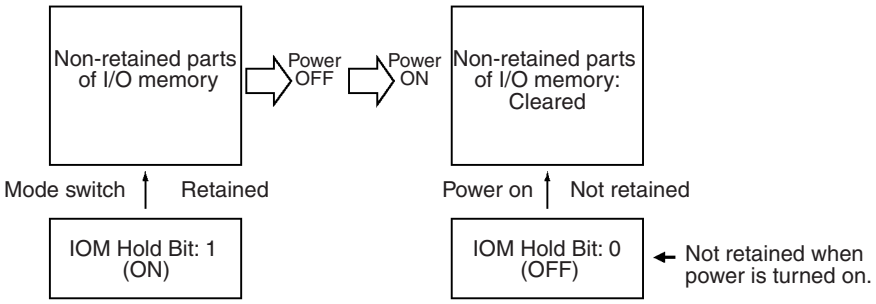
IOM Hold Bit Status at Startup

The IOM Hold Bit (A50012) can be turned ON to retain all of the data in I/O Memory when the CPU Unit's operating mode is switched between PROGRAM mode and RUN/MONITOR mode. When the PC is turned on, the IOM Hold Bit itself will be cleared (OFF) unless it is protected with this PC Setup setting.

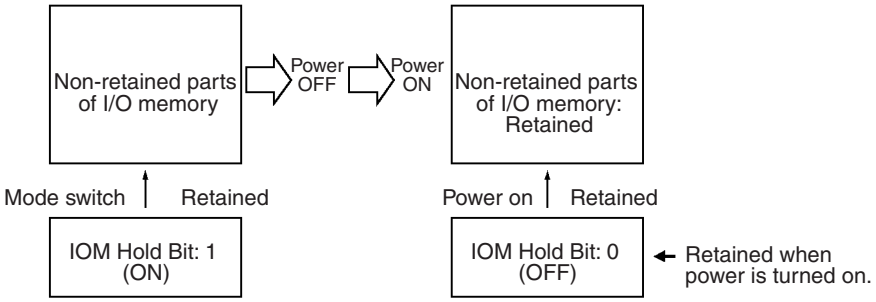
If the IOM Hold Bit Status at Startup setting is ON, the status of the IOM Hold Bit will be protected when the PC is turned on. If this setting is ON and the IOM Hold BIt itself is ON, all data in I/O memory will be retained when the PC is turned on.

Note If the backup battery fails or is disconnected, the IOM Hold Bit will be cleared whether this setting is ON or OFF.

OFF (0): IOM Hold Bit cleared at start-up



ON (1): IOM Hold Bit protected at start-up



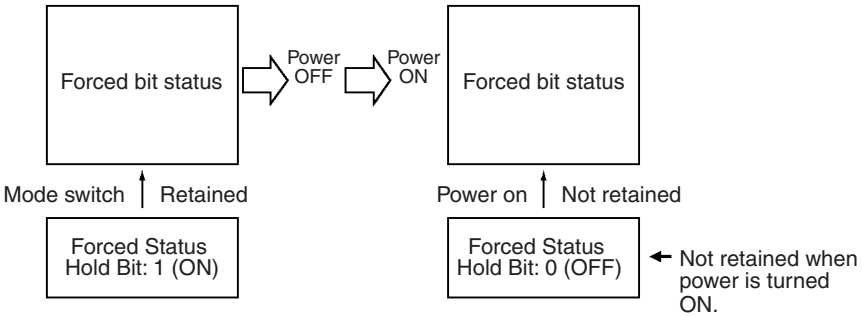
Forced Status Hold Bit at Startup

The Forced Status Hold Bit (A50013) can be turned ON to retain the forced status of all bits that have been force-set or force-reset when the CPU Unit's operating mode is switched between PROGRAM mode and RUN/MONITOR mode. When the PC is turned on, the Forced Status Hold Bit itself will be cleared (OFF) unless it is protected with this PC Setup setting.

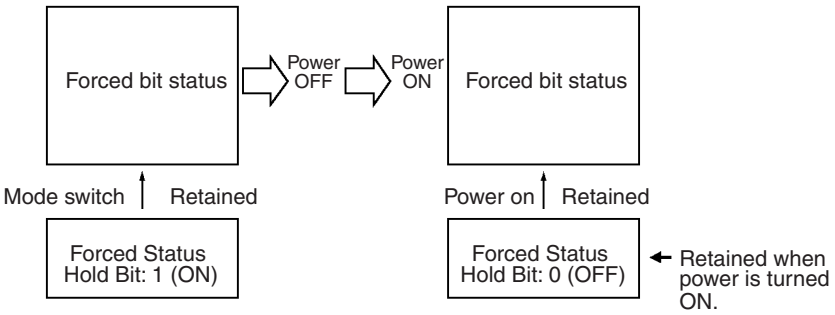
If the Forced Status Hold Bit at Startup setting is ON, the status of the Forced Status Hold Bit will be protected when the PC is turned on. If this setting is ON and the Forced Status Hold BIt itself is ON, all force-set and force-reset bits will retain their forced status when the PC is turned on.

Note If the backup battery fails or is disconnected, the Forced Status Hold Bit will be cleared whether this setting is ON or OFF.

OFF (0): Forced Status Hold Bit cleared at start-up



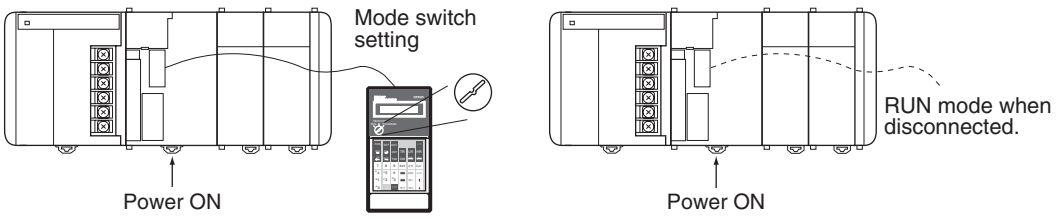
ON (1): Forced Status Hold Bit protected at start-up



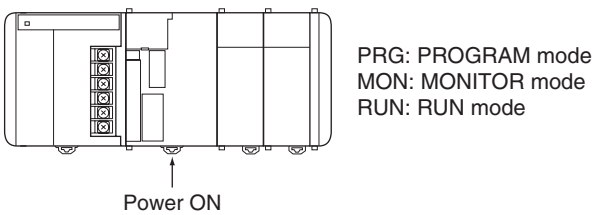
Startup Mode Setting This setting determines whether the startup mode will be the mode set on the Programming Console's mode switch or the mode set here in the PC Setup.

Note If this setting specifies the mode set on the Programming Console's mode switch (0) but a Programming Console isn't connected, the CPU Unit will automatically enter RUN mode at startup. (This differs from the default operation for CS-series CPU Units.)

PRCN: Programming Console's mode switch



Other: PC Setup's Startup Mode setting

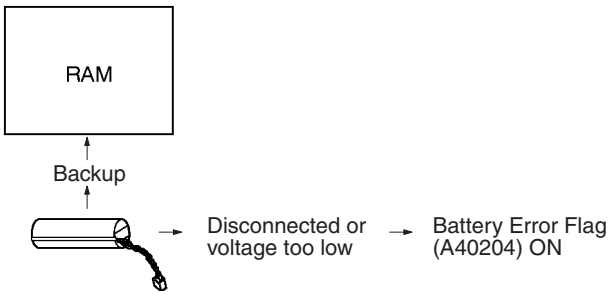


Detect Low Battery This setting determines whether CPU Unit battery errors are detected. Set the PC Setup so that battery errors are not detected when using battery-free operation. Refer to the *CS/CJ Series Programming Manual* for details.

If this setting is set to detect errors (0) and a battery error is detected, the Battery Error Flag (A40204) will be turned ON.

Note

1. The contents of the DM, EM, and HR Areas in the CPU Unit are not backed up to flash memory; they are backed up only by a Battery. If the Battery voltage drops, this data may be lost. Provide countermeasures in the program using the Battery Error Flag (A40204) to re-initialize data or take other actions if the Battery voltage drops
2. A battery error will be detected when the battery is disconnected or its voltage drops below the minimum allowed.



Detect Interrupt Task Error

If this setting is set to detect errors (0), an interrupt task error will be detected in the following cases:

- IORF(097) is executed in an interrupt task to refresh a Special I/O Unit's I/O while that Unit's I/O is being refreshed during cyclic refreshing.

EM File Memory Settings

These settings are used to convert part of the EM Area to file memory.

Programming Console

The specified EM bank and all subsequent banks will be set aside as file memory. Changing these settings using the Programming Console does not format the specified EM banks; the EM banks must be formatted with a Programming Device after changing these PC Setup settings. When formatting the EM banks with a Programming Console, refer to *7-2 Memory Card Format* in the *Programming Console Operation Manual* (W341-E1-1).

CX-Programmer

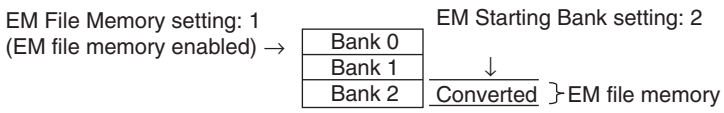
With the CX-Programmer, file memory will be formatted when file memory conversion and the number of banks to be converted is specified when transferring the PC Setup. (EM banks cannot be formatted as file memory unless they have been specified as file memory in the PC Setup.)

Once part of the EM Area has been formatted for use as file memory, it can be converted back to normal EM Area usage by changing these PC Setup settings back to their previous value and "un-formatting" the EM banks with a Programming Device.

Note

1. The actual starting file memory bank is stored in A344 (EM File Memory Starting Bank). When the settings in the PC Setup have been changed but the EM Area hasn't been formatted, the PC Setup setting will differ from the actual file memory setting in the EM Area. In this case, the values in A344 can be checked to see the actual file memory setting.
2. The EM Area cannot be formatted if the current EM bank is one of the banks that is being converted to file memory.

The following example shows EM bank 2 converted to file memory.

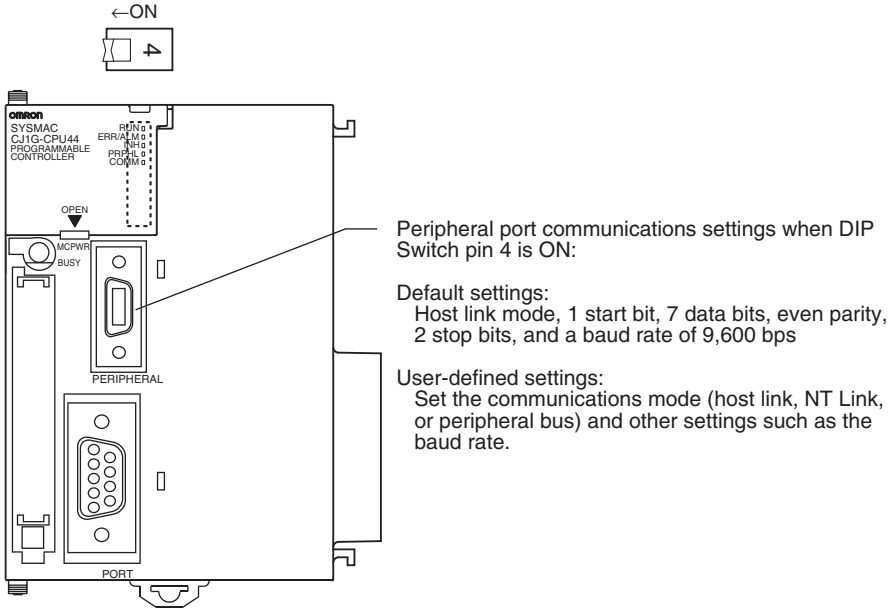


Peripheral Port Settings

These settings are effective only when pin 4 of the DIP switch on the front of the CPU Unit is ON.

The default settings for the peripheral port are: host link mode, 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps. Set the peripheral port settings in the PC Setup when you need to change these settings.

Note When pin 4 of the DIP switch on the front of the CPU Unit is OFF, the CPU Unit automatically detects the communications parameters of a connected Programming Device (including Programming Consoles). Those automatically detected parameters are not stored in the PC Setup.



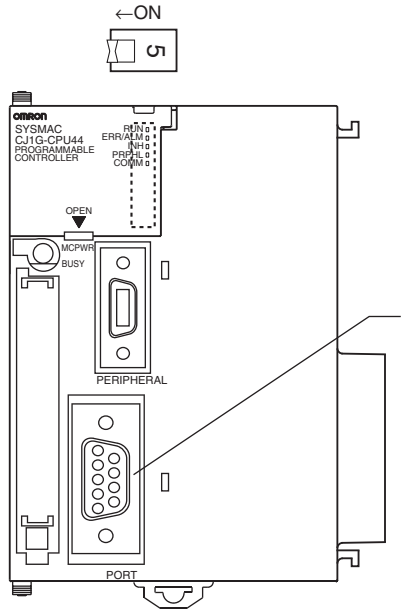
RS-232C Port Settings

These settings are effective only when pin 5 of the DIP switch on the front of the CPU Unit is OFF.

The default settings for the RS-232C port are: host link mode, 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps. Set the RS-232C port settings in the PC Setup when you need to change these settings. Specify the frame format when no-protocol mode is selected.

The RS-232C port settings can also be changed with STUP(237). The RS-232C Port Settings Changing Flag (A61902) is turned ON when STUP(237) is executed and it is turned OFF when the RS-232C port settings have been changed.

Note When pin 5 of the DIP switch on the front of the CPU Unit is ON, the CPU Unit automatically detects the communications parameters of a Programming Device (including Programming Consoles) connected to the RS-232C port. Those automatically detected parameters are not stored in the PC Setup.



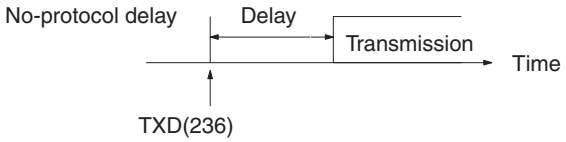
RS-232C port communications settings when DIP switch pin 5 is OFF:

Default settings:
Host link mode, 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps

User-defined settings:
Set the communications mode (host link, NT Link, no-protocol*, or peripheral bus) and other settings such as the baud rate.

*See notes 1 and 2 for details on no-protocol mode.

Note 1. A no-protocol transmission delay (address 162) can be set in no-protocol mode. The operation of this delay is shown in the following diagram.



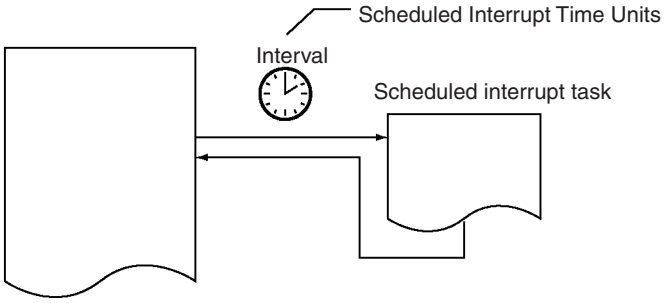
2. The following table shows the message formats that can be set for transmissions and receptions in no-protocol mode. The format is determined by the start code (ST) and end code (ED) settings. (From 1 to 256 bytes can be received in no-protocol mode.)

Start code setting	End code setting		
	None	Yes	CR+LF
None	DATA	DATA+ED	DATA+CR+LF
Yes	ST+DATA	ST+DATA+ED	ST+DATA+CR+LF

Scheduled Interrupt Time Units

This setting determines the time units for the scheduled interrupt interval settings. Set the scheduled interrupt interval from the program with MSKS(690).

Note This setting cannot be changed while the CPU Unit is in RUN or MONITOR mode.



Instruction Error Operation

This setting determines whether instruction execution errors are treated as non-fatal (0) or fatal errors (1). A program error will be generated as an instruction error if any of the following flags is turned ON.

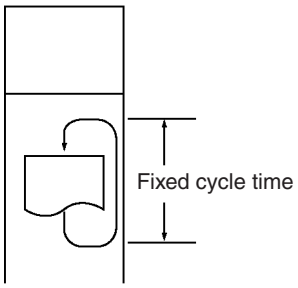
Instruction error flag	Address	Cause
Instruction Processing Error Flag	A29508	The ER Flag was turned ON.
Indirect DM/EM BCD Error Flag	A29509	The contents of a DM/EM word wasn't BCD when BCD was required for indirect addressing.
Illegal Access Error Flag	A29510	Attempted to access part of memory that is off-limits from the program.

If this setting is OFF (0), PC operation will continue after one of these errors. If this setting is ON (1), PC operation will stop after one of these errors.

Minimum Cycle Time

Set the minimum cycle time to a non-zero value to eliminate inconsistencies in I/O responses. This setting is effective only when the actual cycle time is shorter than the minimum cycle time setting. If the actual cycle time is longer than the minimum cycle time setting, the actual cycle time will remain unchanged.

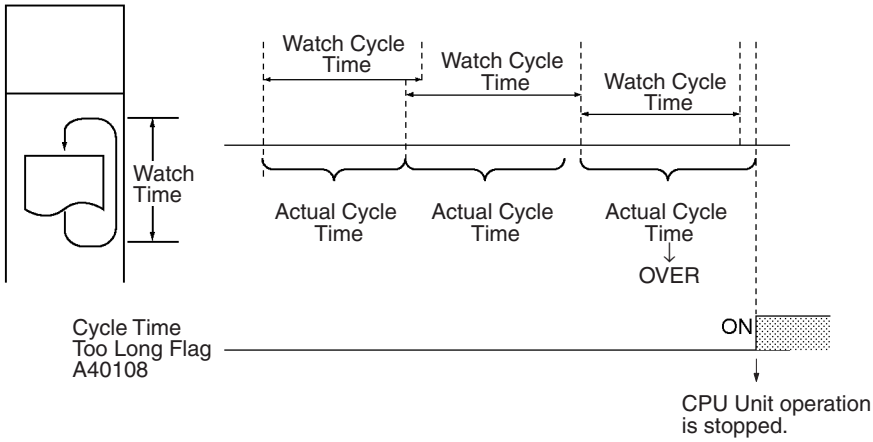
Note The minimum cycle time setting cannot be changed while the CPU Unit is in RUN or MONITOR mode.



Watch Cycle Time

If the cycle time exceeds the watch (maximum) cycle time setting, the Cycle Time Too Long Flag (A40108) will be turned ON and PC operation will be stopped. This setting must be changed if the normal cycle time exceeds the default watch cycle time setting of 1 s.

Note The watch cycle time setting cannot be changed while the CPU Unit is in RUN or MONITOR mode.



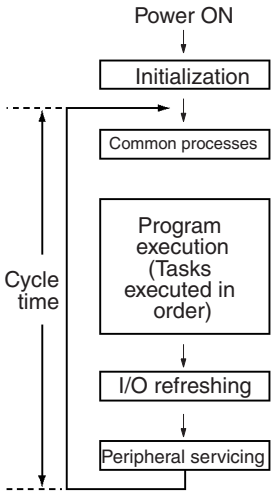
Note The default value for the watch cycle time is 1 s (1,000 ms).

Fixed Peripheral Servicing Time

This setting determines whether the peripheral servicing for the following processes is performed with the default settings (4% of the cycle time) or all together in a fixed servicing time.

Exchange data with Special I/O Units when necessary
Exchange data with CPU Bus Units when necessary
Exchange data with peripheral port
Exchange data with serial communications ports
Service file access operations (Memory Card)

Peripheral servicing is performed at the end of the cycle, just after I/O refreshing.



The following table shows a breakdown of the peripheral servicing time.

Peripheral servicing time	Default value	Setting range
Event service time for Special I/O Units	4% of the previous cycle's cycle time	Uniform servicing time in ms: 0.0 to 25.5 ms in 0.1-ms units
Event service time for CPU Bus Units	Same as above.	
Event service time for peripheral port	Same as above.	
Event service time for RS-232C port	Same as above.	
File access service time for Memory Card	Same as above.	

The default value for each servicing process is 4% of the last cycle's cycle time.

In general, we recommend using the default value. Set a uniform servicing time only when peripheral servicing is being delayed because each service process is being spread over several cycles.

Note

1. When the peripheral servicing time is set to a time longer than the default value, the cycle time will also be longer.
2. The fixed peripheral servicing time setting cannot be changed while the CPU Unit is in RUN mode or MONITOR mode.
3. Use the Peripheral Servicing Priority Mode to give priority to servicing peripheral over program execution.

Power OFF Interrupt Task

This setting determines whether or not a power OFF interrupt task will be executed when a power interruption is detected. (When this setting is set to 0, the regular program will just stop when a power interruption is detected.)

The power OFF interrupt task will be stopped when the power hold time (processing time after power interrupt + power OFF detection delay time) has elapsed. The maximum power hold time is 10 ms.

When a power OFF detection delay time has to be set, be sure that the power OFF interrupt task can be executed in the available time (10 ms – power OFF detection delay time).

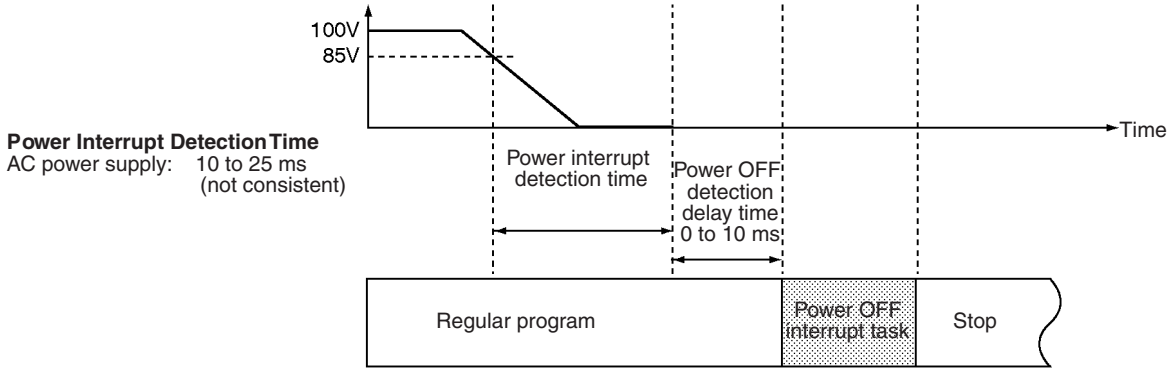
Note The power OFF interrupt task setting cannot be changed while the CPU Unit is in RUN mode or MONITOR mode.

Power OFF Detection Delay Time

This setting determines how much of a delay there will be from the detection of a power interruption (approximately after the power supply voltage drops below 85% of the rated value) until a power interruption is established and the regular program is stopped. The setting can be between 0 and 10 ms.

It takes a maximum of 10 ms for the internal 5-V DC power supply to drop to 0 V DC after the initial power interrupt detection time. Extend the time until detection of a power interruption when momentary interruptions in a bad power supply are causing PC operation to stop.

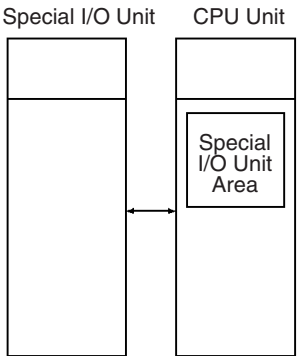
Note The power OFF detection delay time setting cannot be changed while the CPU Unit is in RUN mode or MONITOR mode.



Note The execution time for the power OFF interrupt task must be less than the maximum time available, namely: 10 ms – power OFF detection delay time. Refer to *10-3 Power OFF Operation* for details on CPU Unit operation when power is turned OFF.

Special I/O Unit Cyclic Refreshing

When a Special I/O Unit will be refreshed in an interrupt task by IORF(097), always disable cyclic refreshing for that Unit with this setting. The expected results will not be achieved and the Interrupt Task Error Flag (A40213) will be turned ON if IORF(097) is executed in an interrupt task during normal I/O refreshing.



These settings determine whether or not data will be exchanged with the 10 words allocated to each Special I/O Unit in the Special I/O Unit Area during cyclic I/O refreshing.

Note Whenever disabling a Special I/O Unit's cyclic refreshing, be sure that the I/O for that Unit is refreshed with IORF(097) in the program at least every 11 seconds during operation. A CPU Unit service monitoring error will occur in the Special I/O Unit if it is not refreshed every 11 seconds.

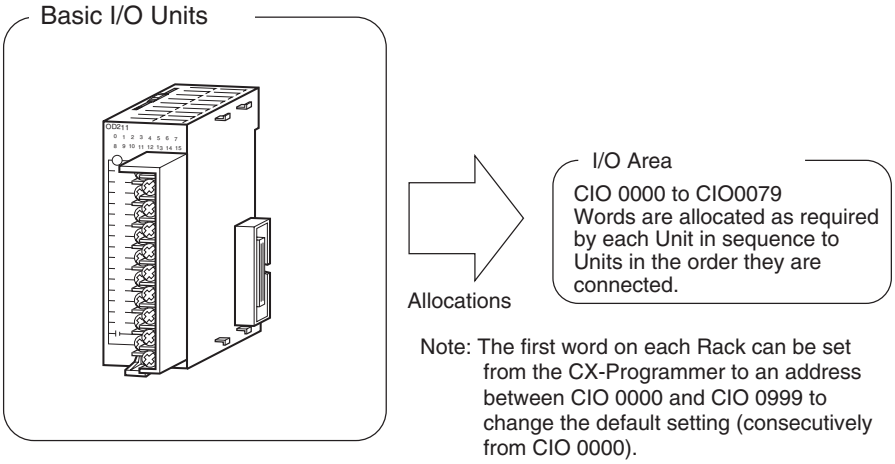
SECTION 8
I/O Allocations and Data Exchange

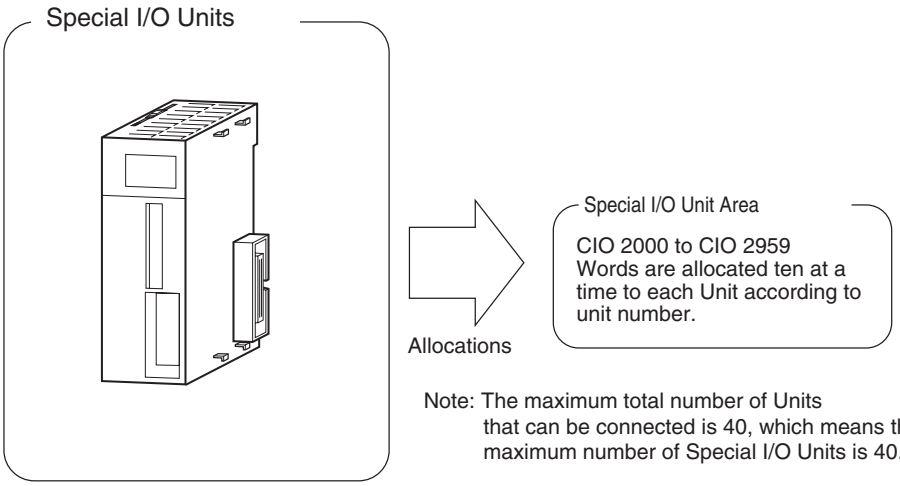
This section describes I/O allocations to Basic I/O Units and CPU Bus Units and data exchange with CPU Bus Units.

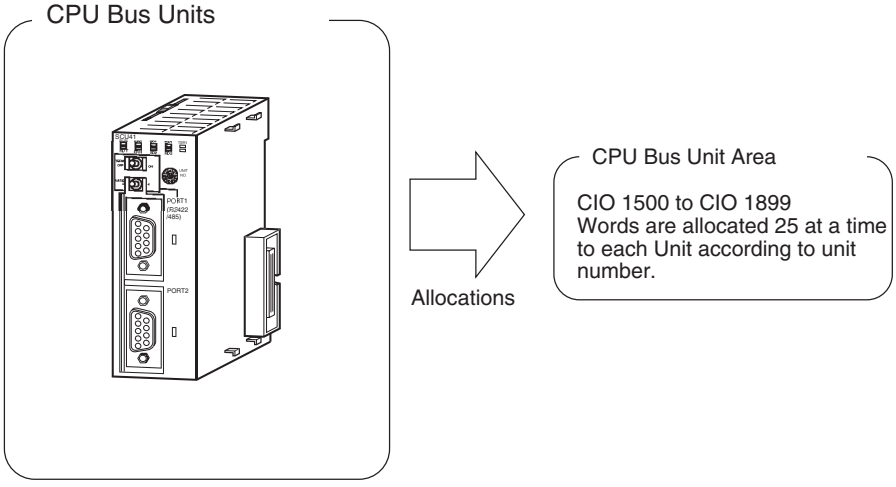
8-1 I/O Allocations

In CJ-series PCs, part of the I/O memory is allocated to each Unit. Memory is allocated differently to Basic I/O Units, Special I/O Units, and CJ-series CPU Bus Units.

8-1-1 Basic I/O Units







8-1-2 I/O Allocation to Basic I/O Units

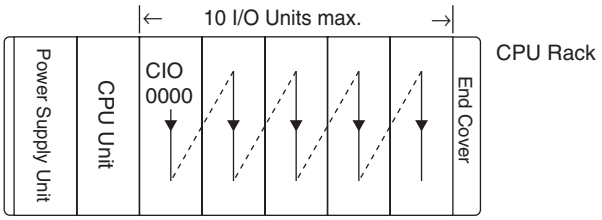
CJ-series Basic I/O Units are allocated words in the I/O Area (CIO 0000 to CIO 0079) and can be mounted to the CPU Rack or Expansion Racks.

Note Refer to *2-4 I/O Units* for list of specific Basic I/O Units.

Basic I/O Units on the CPU Rack

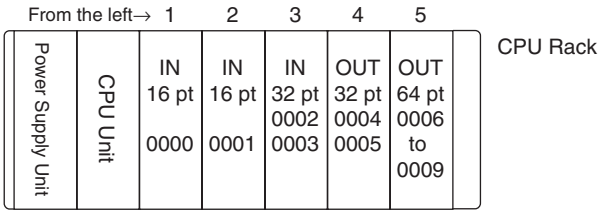
Basic I/O Units on the CPU Rack are allocated words from left to right starting with the Unit closest to the CPU Unit. Each Unit is allocated as many words as it requires.

Note Units that have 1 to 16 I/O points are allocated16 bits and Units that have 17 to 32 I/O points are allocated 32 bits. For example, an 8-point Unit is allocated 16 bits (1 word) and bits 00 to 07 of that word are allocated to the Unit's 8 points.



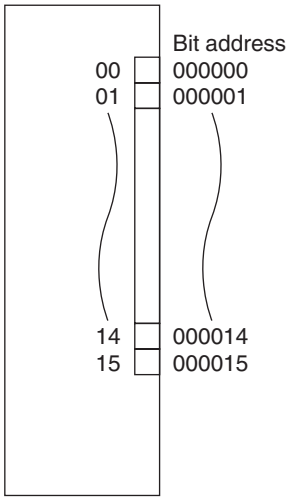
Example 1

The following example shows the I/O allocation to 5 Basic I/O Units in the CPU Rack.

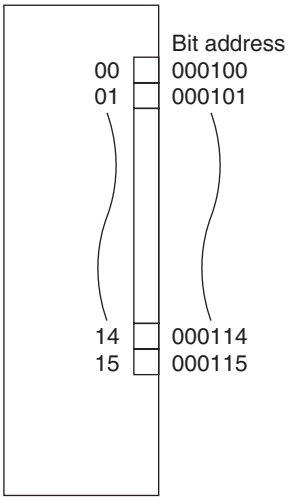


Position to left of CPU Unit	Unit	Words required	Words allocated
1	CJ1W-ID211 16-point DC Input Unit	1	CIO 0000
2	CJ1W-ID211 16-point DC Input Unit	1	CIO 0001
3	CJ1W-ID231 32-point DC Input Unit	2	CIO 0002 and CIO 0003
4	CJ1W-OD231 32-point Transistor Output Unit	2	CIO 0004 and CIO 0005
5	CJ1W-OD261 64-point Transistor Output Unit	4	CIO 0006 to CIO 0009

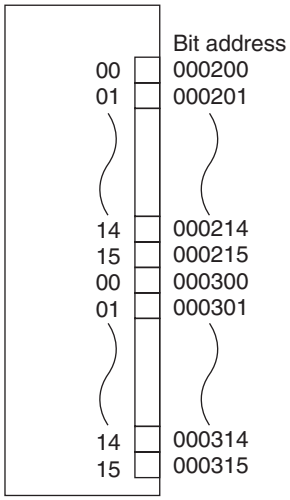
Position 1
16-point DC Input Unit



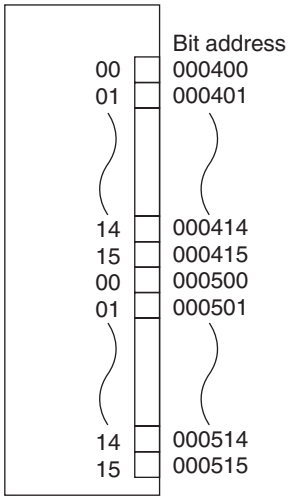
Position 2
16-point DC Input Unit



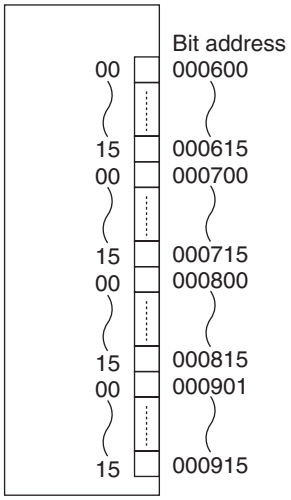
Position 3
32-point DC Input Unit



Position 4
32-point Transistor Output Unit



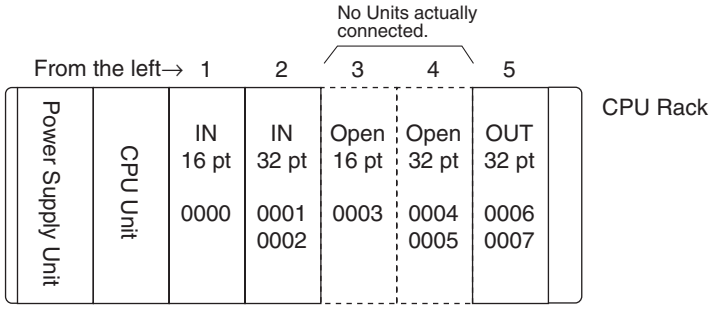
Position 5
64-point Transistor Output Unit



Example 2

With the CJ-series PCs, Dummy Units are not required to reserve unused words. Unused words are reserved by creating I/O tables on the CX-Programmer containing virtual Dummy Units and then downloading the I/O tables to the CPU Unit. Refer to *8-1-7 I/O Table Registration* for details.

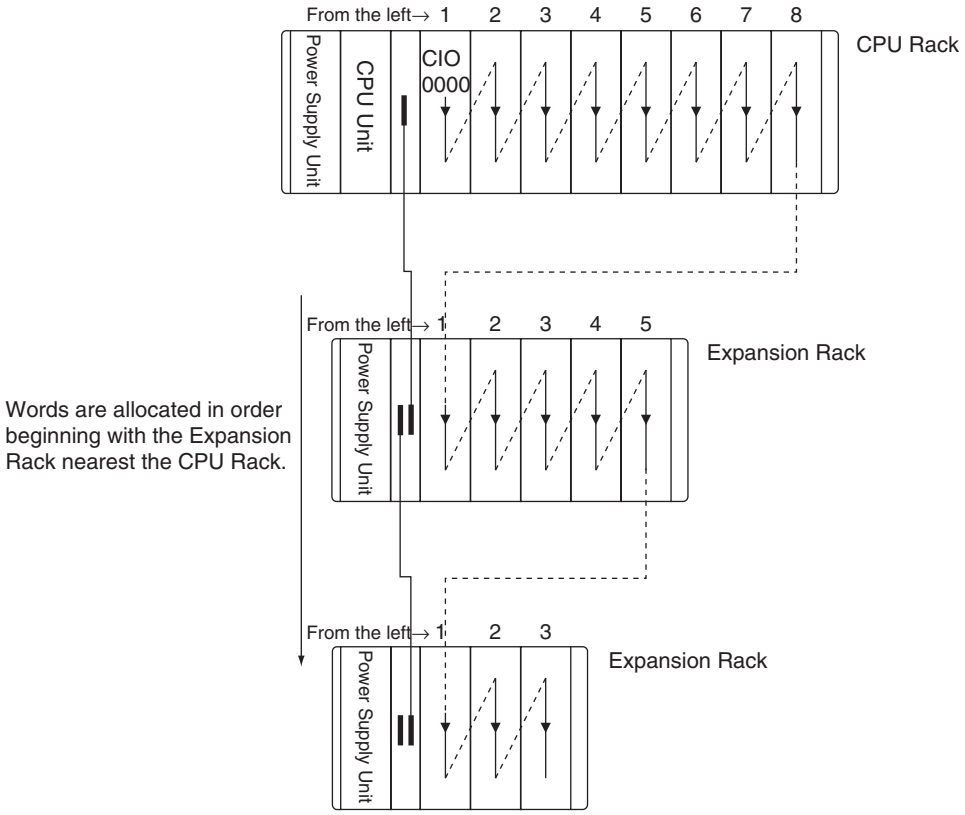
The following example shows the I/O allocation to 3 Basic I/O Units in the CPU Rack with unused empty slot.



Position to left of CPU Unit	Unit	Words required	Words allocated
1	CJ1W-ID111 16-point DC Input Unit	1	CIO 0000
2	CJ1W-ID231 32-point DC Input Unit	2	CIO 0001 and CIO 0002
3	Unused (created in I/O table on CX-Programmer)	1	CIO 0003
4	Unused (created in I/O table on CX-Programmer)	2	CIO 0004 and CIO 0005
5	CJ1W-OD231 32-point Transistor Output Unit	2	CIO 0006 and CIO 0007

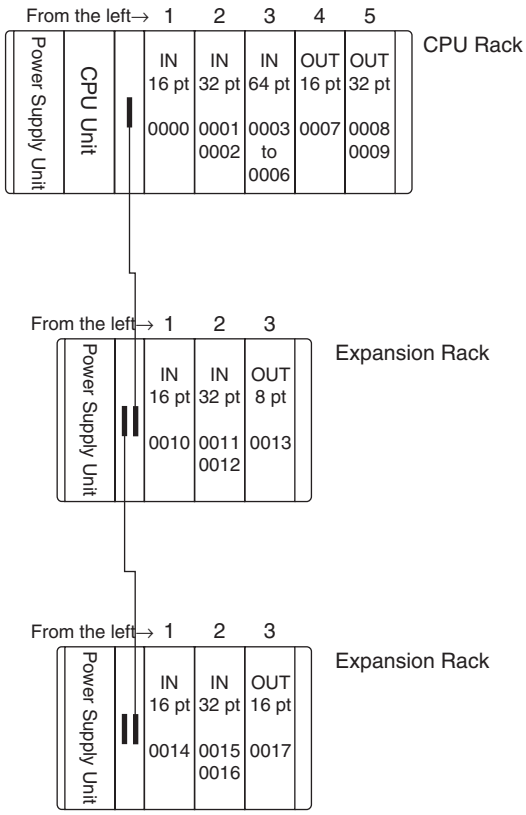
Basic I/O Units in Expansion Racks

I/O allocation to Basic I/O Units continues from the CJ-series CPU Rack to the CJ-series Expansion Rack connected to the CJ-series CPU Rack. Words are allocated from left to right and each Unit is allocated as many words as it requires, just like Units in the CJ-series CPU Rack.



Example

The following example shows the I/O allocation to Basic I/O Units in the CPU Rack and two CJ-series Expansion Racks.

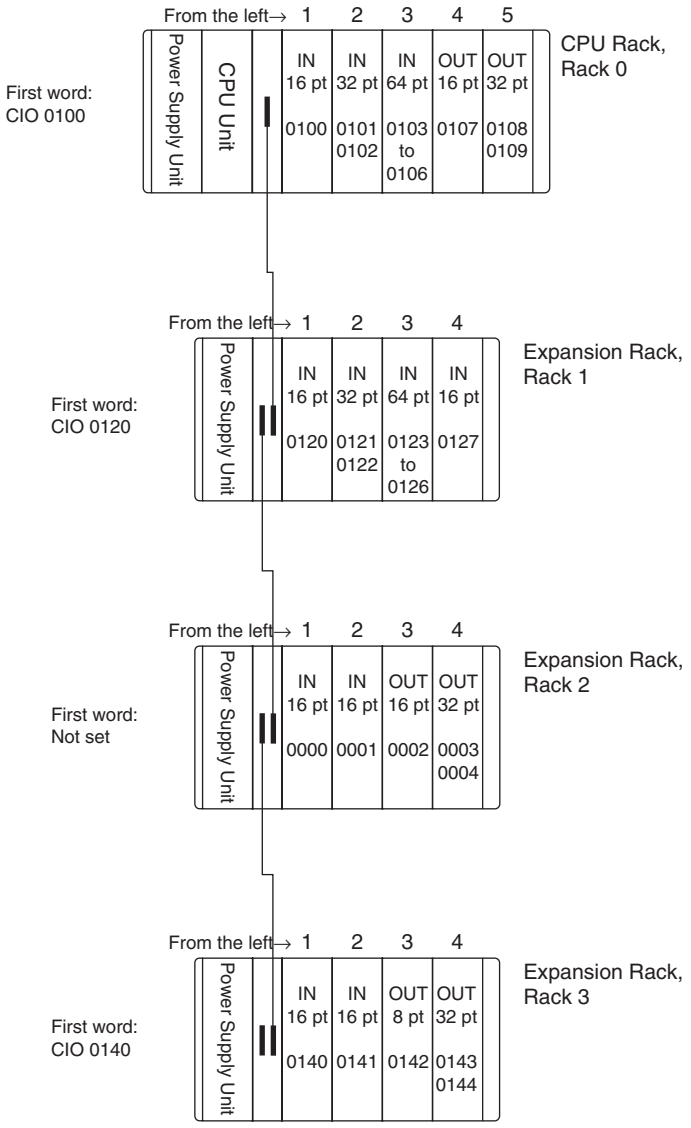


Rack	Position to left of CPU Unit	Unit	Words required	Words allocated
CPU Rack	1	CJ1W-ID211 16-point DC Input Unit	1	CIO 0000
	2	CJ1W-ID231 32-point DC Input Unit	2	CIO 0001 and CIO 0002
	3	CJ1W-ID261 64-point DC Input Unit	4	CIO 0003 to CIO 0006
	4	CJ1W-OD211 16-point Transistor Output Unit	1	CIO 0007
	5	CJ1W-OD231 32-point Transistor Output Unit	2	CIO 0008 and CIO 0009
Expansion Rack	1	CJ1W-ID211 16-point DC Input Unit	1	CIO 0010
	2	CJ1W-ID231 32-point DC Input Unit	2	CIO 0011 and CIO 0012
	3	CJ1W-OC201 8-point Relay Output Unit	1	CIO 0013
Expansion Rack	1	CJ1W-ID211 16-point DC Input Unit	1	CIO 0014
	2	CJ1W-ID231 32-point DC Input Unit	1	CIO 0015 and CIO 0016
	3	CJ1W-OC211 16-point Relay Output Unit	1	CIO 0017

8-1-3 Allocating the First Word for Each Rack

The first word allocated on each Rack can be set by creating I/O tables from the CX-Programmer. Rack numbers 0 to 3 are determined by the order the Racks are connected by the I/O Connecting Cables. (The CPU Rack is always rack 0 and the Expansion Racks are numbered in order from 1 to 3.) The rack numbers must be in the order that the Racks are connected.

For Racks for which the first word has been set, words are allocated from the specified first words to Units in the order that the Units are mounted (from left to right) For Racks in which the first word has not been set, words are allocated in order of rack number (lowest to highest) from CIO 0000. An example of setting the first word for Racks is shown below.



Setting First Rack Words from the CX-Programmer

The first word allocated on each Rack can be set from the CX-Programmer. This setting is not possible from a Programming Console.

Note For CJ1-H CPU Units, an indication of whether or not the first rack words have been set will be displayed on a Programming Console.

Use the following procedure to set the first rack words.

1,2,3...

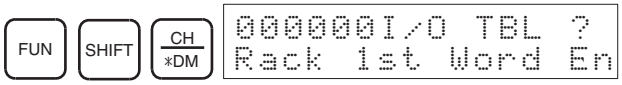
1. Select the ***Rack Start Address*** from the Option Menu on the I/O Table Window.
2. In the dialog box that will appear, remove the checkmarks from the settings disabling the first rack word settings and set the address of the first words for the CPU Rack and Expansion Racks (1 to 7).
3. Click the **OK** Button.

Confirming First Rack Word Settings on a Programming Console

With a CJ1-H CPU Unit, the Programming Console can be used to check whether or not the first word has been set on a Rack. Use the following procedure.

1,2,3...

1. Press the **FUN**, **SHIFT**, and **CH** Keys to start the I/O table creation operation. If the first work for a Rack has been set, a message saying so will appear on the second line of the display.



   If nothing is displayed, then the first word has not been set.
2. Press the **CHG** Key, enter the password (9713), and then press the **WRITE** Key to continue creating the I/O tables, or press the **CLR** Key to cancel the operation and return to the initial display.

Note

1. I/O words are not allocated to the I/O Control Unit or I/O Interface Units.
2. Be sure to make first word settings so that allocated words do not overlap. The first word setting for a rack can be any address from CIO 0000 to CIO 0900. If a word is allocated to two Racks or the first word setting exceeds CIO 0900, the corresponding Expansion Rack Number Duplication Flags (A40900 to A40903: Racks 0 to 3) and the Duplication Error Flag (A40113) will be turned ON
3. Always create I/O tables when setting the first word for one or more Racks. The correct words will not be allocated without use-set I/O tables.
4. The CJ-series PCs do not use Backplanes, so empty slots cannot be left for future expansion. To allow for future expansion, allocate virtual Dummy Units in the I/O tables from the CX-Programmer and download the I/O tables to the CPU Unit. If this is performed, Unit can later be added to the PC for actual application.
5. If the actual system configuration is changed after registering the I/O table so that the number of words or I/O type does not match the I/O table, an I/O setting error (A40110) will occur. A CPU Bus Unit Setting Error (A40203) or Special I/O Unit Setting Error (A40202) may occur as well.
6. When a Unit is removed, words can be reserved for the missing Unit using the I/O Table Change Operation. If a Unit is changed or added, all of the words in the program following that Unit's allocated words will be changed and the I/O Table Registration Operation will have to be performed again.
7. The first word settings for the Racks will be cleared when the I/O tables are deleted from the CX-Programmer.

8-1-4 Reserving I/O Words for Expected Changes

If the system configuration will be changed at a later date, changes to the program can be minimized by reserving I/O words in advance for future Unit changes or additions. To reserve I/O words, change the I/O table with CX-Programmer.

The following procedure can be used to create and download I/O tables. The I/O tables are first created offline on the CX-Programmer and then downloaded from the CX-Programmer to the CPU Unit. Refer to the *CX-Programmer User Manual* and the *CX-Server User Manual* for details.

1,2,3...

1. Open the I/O table window.
2. Allocate the required Units to slots.
3. For each slot for which unused words are to be reserved, allocate a Dummy Unit.
4. Check the I/O tables.
5. Go online with the CPU Unit and download the I/O tables. Downloading the I/O tables will change the CPU Unit PC Setup setting to operating according to use-set I/O tables.

Note You can first generate the I/O tables automatically for the CJ-series PC, upload them to the CX-Programmer, and then edit them before downloading them again to the CPU Unit to same input time.

8-1-5 I/O Allocation to Special I/O Units

Each CJ-series Special I/O Unit is allocated ten words in the Special I/O Unit Area (CIO 2000 to CIO 2959) according the unit number set on the Unit. Special I/O Units can be mounted to the CJ-series CPU Rack or CJ-series Expansion Racks.

Refer to *2-4 I/O Units* for more details on the available Special I/O Units.

Word Allocations

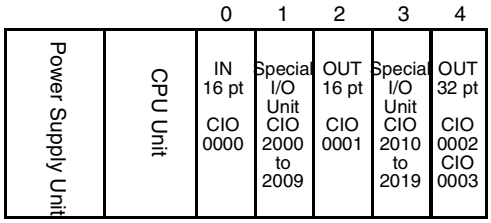
The following table shows which words in the Special I/O Unit Area are allocated to each Unit.

Unit number	Words allocated
0	CIO 2000 to CIO 2009
1	CIO 2010 to CIO 2019
2	CIO 2020 to CIO 2029
:	:
15	CIO 2150 to CIO 2159
: :	: :
95	CIO 2950 to CIO 2959

Special I/O Units are ignored during I/O allocation to Basic I/O Units. Positions containing Special I/O Units aren't allocated any words in the I/O Area.

Example

The following example shows the I/O word allocation to Basic I/O Units and Special I/O Units in the CPU Rack.



Slot	Unit	Words required	Words allocated	Unit number	Group
0	CJ1W-ID211 16-point DC Input Unit	1	CIO 0000	---	Basic I/O Unit
1	CJ1W-AD081 Analog Input Unit	10	CIO 2000 to CIO 2009	0	Special I/O Unit
2	CJ1W-OD211 16-point Transistor Output Unit	1	CIO 0001	---	Basic I/O Unit
3	CJ1W-TC001 Temperature Control Unit	20	CIO 2010 to CIO 2029	1	Special I/O Unit
4	CJ1W-OD231 32-point Transistor Output Unit	2	CIO 0002 and CIO 0003	---	Basic I/O Unit

8-1-6 I/O Allocation to CPU Bus Units

Each CJ-series CPU Bus Unit is allocated 25 words in the CPU Bus Unit Area (CIO 1500 to CIO 1899) according the unit number set on the Unit. CJ-series CPU Bus Units can be mounted to the CJ-series CPU Rack or CJ-series Expansion Racks.

Word Allocation

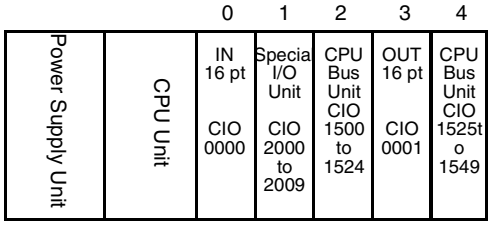
The following table shows which words in the CJ-series CPU Bus Unit Area are allocated to each Unit.

Unit number	Words allocated
0	CIO 1500 to CIO 1524
1	CIO 1525 to CIO 1549
2	CIO 1550 to CIO 1574
:	:
15	CIO 1875 to CIO 1899

CPU Bus Units are ignored during I/O allocation to Basic I/O Units. Positions containing CJ-series CPU Bus Units aren't allocated any words in the I/O Area.

Example

The following example shows the I/O word allocation to Basic I/O Units, Special I/O Units, and CPU Bus Units in the CPU Rack.

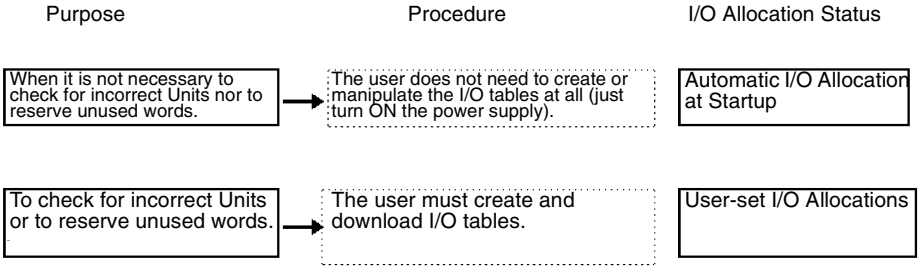


Slot	Unit	Words required	Words allocated	Unit number	Group
0	CJ1W-ID211 16-point DC Input Unit	1	CIO 0000	---	Basic I/O Unit
1	CJ1W-AD081 Analog Input Unit	10	CIO 2000 to CIO 2009	0	Special I/O Unit
2	CJ1W-SCU41 Serial Communications Unit	25	CIO 1500 to CIO 1524	0	CPU Bus Unit

Slot	Unit	Words required	Words allocated	Unit number	Group
3	CJ1W-OD211 16-point Transistor Output Unit	1	CIO 0001	---	Basic I/O Unit
4	CJ1W-CLK21 Controller Link Unit	25	CIO 1525 to CIO 1549	1	CPU Bus Unit

8-1-7 I/O Table Registration

I/O tables must be registered to recognize connected Units and allocate I/O. With a CJ-series CPU Unit, there are two ways in which the I/O tables can be registered. These are related to the I/O allocation status setting in the CPU Unit.



Automatic I/O Allocations at Startup

■ **Purpose**

If there is no need to check for incorrect Units or reserve unused words, the default setting can be used to automatically allocate I/O at startup (i.e., the same system as the CQM1 or CQM1H).

■ **Method**

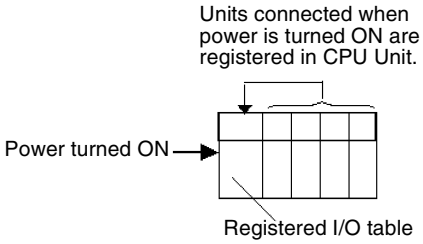
I/O tables will be created automatically according to the Units connected to the Rack each time the power supply is turned ON.

■ **Procedure**

This is the default method and there is no special procedure required. Just assemble the Units, turn ON the power supply, and clear memory from a Programming Device. As long as I/O tables are not downloaded to the CPU Unit, this method will then be used whenever the CPU Unit is turned ON.

■ **Unit Check**

When this method is used, no checking will be performed to confirm that the registered I/O tables agree with the actual I/O.



Note I/O tables created automatically when power is turned ON can be uploaded to the CX-Programmer and edited.

User-set I/O Allocations

■ Purpose

I/O tables can be set by the user if it is necessary to check for incorrect Units or to reserve unused words (i.e., the same system as the CS-series PCs).

■ Method

I/O tables are created by the user and written to the CPU Unit.

■ Procedure

Create the I/O tables from a Programming Device or create them on the CX-Programmer and downloaded them to the CPU Unit. Thereafter, this method will then be used whenever the CPU Unit is turned ON. There are three specific methods that can be used to achieve this.

- Create the I/O tables from a Programming Console or CX-Programmer.
- Edit the I/O tables on the CX-Programmer and download them to the CPU Unit.
- Transfer a parameter file (.STD) to the CPU Unit (including automatically writing the file from a Memory Card at startup).

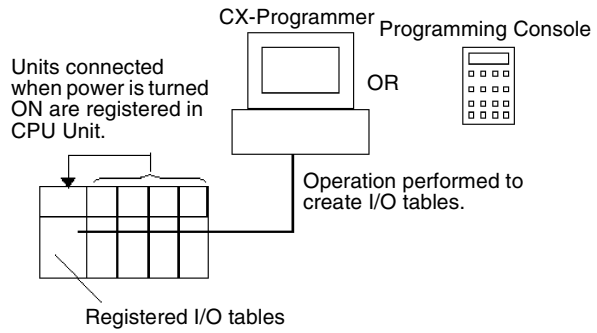
Once implemented, this method will be used until the I/O tables are deleted from the CPU Unit using the CX-Programmer.

■ Unit Check

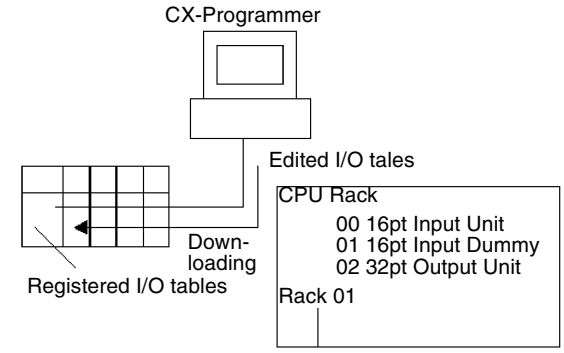
When this method is used, the registered I/O tables are compared with the actual I/O at startup. If they do not agree, A40110 will turn ON to indicate an I/O setting error and operation will not be possible.

■ User Procedures for Creating I/O Tables

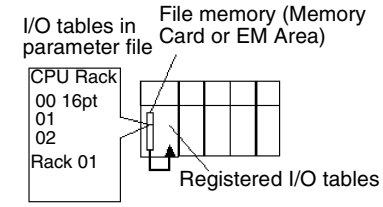
Creating I/O Tables



Editing and Downloading I/O Tables



Transferring Parameter File to CPU Unit

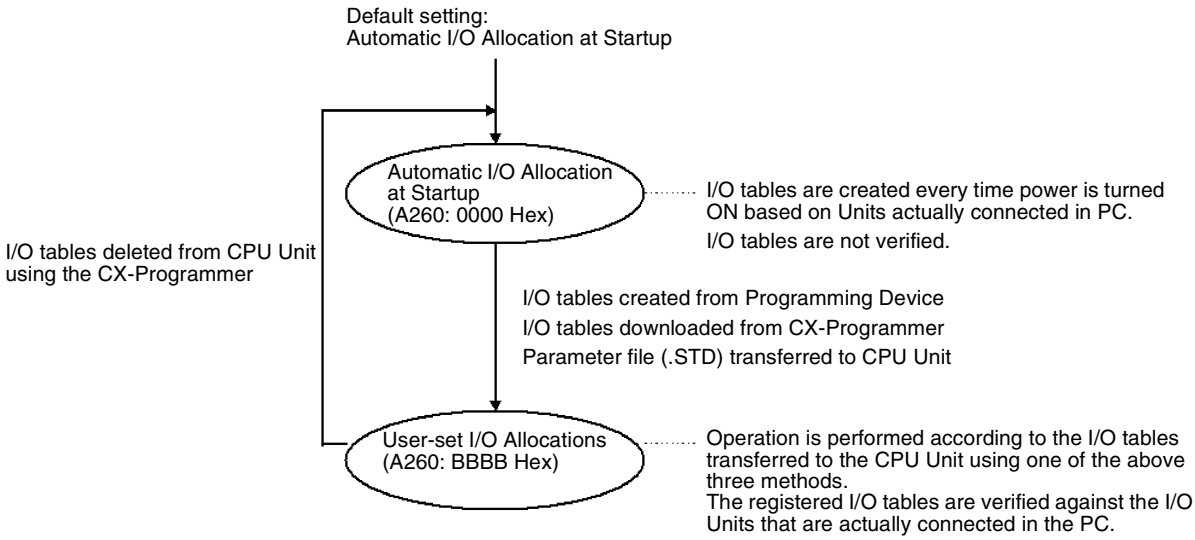


Checking I/O Allocation Status

The I/O allocation status can be checked in A260. If A260 contain 0000 Hex, automatic I/O allocation at startup is being used. If A260 contains BBBB Hex, user-set I/O allocations are being used.

Address	Name	Contents
A260	I/O Allocations Status	0000 Hex: Automatic I/O Allocation at Startup BBBB Hex: User-set I/O Allocation

Changes in I/O Allocation Status



You cannot return to automatic I/O allocation at startup by using the Programming Console. To return to automation I/O allocation, the I/O tables must be deleted from the CPU Unit using the CX-Programmer. When the I/O tables are deleted, all settings for first words for Racks will also be deleted.

Procedures for Registering I/O Tables

I/O Table Registration with CX-Programmer

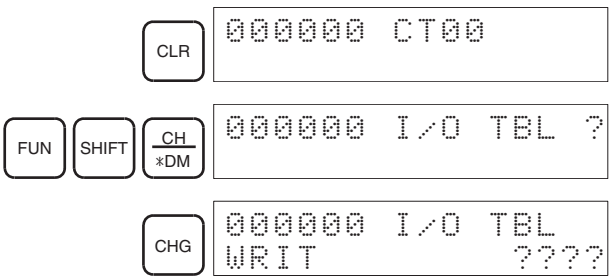
Use the following procedure to register the I/O table with the CX-Programmer.

1,2,3...

1. Double-click ***I/O Table*** in the project tree in the main window. The I/O Table Window will be displayed.
2. Select ***Options*** and then ***Create***. The models and positions of the Units mounted to the Racks will be written to the CPU Unit as the registered I/O tables.

I/O Table Registration with a Programming Console

Use the following procedure to register the I/O table with a Programming Console.



8-1-8 Detailed Information on I/O Table Creation Errors

With a CJ1-H CPU Unit, the contents of A261 will provide information on the Unit causing the error whenever one occurs when creating the I/O tables from the Programming Console or CX-Programmer. This information will make it easier to find the Unit causing the problem with troubleshooting I/O tables. Refer to *SECTION 11 Troubleshooting* for actual procedures.

Name	Address		Contents	When changing to RUN mode	At startup	Setting timing
	Word	Bit				
CPU Bus Unit Setup Area Initialization Error Flag	A261	00	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	Held	Cleared	When I/O tables are created
I/O Overflow Flag		02	ON: Overflow in maximum number of I/O points. Turns OFF when I/O tables are generated normally.			
Duplication Error Flag		03	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.			
I/O Bus Error Flag		04	ON: I/O bus error Turns OFF when I/O tables are generated normally.			
Special I/O Unit Error Flag		07	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.			
I/O Unconfirmed Error Flag		09	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.			

8-2 Data Exchange with CPU Bus Units

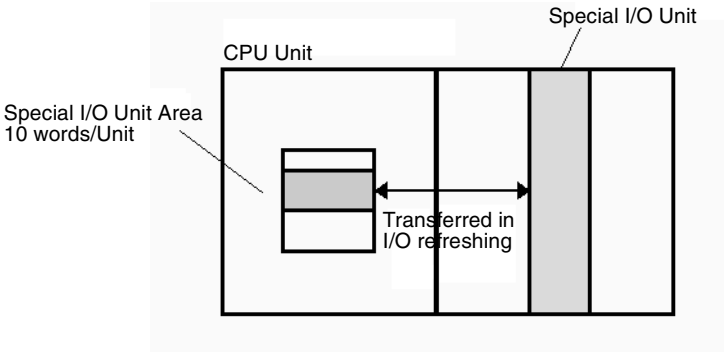
This section describes how data can be exchanged between Special I/O Units or CPU Bus Units, and the CPU Unit.

8-2-1 Special I/O Units

Special I/O Unit Area (I/O Refreshing)

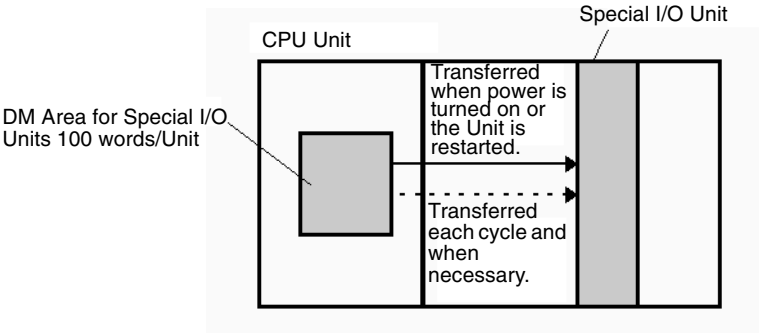
Data is exchanged each cycle during I/O refreshing of the Special I/O Unit Area. Basically, 10 words are allocated to each Special I/O Unit based on its unit number setting. Refer to the operation manuals for individual Special I/O Units for details.

The Special I/O Unit Area ranges from CIO 2000 to CIO 2959 (10 words × 96 Units).



DM Area

Each Special I/O Unit is allocated 100 words in the DM Area in the range of D20000 to D29599 (100 words × 96 Units). These 100 words are generally used to hold initial settings for the Special I/O Unit. When the contents of this area are changed from the program to reflect a change in the system, the Restart Bits for affected Units must be turned ON to restart the Units.



There are three times that data may be transferred through the words allocated to each Unit. The timing of data transfers depends on the model being used.

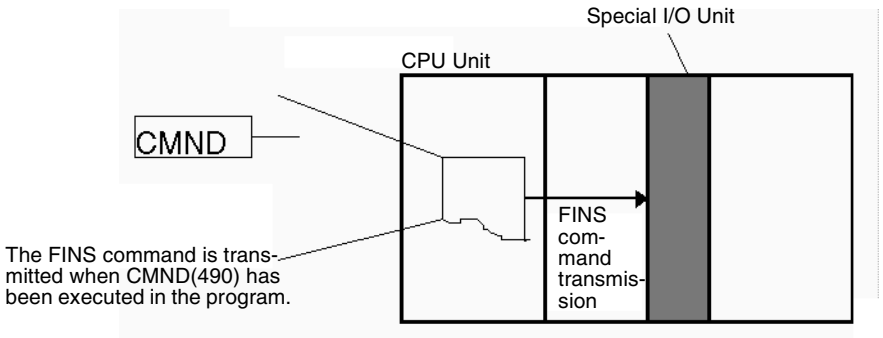
1,2,3...

1. Data transferred when the PC is turned ON.
2. Data transferred when the Unit is restarted.
3. Data transferred when necessary.

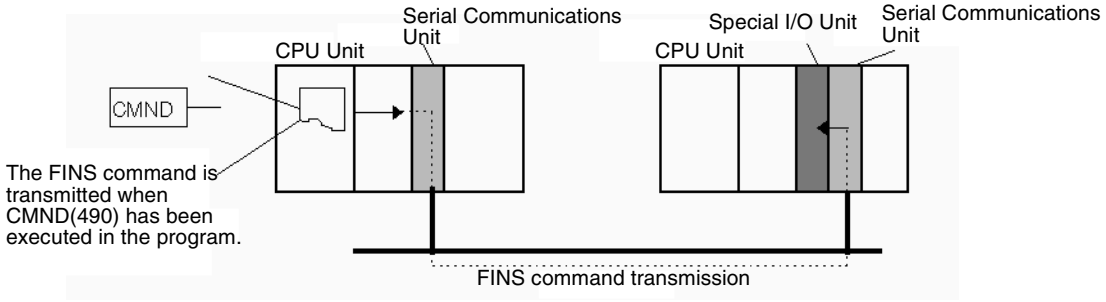
Some models transfer data in both directions, from the DM Area to the Unit and from the Unit to the DM Area. See the Unit's Operation Manual for details on data transfers.

FINS Commands

The CMND(490) instruction can be added to the ladder program to issue a FINS command to the Special I/O Unit.



FINS commands can be transmitted to Special I/O Units in other PCs in the network, not just the local PC.



Special I/O Unit Initialization

Special I/O Units are initialized when the PC's power is turned on or the Unit's Restart Bit is turned ON. The Unit's Special I/O Unit Initialization Flag (A33000 to A33515) will be ON while the Unit is initializing.
I/O refreshing (cyclic I/O refreshing or refreshing by IORF(097)) will not be performed for a Special I/O Unit while its Initialization Flag is ON.

Disabling Special I/O Unit Cyclic Refreshing

Ten words are allocated to each Special I/O Unit in the Special I/O Unit Area (CIO 2000 to CIO 2959) based on the unit number set on the front of each Unit. The data in the Special I/O Unit Area is refreshed in the CPU Unit every cycle during I/O refreshing (just after execution of the END(001) instruction).

I/O refreshing may take too long if too many Special I/O Units are installed. If I/O refreshing is taking too much time, the PC Setup can be set to disable cyclic refreshing for particular Special I/O Units. (The Special I/O Unit Cyclic Refreshing Disable Bits are in PC Setup addresses 226 to 231.)

If the I/O refreshing time is too short, the Unit's internal processing will not be able to keep pace, the Special I/O Unit Error Flag (A40206) will be turned ON, and the Special I/O Unit may not operate properly. In this case, the cycle time can be extended by setting a minimum cycle time in the PC Setup or cyclic I/O refreshing with the Special I/O Unit can be disabled. When cyclic refreshing has been disabled, the Special I/O Unit's data can be refreshed during program execution with IORF(097).

Note

1. Always disable a Special I/O Unit's cyclic refreshing if the Unit's I/O will be refreshed in an interrupt task with IORF(097). An interrupt task error (A40213) will occur if cyclic refreshing and IORF(097) refreshing are performed simultaneously.
2. Whenever disabling a Special I/O Unit's cyclic refreshing, be sure that the I/O for that Unit is refreshed with IORF(097) in the program at least every 11 seconds during operation. A CPU Unit service monitoring error will occur in the Special I/O Unit if it is not refreshed every 11 seconds.

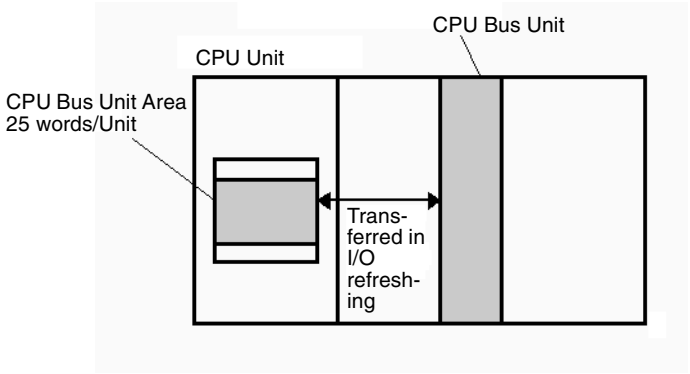
8-2-2 CPU Bus Units

Data can be exchanged between CPU Bus Units and the CPU Unit through the CPU Bus Unit Area, the DM Area, or FINS commands.

CPU Bus Unit Area (I/O Refreshing)

Data is exchanged each cycle during I/O refreshing of the CPU Bus Unit Area. Basically, 25 words are allocated to each CPU Bus Unit based on its unit number setting. The number of words actually used by the CPU Bus Unit varies.

The Special I/O Unit Area ranges from CIO 1500 to CIO 1899 (25 words × 16 Units).



Note With CJ1-H CPU Units, the CPU BUS I/O REFRESH instruction (DLNK(226)) can be executed in the ladder program to refresh the CIO Area words allocated to the CPU Bus Unit of a specified unit number.

DM Area

Each CPU Bus Unit is allocated 100 words in the DM Area in the range of D30000 to D31599 (100 words × 16 Units). There are three times that data may be transferred through the words allocated to each Unit. The timing of data transfers depends on the model being used.

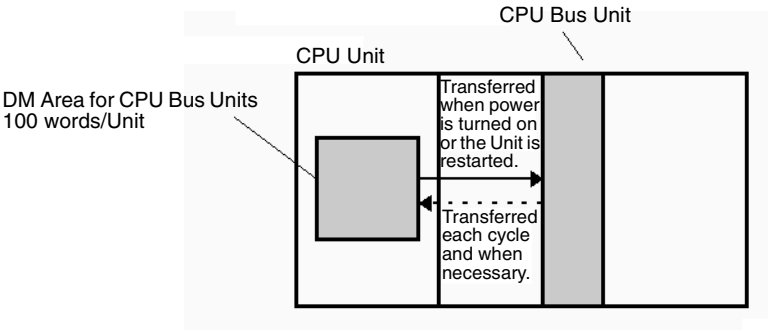
1,2,3...

1. Data transferred when the PC is turned ON.
2. Data transferred each cycle.
3. Data transferred when necessary.

Note With CJ1-H CPU Units, the CPU BUS I/O REFRESH instruction (DLNK(226)) can be executed in the ladder program to refresh the DM Area words allocated to the CPU Bus Unit of a specified unit number.

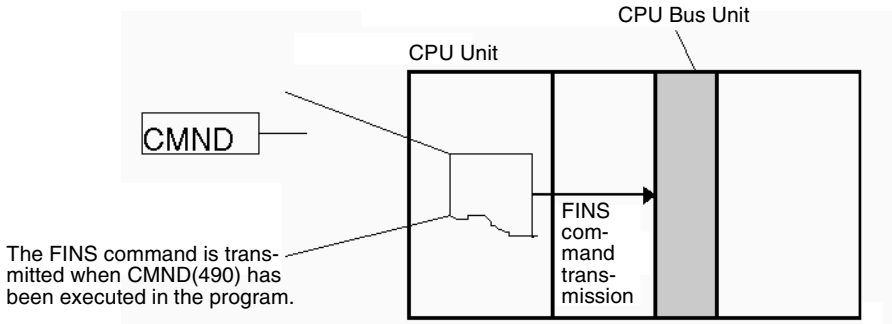
Some models transfer data in both directions, from the DM Area to the Unit and from the Unit to the DM Area. See the Unit's Operation Manual for details on data transfers.

These 100 words are generally used to hold initial settings for the CPU Bus Unit. When the contents of this area are changed from the program to reflect a change in the system, the Restart Bits (A50100 to A50115) for affected Units must be turned ON to restart the Units.

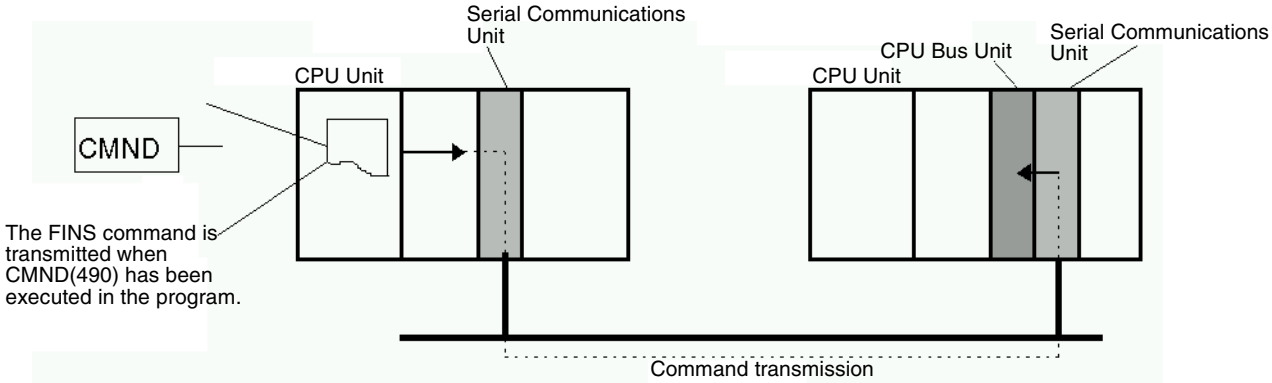


FINS Commands

The CMND(490) instruction can be added to the ladder program to send a FINS command to the CPU Bus Unit.



FINS commands can be transmitted to CPU Bus Units in other PCs in the network, not just the local PC.



CPU Bus Unit Initialization

CPU Bus Units are initialized when the PC's power is turned on or the Unit's Restart Bit is turned ON. The Unit's CPU Bus Unit Initialization Flag (A30200 to A30215) will be ON while the Unit is initializing.

Cyclic I/O refreshing will not be performed for aCPU Bus Unit while its Initialization Flag is ON.

SECTION 9
Memory Areas

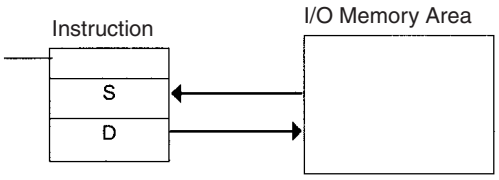
This section describes the structure and functions of the I/O Memory Areas and Parameter Areas.

9-1 Introduction

The CPU Unit's memory (RAM with battery back-up) can be divided into three parts: the User Program Memory, I/O Memory Area, and Parameter Area. This section describes the I/O Memory Area and Parameter Area.

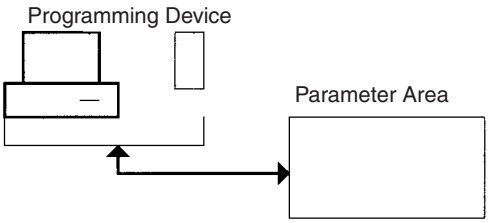
I/O Memory Area

This region of memory contains the data areas which can be accessed by instruction operands. The data areas include the CIO Area, Work Area, Holding Area, Auxiliary Area, DM Area, EM Area, Timer Area, Counter Area, Task Flag Area, Data Registers, Index Registers, Condition Flag Area, and Clock Pulse Area.



Parameter Area

This region of memory contains various settings that cannot be specified by instruction operands; they can be specified from a Programming Device only. The settings include the PC Setup, I/O Table, Routing Table, and CPU Bus Unit settings.



9-2 I/O Memory Areas

9-2-1 I/O Memory Area Structure

The following table shows the basic structure of the I/O Memory Area.

Area		Size	Range	Task usage	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status
								Read	Write			
CIO Area	I/O Area	1,280 bits (80 words)	CIO 0000 to CIO 0079 (See note 1.)	Shared by all tasks	Basic I/O Units	OK	OK	OK	OK	OK	Cleared	OK
	Data Link Area	3,200 bits (200 words)	CIO 1000 to CIO 1199		Data link	OK	OK	OK	OK	OK	Cleared	OK
	CPU Bus Unit Area	6,400 bits (400 words)	CIO 1500 to CIO 1899		CPU Bus Units	OK	OK	OK	OK	OK		OK
	Special I/O Unit Area	15,360 bits (960 words)	CIO 2000 to CIO 2959		Special I/O Units	OK	OK	OK	OK	OK		OK
	DeviceNet Area	9,600 bits (600 words)	CIO 3200 to CIO 3799		DeviceNet (CompoBus/D) Master (fixed allocations	OK	OK	OK	OK	OK	Cleared	OK
	Internal I/O Areas	37,504 bits (2,344 words) 4,800 bits (300 words)	CIO 1200 to CIO 1499 CIO 3800 to CIO 6143		---	OK	OK	OK	OK	OK		OK
Work Area		8,192 bits (512 words)	W000 to W511		---	OK	OK	OK	OK	OK	Cleared	OK
Holding Area		8,192 bits (512 words)	H000 to H511		---	OK	OK	OK	OK	OK	Maintained	OK
Auxiliary Area		15,360 bits (960 words)	A000 to A959		---	OK	OK	OK	A000 to A447 No A448 to A959 OK	A000 to A447 No A448 to A959 OK	Varies from address to address.	No
TR Area		16 bits	TR0 to TR15		---	OK	---	OK	OK	No	Cleared	No
DM Area		32,768 words	D00000 to D32767		---	No (See Note 2)	OK	OK	OK	OK	Maintained	No
EM Area		32,768 words per bank (0 to 2, 3 max.)	E0_00000 to E2_32767		---	No (See Note 2)	OK	OK	OK	OK	Maintained	No
Timer Completion Flags		4,096 bits	T0000 to T4095		---	OK	---	OK	OK	OK	Cleared	OK
Counter Completion Flags		4,096 bits	C0000 to C4095		---	OK	---	OK	OK	OK	Maintained	OK
Timer PVs		4,096 words	T0000 to T4095		---	---	OK	OK	OK	OK	Cleared	No (See note 4.)

Area	Size	Range	Task usage	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status
							Read	Write			
Counter PVs	4,096 words	C0000 to C4095	Shared by all tasks	---	---	OK	OK	OK	OK	Maintained	No (See note 5.)
Task Flag Area	32 bits	TK00 to TK31		---	OK	---	OK	No	No	Cleared	No
Index Registers (See note 3.)	16 registers	IR0 to IR15	Used separately in each task	---	OK	OK	Indirect addressing only	Specific instructions only	No	Cleared	No
Data Registers (See note 3.)	16 registers	DR0 to DR15		---	No	OK	OK	OK	No	Cleared	No

Note

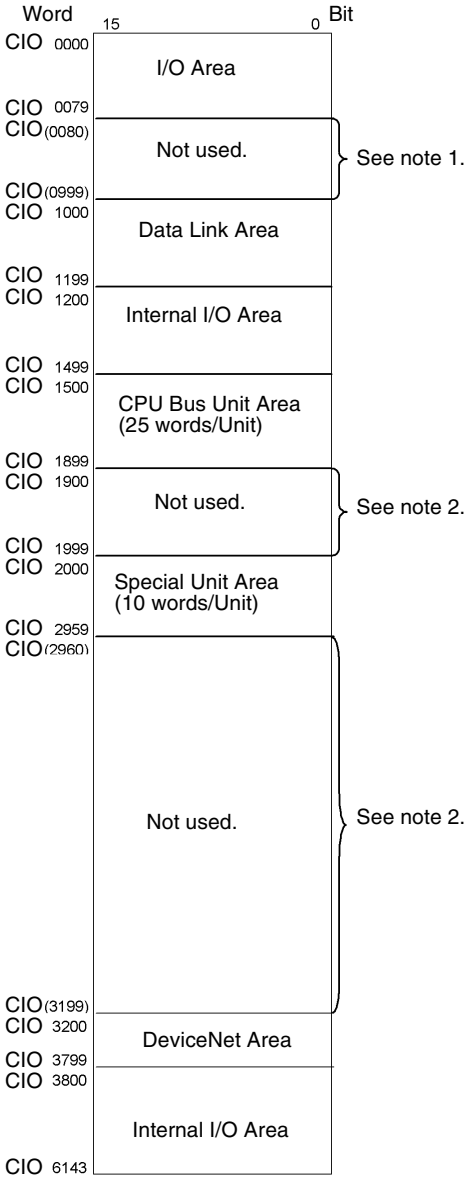
1. The I/O Area can be expanded to CIO 0000 to CIO 0999 by changing the first words allocated to Racks.
2. Bits can be manipulated using TST(350), TSTN(351), SET, SETB(532), RSTB(533), OUTB(534).
3. Index registers and data registers can be used either individually by task or they can be shared by all the tasks (CJ1-H CPU Units only).
4. Timer PVs can be refreshed indirectly by forced setting/resetting Timer Completion Flags.
5. Counter PVs can be refreshed indirectly by forced setting/resetting Counter Completion Flags.

9-2-2 Overview of the Data Areas

The data areas in the I/O Memory Area are described in detail below.

CIO Area

It isn't necessary to input the "CIO" acronym when specifying an address in the CIO Area. The CIO Area is generally used for data exchanges such as I/O refreshing with various Units. Words that aren't allocated to Units may be used as work words and work bits in the program only.



Note

1. It is possible to use CIO 0080 to CIO 0999 for I/O words by making the appropriate settings for the first words on the Racks. Settings for the first words on the Racks can be made using the CX-Programmer to set the first Rack addresses in the I/O table. The settings range for the first Rack addresses is from CIO 0000 to CIO 0900.
2. The parts of the CIO Area that are labelled "Not used" may be used in programming as work bits. In the future, however, unused CIO Area bits may be used when expanding functions. Always use Work Area bits first.

I/O Area

These words are allocated to external I/O terminals on Basic I/O Units. Words that aren't allocated to external I/O terminals may be used only in the program.

Data Link Area

These words are used for data links in Controller Link Networks. Words that aren't used in data links may be used only in the program.

CPU Bus Unit Area

These words are allocated to CPU Bus Units to transfer status information. Each Unit is allocated 25 words and up to 16 Units (with unit numbers 0 to 15) can be used. Words that aren't used by CPU Bus Units may be used only in the program.

Special I/O Unit Area

These words are allocated to Special I/O Units. Each Unit is allocated 10 words and up to 96 Units (unit numbers 0 to 95) can be used).
Words that aren't used by Special I/O Units may be used only in the program.

DeviceNet Area

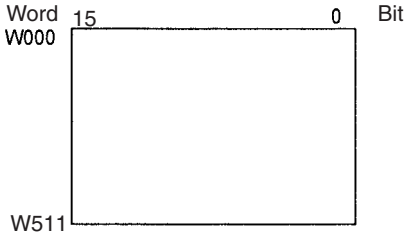
These words are allocated to Slaves for DeviceNet (CompoBus/D) Remote I/O Communications. Allocations are fixed and cannot be changed. Words that aren't used by DeviceNet devices can be used only in the program.

Internal I/O Area

These words can be used only in the program; they cannot be used for I/O exchange with external I/O terminals. Be sure to use the work words provided in the Work Area (WR) before allocating words in the Internal I/O Area or other unused words in the CIO Area. It is possible that these words will be assigned to new functions in future versions of CJ-series CPU Units, so the program may have to be changed before being used in a new CJ-series PC if CIO Area words are used as work words in the program.

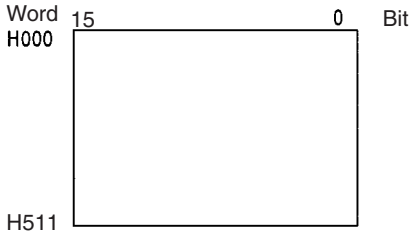
Work Area (WR)

Words in the Work Area can be used only in the program; they cannot be used for I/O exchange with external I/O terminals. No new functions will be assigned to this area in future versions of CJ PCs, so use this area for work words and bits before any words in the CIO Area.



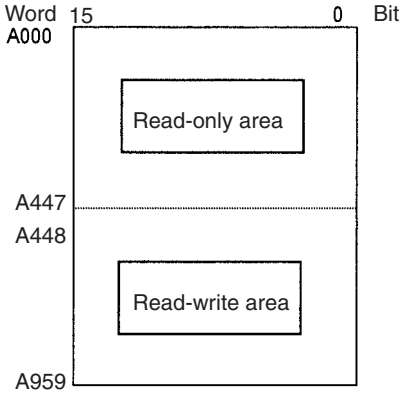
Holding Area (HR)

Words in the Holding Area can be used only in the program. These words retain their content when the PC is turned on or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.



Auxiliary Area (AR)

The Auxiliary Area contains flags and control bits used to monitor and control PC operation. This area is divided into two parts: A000 to A447 are read-only and A448 to A959 can be read or written. Refer to *9-10 Auxiliary Area* for details on the Auxiliary Area.

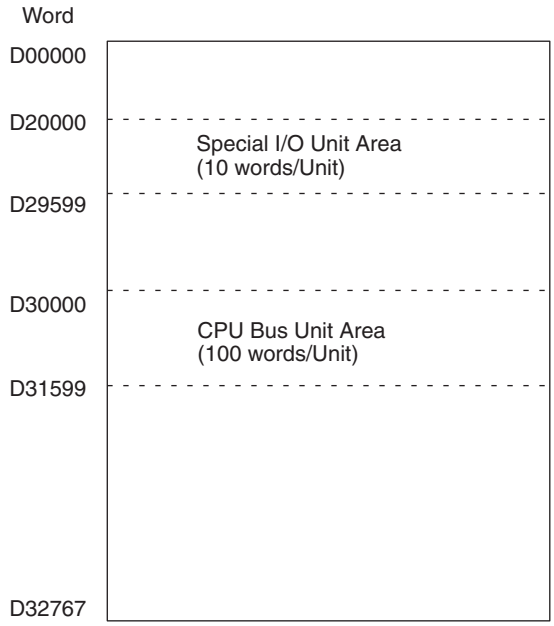


Temporary Relay Area (TR)

The TR Area contains bits that record the ON/OFF status of program branches. The TR bits are used with mnemonics only.

Data Memory Area (DM)

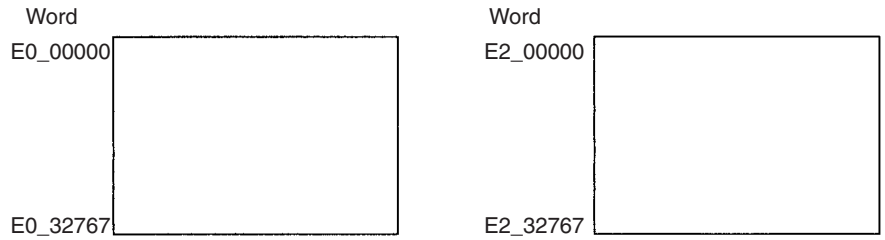
The DM Area is a multi-purpose data area that can be accessed in word-units only. These words retain their content when the PC is turned on or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.



Extended Data Memory Area (EM)

The EM Area is a multi-purpose data area that can be accessed in word-units only. These words retain their content when the PC is turned on or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.

The EM Area is divided into 32,767-word regions called banks. The number of EM banks depends upon the model of CPU Unit, with a maximum of 13 banks (0 to C). Refer to *2-1 Specifications* for details on the number of EM banks provided in each model of CPU Unit.



Timer Area

There are two timer data areas, the Timer Completion Flags and the Timer Present Values (PVs). Up to 4,096 timers with timer numbers T0000 to T4095 can be used. The same number is used to access a timer's Completion Flag and PV.

Timer Completion Flags

These flags are read as bits. A Completion Flag is turned ON by the system when the corresponding timer times out (the set time elapses).

Timer PVs

The PVs are read and written as words (16 bits). The PVs count up or down as the timer operates.

Counter Area

There are two counter data areas, the Counter Completion Flags and the Counter Present Values (PVs). Up to 4,096 counters with counter numbers

C0000 to C4095 can be used. The same number is used to access a counter's Completion Flag and PV.

Counter Completion Flags

These flags are read as bits. A Completion Flag is turned ON by the system when the corresponding counter counts out (the set value is reached).

Counter PVs

The PVs are read and written as words (16 bits). The PVs count up or down as the counter operates.

Condition Flags

These flags include the Arithmetic Flags such as the Error Flag and Equals Flag which indicate the results of instruction execution as well as the Always ON and Always OFF Flags. The Condition Flags are specified with labels (symbols) rather than addresses.

Clock Pulses

The Clock Pulses are turned ON and OFF by the CPU Unit's internal timer. These bits are specified with labels (symbols) rather than addresses.

Task Flag Area (TK)

Task Flags range from TK00 to TK31 and correspond to cyclic tasks 0 to 31. A Task Flag will be ON when the corresponding cyclic task is in executable (RUN) status and OFF when the cyclic task hasn't been executed (INI) or is in standby (WAIT) status.

Index Registers (IR)

These registers (IR0 to IR15) are used to store PC memory addresses (absolute memory addresses in RAM) to indirectly address words in I/O memory. The Index Registers can be used separately in each task or, for CJ1-H CPU Units, they can be shared by all tasks.Data Registers (DR)

Data Registers (DR)

These registers (DR0 to DR15) are used together with the Index Registers. When a Data Register is input just before an Index Register, the content of the Data Register is added to the PC memory address in the Index Register to offset that address. The Data Registers are used separately in each task or, for CJ1-H CPU Units, they can be shared by all tasks.

9-2-3 Data Area Properties

Content after Fatal Errors, Forced Set/Reset Usage

Area		Fatal Error Generated				Forced Set/ Forced Reset Functions Usable?
		Execution of FALS(007)		Other Fatal Error		
		IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	
CIO Area	I/O Area	Retained	Retained	Cleared	Retained	Yes
	Data Link Area					
	CPU Bus Unit Area					
	Special I/O Unit Area					
	DeviceNet Area					
	Internal I/O Area					
Work Area (W)		Retained	Retained	Cleared	Retained	Yes
Holding Area (H)		Retained	Retained	Retained	Retained	Yes
Auxiliary Area (A)		Status varies from address to address.				No
Data Memory Area (D)		Retained	Retained	Retained	Retained	No
Extended Data Memory Area (E)		Retained	Retained	Retained	Retained	No
Timer Completion Flags (T)		Retained	Retained	Cleared	Retained	Yes
Timer PVs (T)		Retained	Retained	Cleared	Retained	No
Counter Completion Flags (C)		Retained	Retained	Retained	Retained	Yes
Counter PVs (C)		Retained	Retained	Retained	Retained	No

Area	Fatal Error Generated				Forced Set/ Forced Reset Functions Usable?
	Execution of FALS(007)		Other Fatal Error		
	IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	
Task Flags (TK)	Cleared	Cleared	Retained	Retained	No
Index Registers (IR)	Retained	Retained	Cleared	Retained	No
Data Registers (DR)	Retained	Retained	Cleared	Retained	No

Content after Mode Change or Power Interruption

Area		Mode Changed[1]		PC Power OFF to ON			
				IOM Hold Bit Cleared[2]		IOM Hold Bit Held[2]	
		IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON
CIO Area	I/O Area	Cleared	Retained	Cleared	Cleared	Cleared	Retained
	Data Link Area						
	CPU Bus Unit Area						
	Special I/O Unit Area						
	DeviceNet Area						
	Internal I/O Area						
Work Area (W)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Holding Area (H)		Retained	Retained	Retained	Retained	Retained	Retained
Auxiliary Area (A)		Status varies from address to address.					
Data Memory Area (D)		Retained	Retained	Retained	Retained	Retained	Retained
Extended Data Memory Area (E)		Retained	Retained	Retained	Retained	Retained	Retained
Timer Completion Flags (T)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Timer PVs (T)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Counter Completion Flags (C)		Retained	Retained	Retained	Retained	Retained	Retained
Counter PVs (C)		Retained	Retained	Retained	Retained	Retained	Retained
Task Flags (TK)		Cleared	Cleared	Cleared	Cleared	Cleared	Cleared
Index Registers (IR)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Data Registers (DR)		Cleared	Retained	Cleared	Cleared	Cleared	Retained

Note
1. Mode changed from PROGRAM to RUN/MONITOR or vice-versa.
2. The PC Setup's "IOM Hold Bit Status at Startup" setting determines whether the IOM Hold Bit's status is held or cleared when the PC is turned on.

9-3 I/O Area

I/O Area addresses range from CIO 0000 to CIO 0079 (CIO bits 000000 to 007915), but the area can be expanded to CIO 0000 to CIO 0999 by changing the first Rack word with any Programming Device other than a Programming Console. The maximum number of bits that can be allocated for external I/O will still be 1,280 (80 words) even if the I/O Area is expanded.

Note The maximum number of external I/O points depends upon the CPU Unit being used.

Words in the I/O Area are allocated to I/O terminals on Basic I/O Units.

Words are allocated to Basic I/O Units based on the slot position (left to right) and number of words required. The words are allocated consecutively and empty slots are skipped. Words in the I/O Area that aren't allocated to Basic I/O Units can be used only in the program.

Forcing Bit Status Bits in the I/O Area can be force-set and force-reset.

I/O Area Initialization The contents of the I/O Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
   (See the following explanation of IOM Hold Bit Operation.)
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.
   (See the following explanation of IOM Hold Bit Operation.)
3. The I/O Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the I/O Area will be retained if FALS(007) is executed.)

IOM Hold Bit Operation If the IOM Hold Bit (A50012) is ON, the contents of the I/O Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the I/O Area won't be cleared when the PC's power supply is cycled. All I/O bits, including outputs, will retain the status that they had before the PC was turned off.

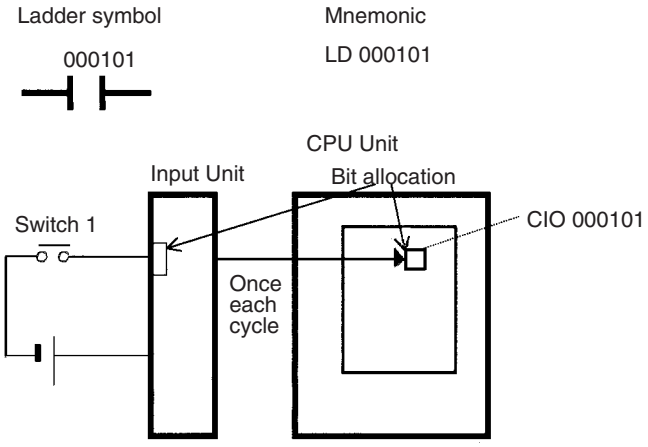
Note If the I/O Hold Bit is turned ON, the outputs from the PC will not be turned OFF and will maintain their previous status when the PC is switched from RUN or MONITOR mode to PROGRAM mode. Make sure that the external loads will not produce dangerous conditions when this occurs. (When operation stops for a fatal error, including those produced with the FALS(007) instruction, all outputs from Output Unit will be turned OFF and only the internal output status will be maintained.)

Input Bits

A bit in the I/O Area is called an input bit when it is allocated to an Input Unit. Input bits reflect the ON/OFF status of devices such as push-button switches, limit switches, and photoelectric switches. There are three ways for the status of input points to be refreshed in the PC: normal I/O refreshing, immediate refreshing, and IORF(097) refreshing.

Normal I/O Refreshing The status of I/O points on external devices is read once each cycle after program execution.

In the following example, CIO 000101 is allocated to switch 1, an external switch connected to the input terminal of an Input Unit. The ON/OFF status of switch 1 is reflected in CIO 000101 once each cycle.



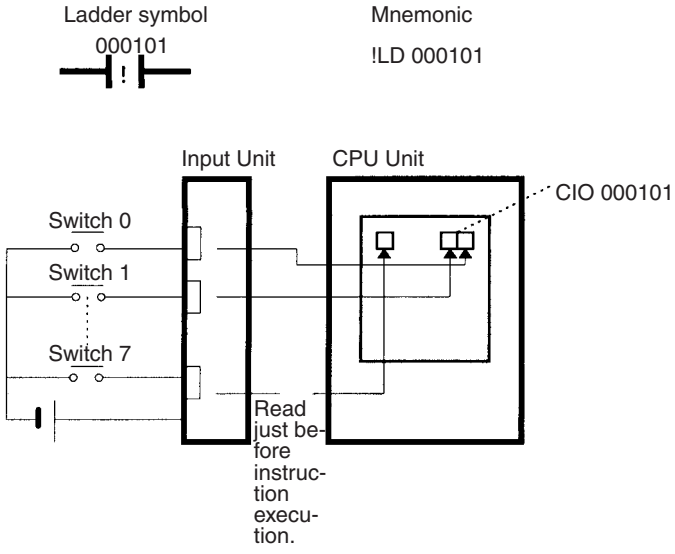
Immediate Refreshing

When the immediate refreshing variation of an instruction is specified by inputting an exclamation point just before the instruction, and the instruction's operand is an input bit or word, the word containing the bit or the word itself will be refreshed just before the instruction is executed. This immediate refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

1,2,3...

1. Bit Operand
   Just before the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the word containing the specified bit will be read to the PC.
2. Word Operand
   Just before the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the specified word will be read to the PC.

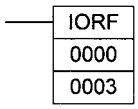
In the following example, CIO 000101 is allocated to switch 1, an external switch connected to the input terminal of an Input Unit. The ON/OFF status of switch 1 is read and reflected in CIO 000101 just before !LD 000101 is executed.



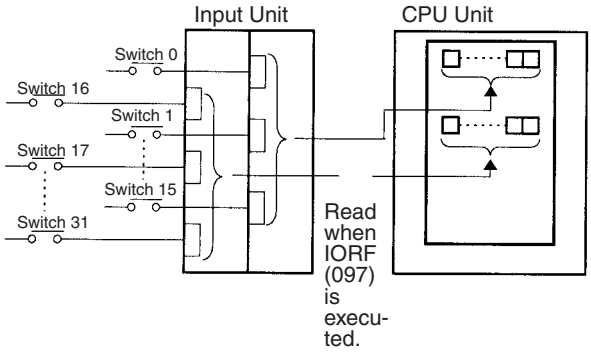
IORF(097) Refreshing

When IORF(097) (I/O REFRESH) is executed, the input bits in the specified range of words are refreshed. This I/O refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

The following IORF(097) instruction refreshes the status of all I/O points in I/O Area words CIO 0000 to CIO 0003. The status of input points is read from the Input Units and the status of output bits is written to the Output Units.



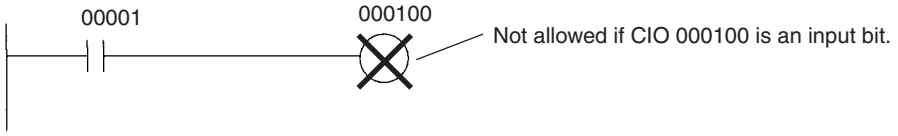
In the following example, the status of input points allocated to CIO 0000 and CIO 0001 are read from the Input Unit. (CIO 0002 and CIO 0003 are allocated to Output Units.)



Limitations on Input bits

There is no limit on the number of times that input bits can be used as normally open and normally closed conditions in the program and the addresses can be programmed in any order.

An input bit cannot be used as an operand in an Output instruction.

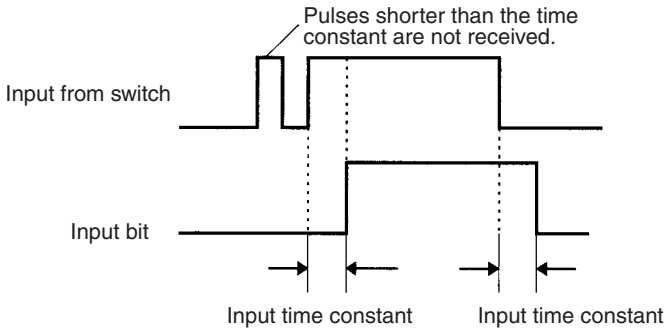


Input Response Time Settings

The input response times for each Input Unit can be set in the PC Setup. Increasing the input response time will reduce chattering and the effects of noise and decreasing the input response time allows higher speed input pulses to be received.

The default value for input response times is 8 ms and the setting range is 0.5 ms to 32 ms.

Note If the time is set to 0 ms, there will still be an ON delay time of 20 μs max. and an OFF delay time of 300 μs due to delays caused by internal elements.



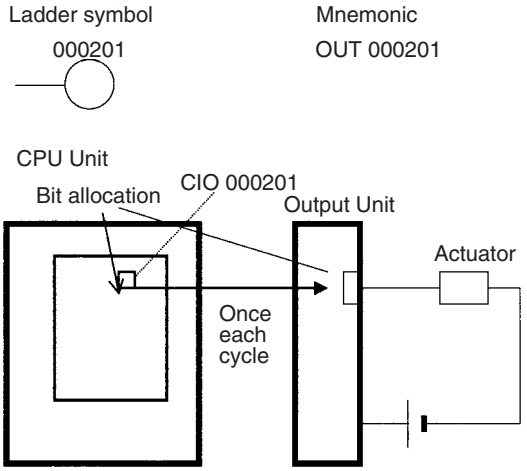
Output Bits

A bit in the I/O Area is called an output bit when it is allocated to an Output Unit. The ON/OFF status of an output bits are output to devices such as actuators. There are three ways for the status of output bits to be refreshed to an Output Unit: normal I/O refreshing, immediate refreshing, and IORF(097) refreshing.

Normal I/O Refreshing

The status of output bits are output to external devices once each cycle after program execution.

In the following example, CIO 000201 is allocated to an actuator, an external device connected to an output terminal of an Output Unit. The ON/OFF status of CIO 000201 is output to that actuator once each cycle.



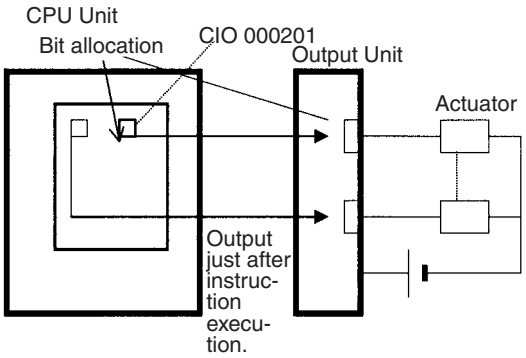
Immediate Refreshing

When the immediate refreshing variation of an instruction is specified by inputting an exclamation point just before the instruction, and the instruction's operand is an output bit or word, the content of the word containing the bit or the word itself will be output just after the instruction is executed. This immediate refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

1,2,3...

1. Bit Operand
   Just after the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the word containing the specified bit will be output to the output device(s).
2. Word Operand
   Just after the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the specified word will be output to the output device(s).

In the following example, CIO 000201 is allocated to an actuator, an external device connected to the output terminal of an Output Unit. The ON/OFF status of CIO 000201 is output to the actuator just after !OUT 000201 is executed.

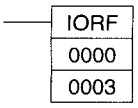


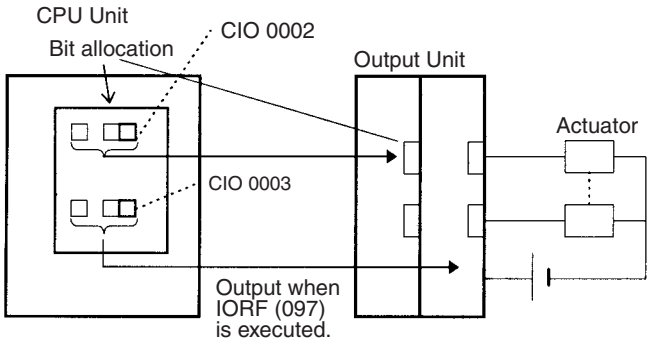
IORF(097) Refreshing

When IORF(097) (I/O REFRESH) is executed, the ON/OFF status of output bits in the specified range of words is output to their external devices. This I/O refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

The following IORF(097) instruction refreshes the status of all I/O points in I/O Area words CIO 0000 to CIO 0003. The status of input points is read from the Input Units and the status of output bits is written to the Output Units.

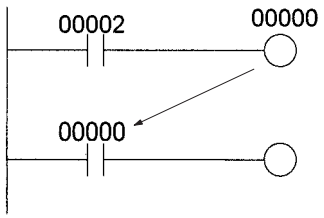
In this example, the status of input points allocated to CIO 0002 and CIO 0003 are output to the Output Unit. (CIO 0000 and CIO 0001 are allocated to Input Units.)



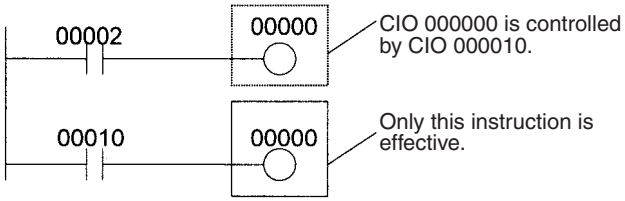


Limitations on Output Bits

Output bits can be programmed in any order. Output bits can be used as operands in Input instructions and there is no limit on the number of times that an output bit is used as a normally open and normally closed condition.



An output bit can be used in only one Output instruction that controls its status. If an output bit is used in two or more Output instructions, only the last instruction will be effective.



Note All outputs on Basic I/O Units and Special I/O Units can be turned OFF by turning ON the Output OFF Bit (A50015). The status of the output bits won't be affected even though the actual outputs are turned OFF.

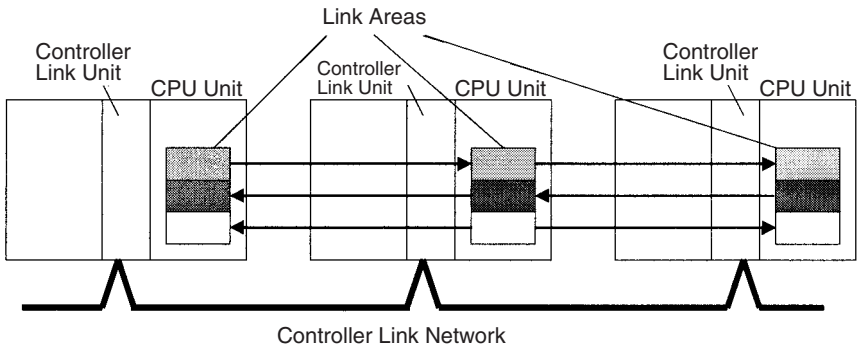
9-4 Data Link Area

Data Link Area addresses range from CIO 1000 to CIO 1199 (CIO bits 100000 to 119915). Words in the Link Area can be used for data links in Controller Link Networks.

A data link automatically (independently of the program) shares data with Link Areas in other CJ-series CPU Units in the network through a Controller Link Unit mounted to the PC's CPU Rack.

Data links can be generated automatically (using the same number of words for each node) or manually. When a user defines the data link manually, he can assign any number of words to each node and make nodes receive-only or transmit-only. Refer to the *Controller Link Units Operation Manual (W309*) for more details.

Words in the Link Area that aren't used for a data link can be used only in the program.



Forcing Bit Status

Bits in the Data Link Area can be force-set and force-reset.

Links to C200HX/HG/HE, C200HS, and C200H PCs

Link Area words CIO 1000 to CIO 1063 in CJ-series PCs correspond to Link Relay Area words LR 00 to LR 63 for data links created in C200HX/HG/HE PCs. When converting C200HX/HG/HE, C200HS, or C200H programs for use in CJ-series PCs, change addresses LR 00 through LR 63 to their equivalent Link Area addresses CIO 1000 through CIO 1063.

Link Area Initialization

The contents of the Link Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.

3. The Link Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Link Area will be retained if FALS(007) is executed.)

IOM Hold Bit Operation

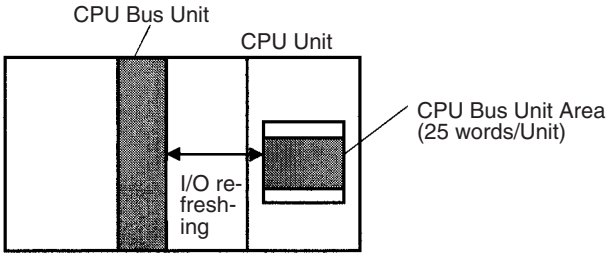
If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Link Area won't be cleared when the PC's power supply is cycled.

If the IOM Hold BIt (A50012) is ON, the contents of the Link Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

9-5 CPU Bus Unit Area

The CPU Bus Unit Area contains 400 words with addresses ranging from CIO 1500 to CIO 1899. Words in the CPU Bus Unit Area can be allocated to CPU Bus Units to transfer data such as the operating status of the Unit. Each Unit is allocated 25 words based on the Unit's unit number setting.

Data is exchanged with CPU Bus Units once each cycle during I/O refreshing, which occurs after program execution. (Words in this data area cannot be refreshed with immediate-refreshing or IORF(097).)



Each CPU Bus Unit is allocated 25 words based on its unit number, as shown in the following table.

Unit number	Allocated words
0	CIO 1500 to CIO 1524
1	CIO 1525 to CIO 1549
2	CIO 1550 to CIO 1574
3	CIO 1575 to CIO 1599
4	CIO 1600 to CIO 1624
5	CIO 1625 to CIO 1649
6	CIO 1650 to CIO 1674
7	CIO 1675 to CIO 1699
8	CIO 1700 to CIO 1724
9	CIO 1725 to CIO 1749
A	CIO 1750 to CIO 1774
B	CIO 1775 to CIO 1799
C	CIO 1800 to CIO 1824
D	CIO 1825 to CIO 1849
E	CIO 1850 to CIO 1874
F	CIO 1875 to CIO 1899

The function of the 25 words depends upon the CPU Bus Unit being used. For details, refer to the Unit's operation manual.

Words in the CPU Bus Unit Area that aren't allocated to CPU Bus Units can be used only in the program.

Forcing Bit Status

Bits in the CPU Bus Unit Area can be force-set and force-reset.

CPU Bus Unit Area Initialization

The contents of the CPU Bus Unit Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.
3. The CPU Bus Unit Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the CPU Bus Unit Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

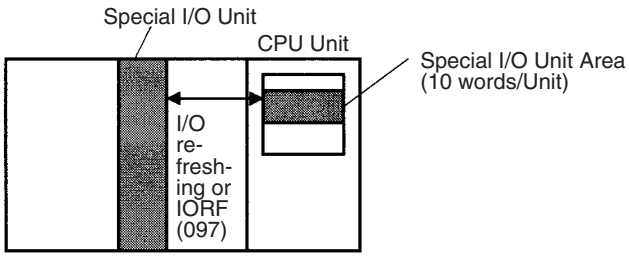
If the IOM Hold BIt (A50012) is ON, the contents of the CPU Bus Unit Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the CPU Bus Unit Area won't be cleared when the PC's power supply is cycled.

9-6 Special I/O Unit Area

The Special I/O Unit Area contains 960 words with addresses ranging from CIO 2000 to CIO 2959. Words in the Special I/O Unit Area are allocated to CJ to transfer data such as the operating status of the Unit. Each Unit is allocated 10 words based on its unit number setting.

Data is exchanged with Special I/O Units once each cycle during I/O refreshing, which occurs after program execution. The words can also be refreshed with IORF(097).



Each Special I/O Unit is allocated 25 words based on its unit number, as shown in the following table.

Unit number	Allocated words
0	CIO 2000 to CIO 2009
1	CIO 2010 to CIO 2019
2	CIO 2020 to CIO 2029
3	CIO 2030 to CIO 2039
4	CIO 2040 to CIO 2049
5	CIO 2050 to CIO 2059
6	CIO 2060 to CIO 2069
7	CIO 2070 to CIO 2079
8	CIO 2080 to CIO 2089

Unit number	Allocated words
9	CIO 2090 to CIO 2099
10 (A)	CIO 2100 to CIO 2109
11 (B)	CIO 2110 to CIO 2119
12 (C)	CIO 2120 to CIO 2129
13 (D)	CIO 2130 to CIO 2139
14 (E)	CIO 2140 to CIO 2149
15 (F)	CIO 2150 to CIO 2159
16	CIO 2160 to CIO 2169
17	CIO 2170 to CIO 2179
95	CIO 2950 to CIO 2959

The function of the 10 words allocated to a Unit depends upon the Special I/O Unit being used. For details, refer to the Unit's Operation Manual.

Words in the Special I/O Unit Area that aren't allocated to Special I/O Units can be used only in the program.

Forcing Bit Status

Bits in the Special I/O Unit Area can be force-set and force-reset.

Special I/O Unit Area Initialization

The contents of the Special I/O Unit Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.
3. The Special I/O Unit Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Special I/O Unit Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

If the IOM Hold BIt (A50012) is ON, the contents of the Special I/O Unit Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Special I/O Unit Area won't be cleared when the PC's power supply is cycled.

9-7 DeviceNet Area

The DeviceNet Area consists of 600 words from CIO 3200 to CIO 3799. Words in the DeviceNet Area are allocated to Slaves for DeviceNet remote I/O communications. Data is exchanged regularly to Slaves in the network (independent of the program) through the DeviceNet Unit.

Words are allocated to Slaves using fixed allocations according to fixed allocation settings 1, 2, and 3. One of these fixed areas is selected.

Area	Output Area (master to slaves)	Input Area (slaves to master)
Fixed Allocation Area 1	CIO 3200 to CIO 3263	CIO 3300 to CIO 3363
Fixed Allocation Area 2	CIO 3400 to CIO 3463	CIO 3500 to CIO 3563
Fixed Allocation Area 3	CIO 3600 to CIO 3663	CIO 3700 to CIO 3763

The following words are allocated to the DeviceNet Unit when the remote I/O slave function is used with fixed allocations.

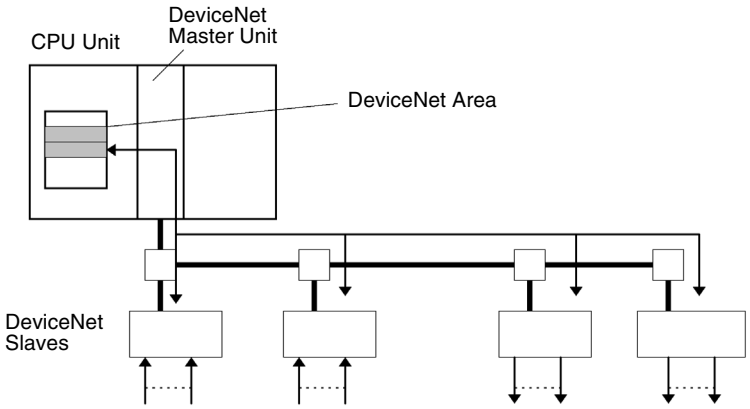
Area	Output Area (master to slaves)	Input Area (slaves to master)
Fixed Allocation Area 1	CIO 3370	CIO 3270
Fixed Allocation Area 2	CIO 3570	CIO 3470
Fixed Allocation Area 3	CIO 3770	CIO 3670

Bits in the DeviceNet Area can be force-set and force-reset.

Note There are two ways to allocated I/O in DeviceNet networks: Fixed allocations according to node addresses and user-set allocations.

- With fixed allocations, words are automatically allocated to the slave in the specified fixed allocation area according to the node addresses.
- With user-set allocations, the user can allocate words to Slaves from the following words.
  CIO 0000 to CIO 0235, CIO 0300 to CIO 0511, CIO 1000 to CIO 1063
  W000 to W511
  H000 to H511
  D00000 to D32767
  E00000 to E32767, banks 0 to 2

For details on word allocations, refer to the *DeviceNet (CompoBus/D) Operation Manual (W267)*.



DeviceNet Area Initialization

The contents of the DeviceNet Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.
3. The DeviceNet Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the DeviceNet Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

If the IOM Hold BIt (A50012) is ON, the contents of the DeviceNet Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the DeviceNet Area won't be cleared when the PC's power supply is cycled.

9-8 Internal I/O Area

The Internal I/O (Work) Area contains 512 words with addresses ranging from W000 to W511. These words can be used only in the program as work words.

There are unused words in the CIO Area (CIO 1200 to CIO 1499 and CIO 3800 to CIO 6143) that can also be used in the program, but use any available words in the Work Area first because the unused words in the CIO Area may be allocated to new functions in future versions of CJ-series CPU Units.

Bits in the Work Area can be force-set and force-reset.

Work Area Initialization

The contents of the Work Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.
3. The Work Area is cleared from a Programming Device.
4. PC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Work Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

If the IOM Hold BIt (A50012) is ON, the contents of the Work Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Work Area won't be cleared when the PC's power supply is cycled.

9-9 Holding Area

The Holding Area contains 512 words with addresses ranging from H000 to H511 (bits H00000 to H51115). These words can be used only in the program.

Holding Area bits can be used in any order in the program and can be used as normally open or normally closed conditions as often as necessary.

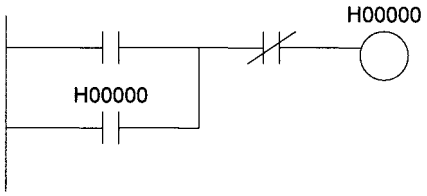
Holding Area Initialization

Data in the Holding Area is not cleared when the PC's power supply is cycled or the PC's operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

A Holding Area bit will be cleared if it is programmed between IL(002) and ILC(003) and the execution condition for IL(002) is OFF. To keep a bit ON even when the execution condition for IL(002) is OFF, turn ON the bit with the SET instruction just before IL(002).

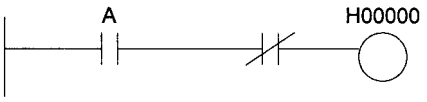
Self-maintaining Bits

When a self-maintaining bit is programmed with a Holding Area bit, the self-maintaining bit won't be cleared even when the power is reset.



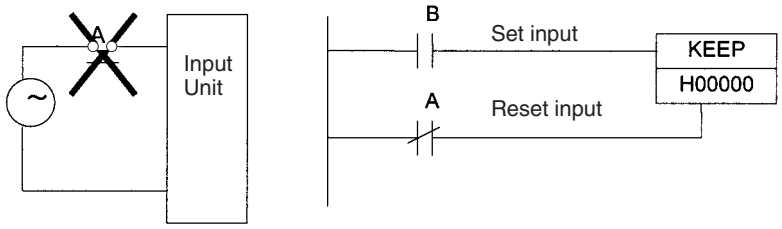
Note

1. If a Holding Area bit is not used for the self-maintaining bit, the bit will be turned OFF and the self-maintaining bit will be cleared when the power is reset.
2. If a Holding Area bit is used but not programmed as a self-maintaining bit as in the following diagram, the bit will be turned OFF by execution condition A when the power is reset.

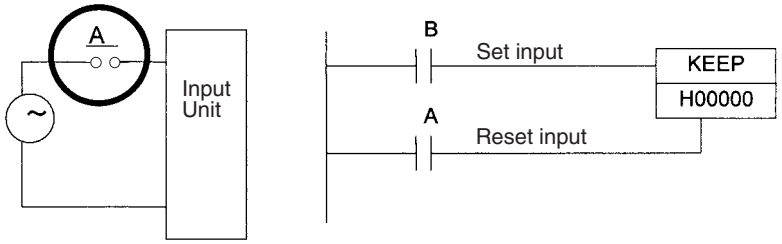


Precautions

When a Holding Area bit is used in a KEEP(011) instruction, never use a normally closed condition for the reset input if the input device uses an AC power supply. When the power supply goes OFF or is temporarily interrupted, the input will go OFF before the PC's internal power supply and the Holding Area bit will be reset.



Instead, use a configuration like the one shown below.



There are no restrictions in the order of using bit address or in the number of N.C. or N.O. conditions that can be programmed.

9-10 Auxiliary Area

The Auxiliary Area contains 960 words with addresses ranging from A000 to A959). These words are preassigned as flags and control bits to monitor and control operation.

A000 through A447 are read-only, but A448 through A959 can be read or written from the program or a Programming Device.

Note The addresses in the Auxiliary Area cannot be designated directly in programming or allocations inside C200H Special I/O Units.

Forcing Bit Status

Bits in the Auxiliary Area cannot be force-set and force-reset continuously.

Writing Auxiliary Area Data

The following operations can be performed from a Programming Device to write data in the Auxiliary Area.

- Using the CX-Programmer: Online set/reset (not force-set/force-reset), changing present values when monitoring programming addresses (set values dialog box), or transferring data to the PC after editing the PC data tables. Refer to the *CX-Programmer User Manual* (W361-E2).
- Using a Programming Console: Temporarily force-setting/force-resetting bits from the Bit/Word Monitor or the 3-word Monitor operation (see the *Programming Console Operation Manual*).

Functions

The following table lists the functions of Auxiliary Area flags and control bits. The table is organized according to the functions of the flags and bits. For more details or to look up a bit by its address, refer to *Appendix B Auxiliary Area*.

Initial Settings

Name	Address	Description	Access
I/O Response Times in Basic I/O Units	A22000 to A25915	Contains the current I/O response times for CJ-series Basic I/O Units.	Read-only
IOM Hold Bit	A50012	Determines whether the contents of I/O memory are retained when the PC's power is reset or the PC's operating mode is changed (from PROGRAM to RUN/MONITOR or vice-versa). Turn ON this bit to maintain I/O memory when changing between PROGRAM and RUN or MONITOR mode. Turn OFF this bit to clear I/O memory when changing the changing between PROGRAM and RUN or MONITOR mode.	Read/write
Forced Status Hold BIt	A50013	Determines whether the status of force-set and force-reset bits is maintained when the PC's power is reset or the PC's operating mode is changed (between PROGRAM and RUN or MONITOR mode).	Read/write
Power Interruption Disable Setting (CJ1-H CPU Units only)	A530	Set to A5A5 Hex to disable power interrupts (except the Power OFF Interrupt task) between DI(693) and EI(694) instructions.	Read/write

CPU Unit Settings

Name	Address	Description	Access
Status of DIP Switch Pin 6	A39512	Contains the status set on pin 6 of the CPU Unit's DIP switch. (Refreshed every cycle.)	Read-only

Basic I/O Unit Settings

Name	Address	Description	Access
Basic I/O Unit Status Area	A05000 to A08915	Indicates whether fuses in Basic I/O Units are intact or blown. The flags correspond to rack 0, slot 0 through rack 7, slot 9.	Read-only
I/O Allocation Status	A260	Indicates the current status of I/O allocation, i.e., Automatic I/O Allocation at Startup or User-set I/O Allocations.	Read-only
Units Detected at Startup (Racks 0 to 3) (CJ1-H CPU Unit only)	Rack 0: A33600 to A33603 Rack 1: A33604 to A33607 Rack 2: A33608 to A33611 Rack 3: A33612 to A33615	The number of Units detected on each Rack is stored in 1-digit hexadecimal (0 to A Hex). Example: The following would be stored if Rack 0 had 1 Unit, Rack 1 had 4 Units, Rack 2 had 8 Units and Rack 3 had 10 Units: A336 = A 8 4 1	Read-only

CPU Bus Unit Flags/Bits

Name	Address	Description	Access
CPU Bus Unit Initialization Flags	A30200 to A30215	These flags correspond to CPU Bus Units 0 to 15. A flag will be ON while the corresponding Unit is initializing after the power is turned ON or the Unit's Restart Bit (in A501) is turned ON.	Read-only
CPU Bus Unit Restart Bits	A50100 to A50115	These bits correspond to CPU Bus Units 0 to 15. Turn a bit from OFF to ON to restart the corresponding Unit.	Read/write

Special I/O Unit Flags/Bits

Name	Address	Description	Access
Special I/O Unit Initialization Flags	A33000 to A33515	These flags correspond to Special I/O Units 0 to 95. A flag will be ON while the corresponding Unit is initializing after the power is turned ON or the Unit's Restart Bit is turned ON. (Restart Bits A50200 to A50715 correspond to Units 0 to 95.)	Read-only
Special I/O Unit Restart Bits	A50200 to A50715	These bits correspond to Special I/O Units 0 to 95. Turn a bit from OFF to ON to restart the corresponding Unit.	Read/write

System Flags

Name	Address	Description	Access
First Cycle Flag	A20011	This flag is turned ON for one cycle when program execution starts (the operating mode is switched from PROGRAM to RUN/MONITOR).	Read-only
Initial Task Execution Flag	A20015	When a task switches from INI to RUN status for the first time, this flag will be turned ON within the task for one cycle only.	Read-only
Task Started Flag (CJ1-H CPU Units only)	A20014	When a task switches from WAIT or INI to RUN status, this flag will be turned ON within the task for one cycle only. The only difference between this flag and A20015 is that this flag also turns ON when the task switches from WAIT to RUN status.	Read-only
Maximum Cycle Time	A262 to A263	These words contain the maximum cycle time in units of 0.1 ms. In a Parallel Processing Mode, the maximum cycle time of the program execution cycle will be given. The time is updated every cycle and is recorded in 32-bit binary (0 to FFFF FFFF, or 0 to 429,496,729.5 ms). (A263 is the leftmost word.)	Read-only
Present Cycle Time	A264 to A265	These words contain the present cycle time in units of 0.1 ms. In a Parallel Processing Mode, the maximum cycle time of the program execution cycle will be given. The time is updated every cycle and is recorded in 32-bit binary (0 to FFFF FFFF, or 0 to 429,496,729.5 ms). (A265 is the leftmost word.)	Read-only
Peripheral Servicing Cycle Time (CJ1-H CPU Units only)	A268	In Parallel Processing with Synchronous or Asynchronous Memory Access, this word contains the peripheral servicing cycle time in units of 0.1 ms. The time is updated every cycle and is recorded in 16-bit binary (0 to 4E20 Hex, or 0.0 to 2,000.0 ms).	Read-only

Task Information

Name	Address	Description	Access
Task Number when Program Stopped	A294	This word contains the task number of the task that was being executed when program execution was stopped because of a program error.	Read-only
Maximum Interrupt Task Processing Time	A440	Contains the Maximum Interrupt Task Processing Time in units of 0.1 ms.	Read-only
Interrupt Task with Max. Processing Time	A441	Contains the task number of the interrupt task with the maximum processing time. Hexadecimal values 8000 to 80FF correspond to task numbers 00 to FF. Bit 15 is turned ON when an interrupt has occurred.	Read-only
IR/DR Operation between Tasks (CJ1-H CPU Units only)	A09914	Turn ON this bit to share index and data registers between all tasks. Turn OFF this bit to use separate index and data registers between in each task.	Read-only

Debugging Information

■ Online Editing

Name	Address	Description	Access
Online Editing Wait Flag	A20110	ON when an online editing process is waiting. (An online editing request was received while online editing was disabled.)	Read-only
Online Editing Processing Flag	A20111	ON when an online editing process is being executed.	Read-only
Online Editing Disable Bit Validator	A52700 to A52707	The Online Editing Disable Bit (A52709) is valid only when this byte contains 5A.	Read/write
Online Editing Disable Bit	A52709	Turn this bit ON to disable online editing.	Read/write

■ Output Control

Name	Address	Description	Access
Output OFF Bit	A50015	Turn this bit ON to turn OFF all outputs from Basic I/O Units, Output Units, and Special I/O Units.	Read/write

■ Differentiate Monitor

Name	Address	Description	Access
Differentiate Monitor Completed Flag	A50809	ON when the differentiate monitor condition has been established during execution of differentiation monitoring.	Read/write

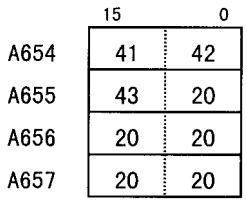
■ Data Tracing

Name	Address	Description	Access
Sampling Start Bit	A50815	When a data trace is started by turning this bit from OFF to ON from a Programming Device, the PC will begin storing data in Trace Memory by one of the three following methods: 1) Periodic sampling (10 to 2,550 ms) 2) Sampling at execution of TRSM(045) 3) Sampling at the end of every cycle.	Read/write
Trace Start Bit	A50814	Turn this bit from OFF to ON to establish the trigger condition. The offset indicated by the delay value (positive or negative) determines which data samples are valid.	Read/write
Trace Busy Flag	A50813	ON when the Sampling Start Bit (A50815) is turned from OFF to ON. OFF when the trace is completed.	Read/write
Trace Completed Flag	A50812	ON when sampling of a region of trace memory has been completed during execution of a Trace. OFF when the next time the Sampling Start Bit (A50815) is turned from OFF to ON.	Read/write
Trace Trigger Monitor Flag	A50811	ON when a trigger condition is established by the Trace Start Bit (A50814). OFF when the next Data Trace is started by the Sampling Start bit (A50815).	Read/write

File Memory Information

Name	Address	Description	Access
Memory Card Type	A34300 to A34302	Indicates the type of Memory Card, if any, installed.	Read-only
Memory Card Format Error Flag	A34307	ON when the Memory Card is not formatted or a formatting error has occurred.	Read-only
File Transfer Error Flag	A34308	ON when an error occurred while writing data to file memory.	Read-only
File Write Error Flag	A34309	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory.	Read-only
File Read Error	A34310	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted).	Read-only
File Missing Flag	A34311	ON when an attempt is made to read a file that doesn't exist, or an attempt is made to write to a file in a directory that doesn't exist.	Read-only
File Memory Operation Flag	A34313	ON while any of the following operations is being executed. OFF when none of them are being executed. Memory Card detection started. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Easy backup operation. If this flag is ON, write and comparison operations to the Memory Card cannot be executed.	Read-only

Name	Address	Description	Access
Memory Card Detected Flag	A34315	ON when a Memory Card has been detected. OFF when a Memory Card has not been detected.	Read-only
Number of Items to Transfer	A346 to A347	These words contain the number of words or fields remaining to be transferred (32 bits). For binary files (.IOM), the value is decremented for each word that is read. For text (.TXT) or CSV (.CSV) data, the value is decremented for each field that is read.	Read-only
Accessing File Data Flag	A34314	ON while file data is being accessed.	Read-only
EM File Memory Format Error Flag	A34306	Turns ON when a format error occurs in the first EM bank allocated for file memory. Turns OFF when formatting is completed normally.	Read-only
EM File Memory Starting Bank	A344	Contains the starting bank number of EM file memory (bank number of the first formatted bank). This number is read when starting to write data from a Memory Card. If the largest bank number for which there is an EM file for simple backup (BACKUPE□.IOM, where represents consecutive bank numbers) is the same as the largest bank number supported by the CPU Unit, the EM Area will be formatted as file memory using the value in A344. If the maximum bank numbers are different, the EM Area will be returned to it's unformatted (not file memory) status.	Read-only
File Deletion Flags	A39506	The system automatically deleted the remainder of an EM file memory file that was being updated when a power interruption occurred.	Read-only
	A39507	The system automatically deleted the remainder of a Memory Card file that was being updated when a power interruption occurred.	Read-only
Simple Backup Write Capacity	A397	If a write for a simple backup operation fails, A397 will contain the Memory Card capacity that would have been required to complete the write operation. The value is in Kbytes. (This indicates that the Memory Card did not have the specified capacity when the write operation was started.) 0001 to FFFF Hex: Write error (value indicates required capacity from 1 to 65,535 Kbytes). A397 will be cleared to 0000 Hex when the write is completed successfully for a simple backup operation.	Read-only
Program Replacement End Code	A65000 to A65007	Normal End (i.e., when A65014 is OFF) 01 Hex: Program file (.OBJ) replaced. Error End (i.e., when A65014 is ON) 00 Hex: Fatal error 01 Hex: Memory error 11 Hex: Write-protected 12 Hex: Program replacement password error 21 Hex: No Memory Card 22 Hex: No such file 23 Hex: Specified file exceeds capacity (memory error). 31 Hex: One of the following in progress: File memory operation User program write Operating mode change	Read-only
Replacement Error Flag	A65014	ON when the Replacement Start Bit (A65015) has been turned ON to replace the program, but there is an error. If the Replacement Start Bit is turned ON again, the Replacement Error Flag will be turned OFF.	Read/write

Name	Address	Description	Access
Replacement Start Bit	A65015	Program replacement starts when the Replacement Start Bit is turned ON if the Program Password (A651) is valid (A5A5 Hex). Do not turn OFF the Replacement Start Bit during program replacement. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error. It is possible to confirm if program replacement is being executed by reading the Replacement Start Bit using a Programming Device, PT, or host computer.	Read/write
Program Password	A651	Input the password to replace a program. A5A5 Hex: Replacement Start Bit (A65015) is enabled. Any other value: Replacement Start Bit (A65015) is disabled. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error.	Read/write
Program File Name	A654 to A657	When program replacement starts, the program file name will be stored in ASCII. File names can be specified up to eight characters in length excluding the extension. File names are stored in the following order: A654 to A657 (i.e., from the lowest word to the highest), and from the highest byte to the lowest. If a file name is less than eight characters, the lowest remaining bytes and the highest remaining word will be filled with spaces (20 Hex). Null characters and space characters cannot be used within file names. Example: File name is ABC.OBJ 	Read/write

Program Error Information

Name	Address	Description	Access
Program Error Flag (Fatal error)	A40109	ON when program contents are incorrect. CPU Unit operation will stop.	Read-only
Program Error Task	A294	Provides the type and number of the tack that was being executed when program execution stops as a result of a program error.	Read-only
Instruction Processing Error Flag	A29508	This flag and the Error Flag (ER) will be turned ON when an instruction processing error has occurred and the PC Setup has been set to stop operation for an instruction error.	Read-only
Indirect DM/EM BCD Error Flag	A29509	This flag and the Access Error Flag (AER) will be turned ON when an indirect DM/EM BCD error has occurred and the PC Setup has been set to stop operation an indirect DM/EM BCD error.	Read-only
Illegal Access Error Flag	A29510	This flag and the Access Error Flag (AER) will be turned ON when an illegal access error has occurred and the PC Setup has been set to stop operation an illegal access error.	Read-only
No END Error Flag	A29511	ON when there isn't an END(001) instruction in each program within a task.	Read-only
Task Error Flag	A29512	ON when a task error has occurred. The following conditions will generate a task error. 1) There isn't an executable cyclic task. 2) There isn't a program allocated to the task.	Read-only
Differentiation Overflow Error Flag	A29513	ON when the specified Differentiation Flag Number exceeds the allowed value.	Read-only
Illegal Instruction Error Flag	A29514	ON when a program that cannot be executed has been stored.	Read-only
UM Overflow Error Flag	A29515	ON when the last address in UM (user program memory) has been exceeded.	Read-only
Program Address Where Program Stopped	A298 and A299	These words contain the 8-digit hexadecimal program address of the instruction where program execution was stopped due to a program error. (A299 contains the leftmost digits.)	Read-only

Error Information

■ Error Log, Error Code

Name	Address	Description	Access
Error Log Area	A100 to A199	When an error has occurred, the error code, error contents, and error's time and date are stored in the Error Log Area.	Read-only
Error Log Pointer	A300	When an error occurs, the Error Log Pointer is incremented by 1 to indicate the location where the next error record will be recorded as an offset from the beginning of the Error Log Area (A100).	Read-only
Error Log Pointer Reset Bit	A50014	Turn this bit ON to reset the Error Log Pointer (A300) to 00.	Read/write
Error Code	A400	When a non-fatal error (user-defined FALS(006) or system error) or a fatal error (user-defined FALS(007) or system error) occurs, the 4-digit hexadecimal error code is written to this word.	Read-only

■ **FAL/FALS Error Information**

Name	Address	Description	Access
FAL Error Flag (Non-fatal error)	A40215	ON when a non-fatal error is generated by executing FAL(006).	Read-only
Executed FAL Number Flags	A360 to A391	The flag corresponding to the specified FAL number will be turned ON when FAL(006) is executed. Bits A36001 to A39115 correspond to FAL numbers 001 to 511.	Read-only
FALS Error Flag (Fatal error)	A40106	ON when a fatal error is generated by the FALS(007) instruction.	Read-only
FAL/FALS Number for System Error Simulation (CJ1-H CPU Units only)	A053	Set a dummy FAL/FALS number to use to simulate the system error using FAL(006) or FALS(007). 0001 to 01FF Hex: FAL/FALS numbers 1 to 511 0000 or 0200 to FFFF Hex: No FAL/FALS number for system error simulation. (No error will be generated.)	Read/write

■ **Memory Error Information**

Name	Address	Description	Access
Memory Error Flag (Fatal error)	A40115	ON when an error occurred in memory or there was an error in automatic transfer from the Memory Card when the power was turned ON. The ERR/ALM indicator on the front of the CPU Unit will light and CPU Unit operation will stop when this flag turns ON. If the automatic data transfer at startup fails, A40309 will be turned ON. If an error occurs in automatic transfer at startup, this error cannot be cleared.	Read-only
Memory Error Location	A40300 to A40308	When a memory error occurs, the Memory Error Flag (A40115) is turned ON and one of the following flags is turned ON to indicate the memory area where the error occurred. A40300: User program A40304: PC Setup A40305: Registered I/O Table A40307: Routing Table A40308: CJ-series CPU Bus Unit Settings	Read-only
Startup Memory Card Transfer Error Flag	A40309	ON when an error occurs in automatically transferring a file from the Memory Card to the CPU Unit at startup, including when a file is missing or a Memory Card is not mounted. The error can be cleared by turning OFF the power. (This error cannot be cleared while the power is ON.)	Read-only
Flash Memory Error (CJ1-H CPU Units only)	A40310	Turns ON when the flash memory fails.	Read-only

■ **PC Setup Error Information**

Name	Address	Description	Access
PC Setup Error Flag (Non-fatal error)	A40210	ON when there is a setting error in the PC Setup.	Read-only
PC Setup Error Location	A406	When there is a setting error in the PC Setup, the location of that error is written to A406 in 16 bits binary. The location is given as the address set on the Programming Console.	Read-only

■ **Interrupt Task Error Information**

Name	Address	Description	Access
Interrupt Task Error Flag (Non-fatal error)	A40213	ON when the Detect Interrupt Task Errors setting in the PC Setup is set to “Detect” and one of the following occurs. IORD(222) or IOWR(223) in a cyclic task are competing with IORD(222) or IOWR(223) in an interrupt task. IORD(222) or IOWR(223) was executed in an interrupt task when I/O was being refreshed.	Read-only
Interrupt Task Error Cause Flag	A42615	Indicates the cause of an Interrupt Task Error.	Read-only
Interrupt Task Error, Task Number	A42600 to A42611	The function of these bits depends upon the status of A42615 (the Interrupt Task Error Flag). A42615 ON: Contains the Special I/O Unit’s unit number when an attempt was made to refresh a Special I/O Unit’s I/O from an interrupt task with IORF(097) while the Unit’s I/O was being refreshed by cyclic I/O refreshing (duplicate refreshing).	Read-only

■ **I/O Information**

Name	Address	Description	Access
Basic I/O Unit Error Flag (Non-fatal error)	A40212	ON when an error has occurred in a Basic I/O Unit (including C200H Group-2 High-density I/O Units and C200H Interrupt Input Units).	Read-only
Basic I/O Unit Error, Slot Number	A40800 to A40807	Contains the binary slot number where the error occurred when an error has occurred in a Basic I/O Unit (including C200H Group-2 High-density I/O Units and C200H Interrupt Input Units).	Read-only
Basic I/O Unit Error, Rack Number	A40808 to A40815	Contains the binary rack number where the error occurred when an error has occurred in a Basic I/O Unit (including C200H Group-2 High-density I/O Units and C200H Interrupt Input Units).	Read-only
I/O Setting Error Flag (Fatal error)	A40110	ON when an Input Unit has been installed in an Output Unit’s slot or vice-versa, so the Input and Output Units clash in the registered I/O table.	Read-only
Expansion I/O Rack Number Duplication Flags	A40900 to A40903	The corresponding flag will be turned ON when an Expansion I/O Rack’s starting word address was set from a Programming Device and two Racks have overlapping word allocations or a Rack’s starting address exceeds CIO 0901. Bits 00 to 07 correspond to Racks 0 to 3.	Read-only
Too Many I/O Points Flag (Fatal error)	A40111	ON when the number of I/O points being used in Basic I/O Units exceeds the maximum allowed for the PC.	Read-only
Too Many I/O Points, Details	A40700 to A40712	The three possible causes of the Too Many I/O Points Error are listed below. The 3-digit binary value in A40713 to A40715 indicates the cause of the error. The number of I/O points will be written here when the total number of I/O points set in the I/O Table (excluding Slave Racks) exceed the maximum allowed for the CPU Unit. The number of interrupt inputs will be written here when there are more than 32 interrupt inputs. The number of Racks will be written here when the number of Expansion I/O Racks exceeds the maximum.	Read-only
Too Many I/O Points, Cause	A40713 to A40715	These three bits indicate the cause of the Too Many I/O Points Error. (See A40700 to A40712.) 000 (0): Too many I/O points. 001 (1): Too many Interrupt Input points. 101 (5): Too many Expansion Racks connected. 111 (7): Too many Units are connected to one rack (more than 10).	Read-only

Name	Address	Description	Access
I/O Bus Error Flag (Fatal error)	A40114	ON when an error occurs in a data transfer between the CPU Unit and a Unit mounted to a slot or the End Cover is not connected to the CPU Rack or an Expansion Rack.	Read-only
I/O Bus Error Slot Number	A40400 to A40407	Contains the 8-bit binary slot number (00 to 09) where an I/O Bus Error occurred. Contain 0E Hex of the End Cover is not connected to the CPU Rack or an Expansion Rack.	Read-only
CPU Bus Unit Setup Area Initialization Error Flag	A26100	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	Read-only
I/O Overflow Flag	A26102	ON: Overflow in maximum number of I/O points. Turns OFF when I/O tables are generated normally.	Read-only
Duplication Error Flag	A26103	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.	Read-only
I/O Bus Error Flag	A26104	ON: I/O bus error Turns OFF when I/O tables are generated normally.	Read-only
Special I/O Unit Error Flag	A26107	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.	Read-only
I/O Unconfirmed Error Flag	A26109	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.	Read-only
I/O Bus Error Rack Number	A40408 to A40415	Contains the 8-bit binary rack number (00 to 07) where an I/O Bus Error occurred.	Read-only
Duplication Error Flag (Fatal error)	A40113	ON in the following cases: Two CPU Bus Units have been assigned the same unit number. Two Special I/O Units have been assigned the same unit number. Two Basic I/O Units have been allocated the same data area words. The same rack number is set for more than one Expansion Rack.	Read-only
Interrupt Input Unit Position Error Flag (CJ1-H CPU Units only)	A40508	ON when the Interrupt Input Unit is not connected in one of the five positions (slots 0 to 4) next to the CPU Unit on the CPU Rack.	Read-only

■ CPU Bus Unit Information

Name	Address	Description	Access
CPU Bus Unit Number Duplication Flags	A41000 to A41015	The Duplication Error Flag (A40113) and the corresponding flag in A410 will be turned ON when a CPU Bus Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Error, Unit Number Flags	A41700 to A41715	When an error occurs in a data exchange between the CPU Unit and a CPU Bus Unit, the CPU Bus Unit Error Flag (A40207) and the corresponding flag in A417 are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Setting Error, Unit Number Flags	A42700 to A42715	When a CPU Bus Unit Setting Error occurs, A40203 and the corresponding flag in A427 are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Setting Error Flag (Non-fatal error)	A40203	ON when an installed CPU Bus Unit does not match the CPU Bus Unit registered in the I/O table.	Read-only
CPU Bus Unit Error Flag (Non-fatal error)	A40207	ON when an error occurs in a data exchange between the CPU Unit and a CPU Bus Unit (including an error in the CPU Bus Unit itself).	Read-only

■ **Special I/O Unit Information**

Name	Address	Description	Access
Special I/O Unit Number Duplication Flags	A41100 to A41615	The Duplication Error Flag (A40113) and the corresponding flag in A411 through A416 will be turned ON when a Special I/O Unit's unit number has been duplicated. (Bits A41100 to A41615 correspond to unit numbers 0 to 95.)	Read-only
Special I/O Unit Setting Error Flag (Non-fatal error)	A40202	ON when an installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table.	Read-only
Special I/O Unit Setting Error, Unit Number Flags	A42800 to A43315	When a Special I/O Unit Setting Error occurs, A40202 and the corresponding flag in these words are turned ON. (Bits A42800 to A43315 correspond to unit numbers 0 to 95.)	Read-only
Special I/O Unit Error Flag (Non-fatal error)	A40206	ON when an error occurs in a data exchange between the CPU Unit and a Special I/O Unit (including an error in the Special I/O Unit itself).	Read-only
Special I/O Unit Error, Unit Number Flags	A41800 to A42315	When an error occurs in a data exchange between the CPU Unit and a Special I/O Unit, the Special I/O Unit Error Flag (A40206) and the corresponding flag in these words are turned ON. (Bits A42800 to A43315 correspond to unit numbers 0 to 95.)	Read-only

■ **Other PC Operating Information**

Name	Address	Description	Access
Battery Error Flag (Non-fatal error)	A40204	ON if the CPU Unit's battery is disconnected or its voltage is low and the PC Setup has been set to detect this error. (Detect Low Battery)	Read-only
Cycle Time Too Long Flag (Fatal error)	A40108	ON if the cycle time exceeds the maximum cycle time set in the PC Setup. In the Parallel Processing Modes, the program execution cycle time will be used. (Watch Cycle Time)	Read-only
Peripheral Servicing Too Long Flag (Fatal error, CJ1-H CPU Unit only)	A40515	Turns ON when the peripheral servicing time in a Parallel Processing Mode exceeds 2 s. This will also cause a cycle time error and operation will stop.	Read-only
FPD Teaching Bit	A59800	Turn this bit ON to set the monitoring time in FPD(269) automatically with the teaching function.	Read/write
Memory Backup Battery Failure Flag	A39511	Data from the I/O memory areas that are maintained when power is turned OFF (HR, DM, etc.) are backed up with a Battery. A39511 turns ON if the Battery voltage drops and the data can no longer be maintained. The data in the I/O memory will not be dependable when this happens.	Read-only

Clock

■ Clock Information

Name	Address	Description	Access
Clock Data	The clock data from the clock built into the CPU Unit is stored here in BCD.		Read-only
	A35100 to A35107	Seconds: 00 to 59 (BCD)	Read-only
	A35108 to A35115	Minutes: 00 to 59 (BCD)	Read-only
	A35200 to A35207	Hour: 00 to 23 (BCD)	Read-only
	A35208 to A35215	Day of the month: 01 to 31 (BCD)	Read-only
	A35300 to A35307	Month: 01 to 12 (BCD)	Read-only
	A35308 to A35315	Year: 00 to 99 (BCD)	Read-only
	A35400 to A35407	Day of the week: 00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday	Read-only

■ Power Supply Information

Name	Address	Description	Access
Startup Time	A510 and A511	These words contain the time (in BCD) at which the power was turned ON. The contents are updated every time that the power is turned ON. A51000 to A51007: Seconds (00 to 59) A51008 to A51015: Minutes (00 to 59) A51100 to A51107: Hour (00 to 23) A51108 to A51115: Day of the month (00 to 31)	Read/write
Power Interruption Time	A512 and A513	These words contain the time (in BCD) at which the power was interrupted. The contents are updated every time that the power is interrupted. A51200 to A51207: Seconds (00 to 59) A51208 to A51215: Minutes (00 to 59) A51300 to A51307: Hour (00 to 23) A51308 to A51315: Day of month (00 to 31)	Read/write
Number of Power Interruptions	A514	Contains the number of times (in binary) that power has been interrupted since the power was first turned on. To reset this value, overwrite the current value with 0000.	Read/write
Total Power ON Time	A523	Contains the total time (in binary) that the PC has been on in 10-hour units. The data is stored is updated every 10 hours. To reset this value, overwrite the current value with 0000.	Read/write

Flash Memory Backup Information

Name	Address	Description	Access
User Program Date (CJ1-H CPU Units only)	A090 to A093	These words contain in BCD the date and time that the user program was last overwritten. A09000 to A09007: Seconds (00 to 59) A09008 to A09015: Minutes (00 to 59) A09100 to A09107: Hour (00 to 23) A09108 to A09115: Day of month (00 to 31) A09200 to A09207: Month (01 to 12) A09208 to A09215: Year (00 to 99) A09308 to A09307: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	Read-only
Parameter Date (CJ1-H CPU Units only)	A094 to A0947	These words contain in BCD the date and time that the parameters were last overwritten. A09400 to A09407: Seconds (00 to 59) A09408 to A09415: Minutes (00 to 59) A09500 to A09507: Hour (00 to 23) A09508 to A09515: Day of month (00 to 31) A09600 to A09607: Month (01 to 12) A09608 to A09615: Year (00 to 99) A09708 to A09707: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	Read-only

Communications

■ Network Communications Information

Name	Address	Description	Access
Communications Port Enabled Flags	A20200 to A20207	ON when a network instruction (SEND, RECV, CMND, or PMCR) can be executed with the corresponding port number or background execution can be executed with the corresponding port number (CJ1-H CPU Units only). Bits 00 to 07 correspond to communications ports 0 to 7 When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated, and the corresponding flag will be turned ON during the operation and turned OFF when the operation has been completed.	Read-only
Communications Port Completion Codes	A203 to A210	These words contain the completion codes for the corresponding port numbers when network instructions (SEND, RECV, CMND, or PMCR) have been executed. The contents will be cleared when background execution has been completed (for CJ1-H CPU Unit only). Words A203 to A210 correspond to communications ports 0 to 7. When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated, and a completion code will be stored in the corresponding word.	Read-only
Communications Port Error Flags	A21900 to A21907	ON when an error occurred during execution of a network instruction (SEND, RECV, CMND, or PMCR). Turns OFF then execution has been finished normally. Bits 00 to 07 correspond to communications ports 0 to 7. When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated. The corresponding flag will be turned ON if an error occurs and will be turned OFF if the simple backup operation ends normally.	Read-only

■ **Peripheral Port Communications Information**

Name	Address	Description	Access
Peripheral Port Communications Error Flag	A39212	ON when a communications error has occurred at the peripheral port.	Read-only
Peripheral Port Restart Bit	A52601	Turn this bit ON to restart the peripheral port.	Read/write
Peripheral Port Settings Change Bit	A61901	ON while the peripheral port's communications settings are being changed.	Read/write
Peripheral Port Error Flags	A52808 to A52815	These flags indicate what kind of error has occurred at the peripheral port.	Read/write
Peripheral Port PT Communications Flags	A39400 to A39407	The corresponding bit will be ON when the peripheral port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
Peripheral Port PT Priority Registered Flags	A39408 to A39415	The corresponding bit will be ON for the PT that has priority when the peripheral port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only

■ **RS-232C Port Communications Information**

Name	Address	Description	Access
RS-232C Port Communications Error Flag	A39204	ON when a communications error has occurred at the RS-232C port.	Read-only
RS-232C Port Restart Bit	A52600	Turn this bit ON to restart the RS-232C port.	Read/write
RS-232C Port Settings Change Bit	A61902	ON while the RS-232C port's communications settings are being changed.	Read/write
RS-232C Port Error Flags	A52800 to A52807	These flags indicate what kind of error has occurred at the RS-232C port.	Read/write
RS-232C Port Send Ready Flag (No-protocol mode)	A39205	ON when the RS-232C port is able to send data in no-protocol mode.	Read-only
RS-232C Port Reception Completed Flag (No-protocol mode)	A39206	ON when the RS-232C port has completed the reception in no-protocol mode.	Read-only
RS-232C Port Reception Overflow Flag (No-protocol mode)	A39207	ON when a data overflow occurred during reception through the RS-232C port in no-protocol mode.	Read-only
RS-232C Port PT Communications Flags	A39300 to A39307	The corresponding bit will be ON when the RS-232C port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
RS-232C Port PT Priority Registered Flags	A39308 to A39315	The corresponding bit will be ON for the PT that has priority when the RS-232C port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
RS-232C Port Reception Counter (No-protocol mode)	A39300 to A39315	Indicates (in binary) the number of bytes of data received when the RS-232C port is in no-protocol mode.	Read-only

■ **Serial Device Communications Information**

Name	Address	Description	Access
Communications Units 0 to 15, Ports 1 to 4 Settings Change Bits	A62001 to A63504	The corresponding flag will be ON when the settings for that port are being changed. (Bits 1 to 4 in A620 to A635 correspond to ports 1 to 4 in Communications Units 0 to 15.)	Read/write

Instruction-related Information

Name	Address	Description	Access
Step Flag	A20012	ON for one cycle when step execution is started with STEP(008).	Read-only
Current EM Bank	A301	This word contains the current EM bank number in 4-digit hexadecimal.	Read-only
Macro Area Input Words	A600 to A603	When MCRO(099) is executed, it copies the input data from the specified source words (input parameter words) to A600 through A603.	Read/write
Macro Area Output Words	A604 to A607	After the subroutine specified in MCRO(099) has been executed, the results of the subroutine are transferred from A604 through A607 to the specified destination words (output parameter words).	Read/write

Background Execution Information

Name	Address	Description	Access
DR00 Output for Background Execution (CJ1-H CPU Units only)	A597	When a data register is specified as the output for an instruction processed in the background, A597 receives the output instead of DR00. 0000 to FFFF Hex	Read-only
IR00 Output for Background Execution (CJ1-H CPU Units only)	A595 and A596	When an index register is specified as the output for an instruction processed in the background, A595 and A596 receive the output instead of IR00. 0000 0000 to FFFF FFFF Hex (A596 contains the leftmost digits.)	Read-only
Equals Flag for Background Execution (CJ1-H CPU Units only)	A59801	Turns ON if matching data is found for an SRCH(181) instruction executed in the background.	Read-only
ER/AER Flag for Background Execution (CJ1-H CPU Units only)	A39510	Turns ON if an error or illegal access occurs during background execution. Turns OFF when power is turned ON or operation is started.	Read-only

9-11 TR (Temporary Relay) Area

The TR Area contains 16 bits with addresses ranging from TR0 to TR15. These temporarily store the ON/OFF status of an instruction block for branching. TR bits are useful when there are several output branches and interlocks cannot be used.

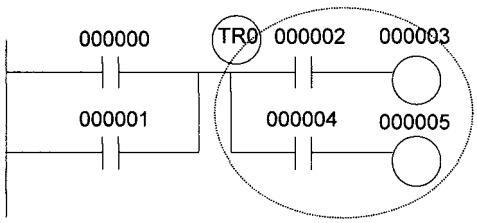
The TR bits can be used as many times as required and in any order required as long as the same TR bit is not used twice in the same instruction block.

TR bits can be used only with the OUT and LD instructions. OUT instructions (OUT TR0 to OUT TR15) store the ON OFF status of a branch point and LD instructions recall the stored ON OFF status of the branch point.

TR bits cannot be changed from a Programming Device.

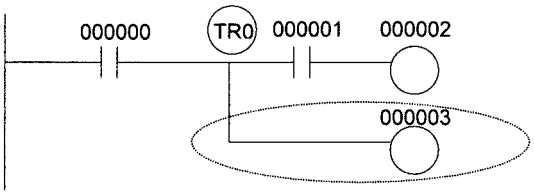
Examples

In this example, a TR bit is used when two outputs have been directly connected to a branch point.



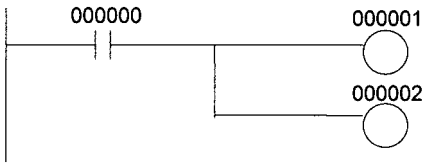
Instruction	Operand
LD	000000
OR	000001
OUT	TR 0
AND	000002
OUT	000003
LD	TR 0
AND	000004
OUT	000005

In this example, a TR bit is used when an output is connected to a branch point without a separate execution condition.

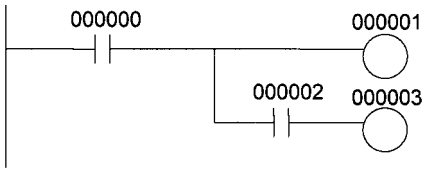


Instruction	Operand
LD	000000
OUT	TR 0
AND	000001
OUT	000002
LD	TR 0
OUT	000003

Note A TR bit is not required when there are no execution conditions after the branch point or there is an execution condition only in the last line of the instruction block.



Instruction	Operand
LD	000000
OUT	000001
OUT	000002



Instruction	Operand
LD	000000
OUT	000001
AND	000002
OUT	000003

9-12 Timer Area

The 4,096 timer numbers (T0000 to T4095) are shared by the TIM, TIMH(015), TMHH(540), TTIM(087), TIMW(813), and TMHW(815) instructions. Timer Completion Flags and present values (PVs) for these instructions are accessed with the timer numbers. (The TIML(542) and MTIM(543) instructions do not use timer numbers.)

When a timer number is used in an operand that requires bit data, the timer number accesses the Completion Flag of the timer. When a timer number is used in an operand that requires word data, the timer number accesses the PV of the timer. Timer Completion Flags can be used as often as necessary as normally open and normally closed conditions and the values of timer PVs can be read as normal word data.

Note It is not recommended to use the same timer number in two timer instructions because the timers will not operate correctly if they are timing simultaneously. (If two or more timer instructions use the same timer number, an error will be generated during the program check, but the timers will operate as long as the instructions are not executed in the same cycle.)

The following table shows when timer PVs and Completion Flags will be reset.

Instruction name	Effect on PV and Completion Flag			Operation in Jumps and Interlocks	
	Mode change[1]	PC start-up[1]	CNR(545)	Jumps (JMP-JME) or Tasks on standby	Interlocks (IL-ILC)
TIMER: TIM	PV → 0 Flag → OFF	PV → 0 Flag → OFF	PV → 9999 Flag → OFF	PVs refreshed in operating timers	PV → SV (Reset to SV.) Flag → OFF
HIGH-SPEED TIMER: TIMH(015)					
ONE-MS TIMER: TMHH(540)					
ACCUMULATIVE TIMER: TTIM(087)				PV Maintained	PV Maintained
TIMER WAIT: TIMW(813)				PVs refreshed in operating timers	---
HIGH-SPEED TIMER WAIT: TMHW(815)					---

Note

1. If the IOM Hold BIt (A50012) is ON, the PV and Completion Flag will be retained when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa. The PV and Completion Flag will be cleared when power is cycled.
2. If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the PV and Completion Flag will be retained when the PC's power is cycled.
3. Since the TIML(542) and MTIM(543) instructions do not use timer numbers, they are reset under different conditions. Refer to the descriptions of these instructions for details.
4. The present value of TIM, TIMH(015), TMHH(540), TIMW(813), and TMHW(815) timers programmed with timer numbers 0000 to 2047 will be updated even when jumped between JMP and JME instructions or when in a task that is on standby. The present value of timers programmed with timer numbers 2048 to 4095 will be held when jumped or when in a task that is on standby.

Timer Completion Flags can be force-set and force-reset.

Timer PVs cannot be force-set or force-reset, although the PVs can be refreshed indirectly by force-setting/resetting the Completion Flag.

There are no restrictions in the order of using timer numbers or in the number of N.C. or N.O. conditions that can be programmed. Timer PVs can be read as word data and used in programming.

9-13 Counter Area

The 4,096 counter numbers (C0000 to C4095) are shared by the CNT, CNTR(012), and CNTW(814) instructions. Counter Completion Flags and present values (PVs) for these instructions are accessed with the counter numbers.

When a counter number is used in an operand that requires bit data, the counter number accesses the Completion Flag of the counter. When a counter number is used in an operand that requires word data, the counter number accesses the PV of the counter.

It is not recommended to use the same counter number in two counter instructions because the counters will not operate correctly if they are counting simultaneously. If two or more counter instructions use the same counter

number, an error will be generated during the program check, but the counters will operate as long as the instructions are not executed in the same cycle.

The following table shows when counter PVs and Completion Flags will be reset.

Instruction name	Effect on PV and Completion Flag					
	Reset	Mode change	PC startup	Reset Input	CNR(545)	Interlocks (IL-ILC)
COUNTER: CNT	PV → 0000	Maintained	Maintained	Reset	Reset	Maintained
REVERSIBLE COUNTER: CNTR(012)	Flag → OFF					
COUNTER WAIT: CNTW(814)						

Counter Completion Flags can be force-set and force-reset.

Counter PVs cannot be force-set or force-reset, although the PVs can be refreshed indirectly by force-setting/resetting the Completion Flag.

There are no restrictions in the order of using counter numbers or in the number of N.C. or N.O. conditions that can be programmed. Counter PVs can be read as word data and used in programming.

9-14 Data Memory (DM) Area

The DM Area contains 32,768 words with addresses ranging from D00000 to D32767. This data area is used for general data storage and manipulation and is accessible only by word.

Data in the DM Area is retained when the PC's power is cycled or the PC's operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

Although bits in the DM Area cannot be accessed directly, the status of these bits can be accessed with the BIT TEST instructions, TST(350) and TSTN(351).

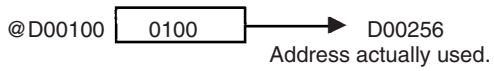
Bits in the DM Area cannot be force-set or force-reset.

Indirect Addressing

Words in the DM Area can be indirectly addressed in two ways: binary-mode and BCD-mode.

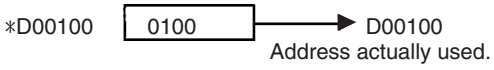
Binary-mode Addressing (@D)

When a "@" character is input before a DM address, the content of that DM word is treated as binary and the instruction will operate on the DM word at that binary address. The entire DM Area (D00000 to D32767) can be indirectly addressed with hexadecimal values 0000 to 7FFF.



BCD-mode Addressing (*D)

When a "*" character is input before a DM address, the content of that DM word is treated as BCD and the instruction will operate on the DM word at that BCD address. Only part of the DM Area (D00000 to D09999) can be indirectly addressed with BCD values 0000 to 9999.



DM Area Allocation to Special I/O Units

Parts of the DM Area are allocated to Special I/O Units and CPU Bus Units for functions such as initial Unit settings. The timing for data transfers is different for these Units, but may occur at any of the three following times.

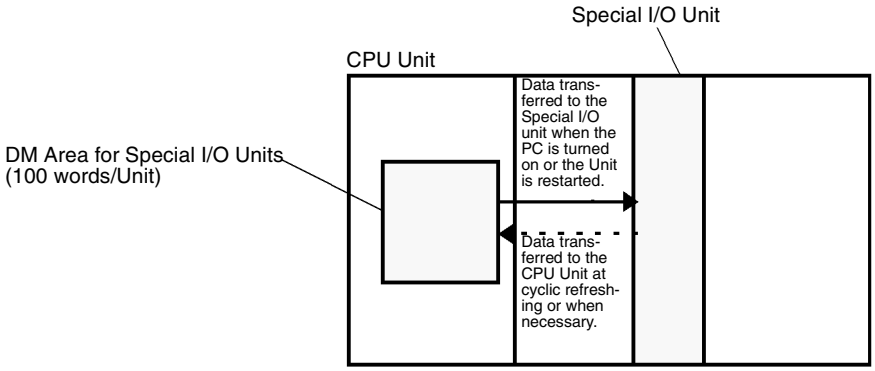
1,2,3...

1. Transfer data when the PC's power is turned ON or the Unit is restarted.
2. Transfer data once each cycle.
3. Transfer data when required.

Refer to the Unit's operation manual for details on data transfer timing.

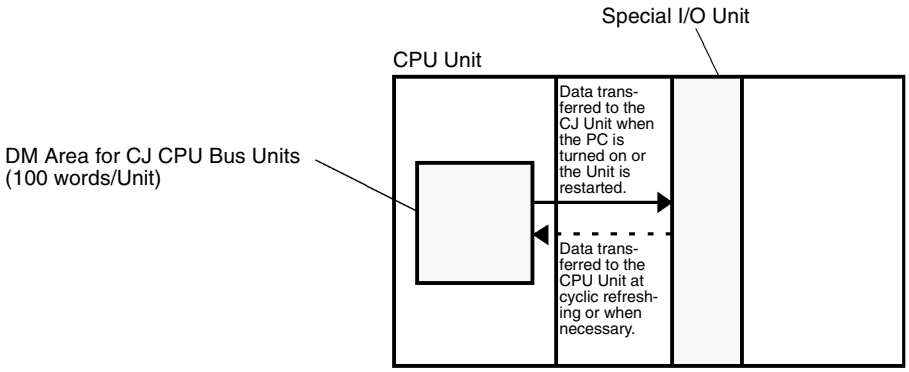
Special I/O Units (D20000 to D29599)

Each Special I/O Unit is allocated 100 words (based on unit numbers 0 to 95). Refer to the Unit's Operation Manual for details on the function of these words.



CPU Bus Units (D30000 to D31599)

Each CPU Bus Unit is allocated 100 words (based on unit numbers 0 to F). Refer to the Unit's Operation Manual for details on the function of these words. With some CPU Bus Units such as Ethernet Units, initial settings must be registered in the CPU Unit's Parameter Area; this data can be registered with a Programming Device other than a Programming Console.



9-15 Extended Data Memory (EM) Area

The EM Area is divided into 13 banks (0 to 2) that each contain 32,768 words. EM Area addresses range from E0_00000 to E2_32767. This data area is used for general data storage and manipulation and is accessible only by word.

Data in the EM Area is retained when the PC's power is cycled or the PC's operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

Although bits in the EM Area cannot be accessed directly, the status of these bits can be accessed with the BIT TEST instructions, TST(350) and TSTN(351).

Bits in the EM Area cannot be force-set or force-reset.

Specifying EM Addresses

There are two ways to specify an EM address: the bank and address can be specified at the same time or an address in the current bank can be specified (after changing the current bank, if necessary). In general, we recommend specifying the bank and address simultaneously.

1,2,3...

1. Bank and Address Specification
   With this method, the bank number is specified just before the EM address. For example, E2_00010 specifies EM address 00010 in bank 2.
2. Current Bank Address Specification
   With this method, just the EM address is specified. For example, E00010 specifies EM address 00010 in the current bank. (The current bank must be changed with EMBC(281) to access data in another bank. A301 contains the current EM bank number.)

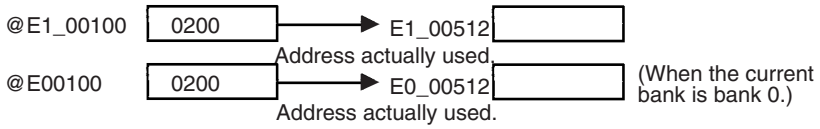
   The current bank will be reset to 0 when the operating mode is changed from PROGRAM mode to RUN/MONITOR mode, unless the IOM Hold Bit (A50012) is ON. The current bank is not changed as the program proceeds through cyclic tasks and the current bank will be returned to its original value (in the source cyclic task) if it has been changed in an interrupt task.

Indirect Addressing

Words in the EM Area can be indirectly addressed in two ways: binary-mode and BCD-mode.

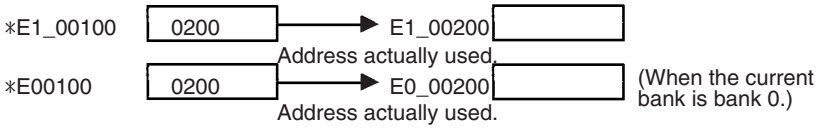
Binary-mode Addressing (@E)

When a "@" character is input before a EM address, the content of that EM word is treated as binary and the instruction will operate on the EM word in the same bank at that binary address. All of the words in the same EM bank (E00000 to E32767) can be indirectly addressed with hexadecimal values 0000 to 7FFF and words in the next EM bank (E00000 to E32767) can be addressed with hexadecimal values 8000 to FFFF.



BCD-mode Addressing (*E)

When a "*" character is input before a EM address, the content of that EM word is treated as BCD and the instruction will operate on the EM word in the same bank at that BCD address. Only part of the EM bank (E00000 to E09999) can be indirectly addressed with BCD values 0000 to 9999.

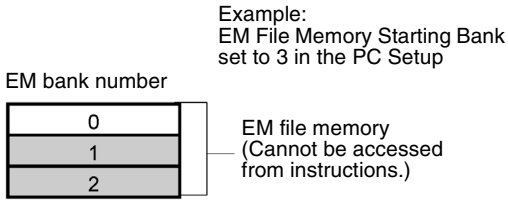


File Memory Conversion

Part of the EM Area can be converted for use as file memory with settings in the PC Setup. All EM banks from the specified bank (EM File Memory Starting Bank) to the last EM bank will be converted to file memory.

Once EM banks have been converted to file memory, they cannot be accessed (read or written) by instructions. An Illegal Access Error will occur if a file-memory bank is specified as an operand in an instruction.

The following example shows EM file memory when the EM File Memory Starting Bank has been set to 3 in the PC Setup.



9-16 Index Registers

The sixteen Index Registers (IR0 to IR15) are used for indirect addressing. Each Index Register can hold a single PC memory address, which is the absolute memory address of a word in I/O memory. Use MOVR(560) to convert a regular data area address to its equivalent PC memory address and write that value to the specified Index Register. (Use MOVRW(561) to set the PC memory address of a timer/counter PV in an Index Register.)

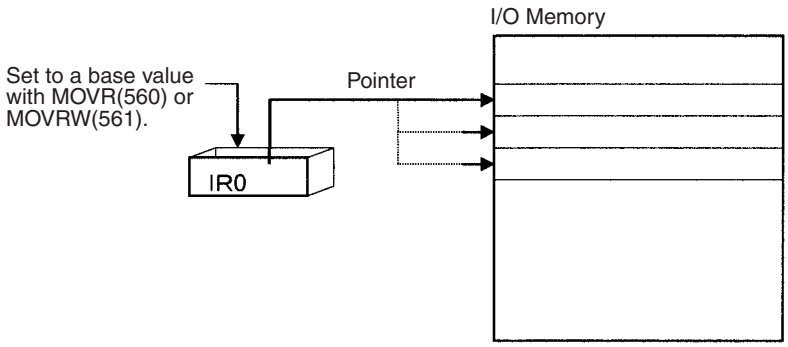
Note Refer to *Appendix E Memory Map* for more details on PC memory addresses.

Indirect Addressing

When an Index Register is used as an operand with a "," prefix, the instruction will operate on the word indicated by the PC memory address in the Index Register, not the Index Register itself. Basically, the Index Registers are I/O memory pointers.

- All addresses in I/O memory (except Index Registers, Data Registers, and Condition Flags) can be specified seamlessly with PC memory addresses. It isn't necessary to specify the data area.
- In addition to basic indirect addressing, the PC memory address in an Index Register can be offset with a constant or Data Register, auto-incremented, or auto-decremented. These functions can be used in loops to read or write data while incrementing or decrementing the address by one each time that the instruction is executed.

With the offset and increment/decrement variations, the Index Registers can be set to base values with MOVR(560) or MOVRW(561) and then modified as pointers in each instruction.



Note It is possible to specify regions outside of I/O memory and generate an Illegal Access Error when indirectly addressing memory with Index Registers. Refer to *Appendix E Memory Map* for details on the limits of PC memory addresses.

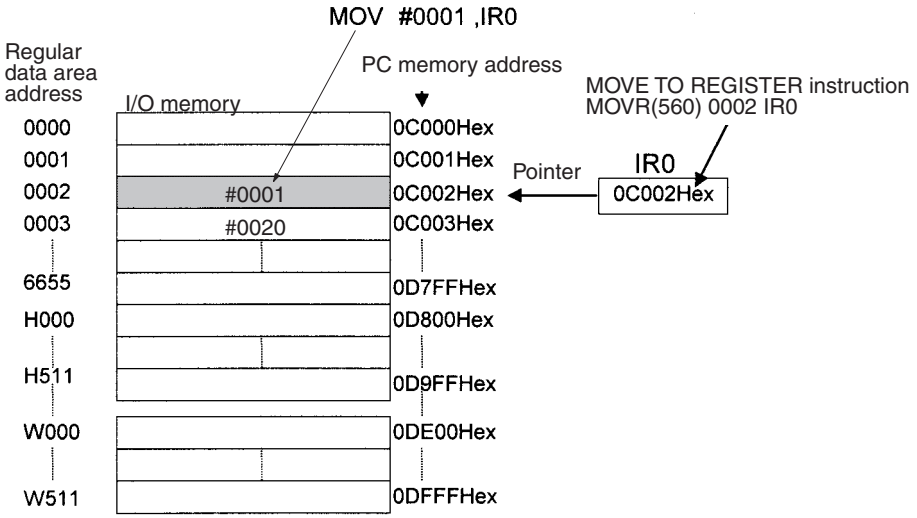
The following table shows the variations available when indirectly addressing I/O memory with Index Registers. (IR□ represents an Index Register from IR0 to IR15.)

Variation	Function	Syntax	Example	
Indirect addressing	The content of IR□ is treated as the PC memory address of a bit or word.	,IR□	LD ,IR0	Loads the bit at the PC memory address contained in IR0.
Indirect addressing with constant offset	The constant prefix is added to the content of IR□ and the result is treated as the PC memory address of a bit or word. The constant may be any integer from –2,048 to 2,047.	Constant ,IR□ (Include a + or – in the constant.)	LD +5,IR0	Adds 5 to the contents of IR0 and loads the bit at that PC memory address.
Indirect addressing with DR offset	The content of the Data Register is added to the content of IR□ and the result is treated as the PC memory address of a bit or word.	DR□,IR□	LD DR0,IR0	Adds the contents of DR0 to the contents of IR0 and loads the bit at that PC memory address.
Indirect addressing with auto-increment	After referencing the content of IR□ as the PC memory address of a bit or word, the content is incremented by 1 or 2.	Increment by 1: ,IR□+ Increment by 2: ,IR□++	LD , IR0++	Loads the bit at the PC memory address contained in IR0 and then increments the content of IR0 by 2.
Indirect addressing with auto-decrement	The content of IR□ is decremented by 1 or 2 and the result is treated as the PC memory address of a bit or word.	Decrement by 1: ,–IR□ Decrement by 2: ,– –IR□	LD , – –IR0	Decrements the content of IR0 by 2 and then loads the bit at that PC memory address.

Example

This example shows how to store the PC memory address of a word (CIO 0002) in an Index Register (IR0), use the Index Register in an instruction, and use the auto-increment variation.

MOVR(560)	0002	IR0	Stores the PC memory address of CIO 0002 in IR0.
MOV(021)	#0001	,IR0	Writes #0001 to the PC memory address contained in IR0.
MOV(021)	#0020	+1,IR0	Reads the content of IR0, adds 1, and writes #0020 to that PC memory address.



Note The PC memory addresses are listed in the diagram above, but it isn't necessary to know the PC memory addresses when using Index Registers.

Since some operands are treated as word data and others are treated as bit data, the meaning of the data in an Index Register will differ depending on the operand in which it is used.

1,2,3... 1. Word Operand:

```
MOVR(560)    0000      IR2
MOV(021)     D00000    , IR2
```

When the operand is treated as a word, the contents of the Index Register are used "as is" as the PC memory address of a word.
In this example MOVR(560) sets the PC memory address of CIO 0002 in IR2 and the MOV(021) instruction copies the contents of D00000 to CIO 0002.

2. Bit Operand:

```
MOVR(560)    000013    ,IR2
SET          +5 , IR2
```

When the operand is treated as a bit, the leftmost 7 digits of the Index Register specify the word address and the rightmost digit specifies the bit number. In this example, MOVR(560) sets the PC memory address of CIO 000013 (0C000D Hex) in IR2. The SET instruction adds +5 from bit 13 to this PC memory address, so it turns ON bit CIO 000102.

Direct Addressing

When an Index Register is used as an operand without a "," prefix, the instruction will operate on the contents of the Index Register itself (a two-word or "double" value). Index Registers can be directly addressed only in the instructions shown in the following table. Use these instructions to operate on the Index Registers as pointers.

The Index Registers cannot be directly addressed in any other instructions, although they can usually be used for indirect addressing.

Instruction group	Instruction name	Mnemonic
Data Movement Instructions	MOVE TO REGISTER	MOVR(560)
	MOVE TIMER/COUNTER PV TO REGISTER	MOVRW(561)
	DOUBLE MOVE	MOVL(498)
	DOUBLE DATA EXCHANGE	XCGL(562)
Table Data Processing Instructions	SET RECORD LOCATION	SETR(635)
	GET RECORD NUMBER	GETR(636)
Increment/Decrement Instructions	DOUBLE INCREMENT BINARY	++L(591)
	DOUBLE DECREMENT BINARY	– –L(593)
Comparison Instructions	DOUBLE EQUAL	=L(301)
	DOUBLE NOT EQUAL	< >L(306)
	DOUBLE LESS THAN	< L(311)
	DOUBLE LESS THAN OR EQUAL	< =L(316)
	DOUBLE GREATER THAN	> L(321)
	DOUBLE GREATER THAN OR EQUAL	> =L(326)
	DOUBLE COMPARE	CMPL(060)
Symbol Math Instructions	DOUBLE SIGNED BINARY ADD WITHOUT CARRY	+L(401)
	DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY	–L(411)

The SRCH(181), MAX(182), and MIN(183) instructions can output the PC memory address of the word with the desired value (search value, maximum, or minimum) to IR0. In this case, IR0 can be used in later instructions to access the contents of that word.

Index Register Initialization

The Index Registers will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.

IOM Hold Bit Operation

If the IOM Hold BIt (A50012) is ON, the Index Registers won't be cleared when a FALS error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the Index Registers won't be cleared when the PC's power supply is reset (ON → OFF → ON).

Precautions

Do not use Index Registers until a PC memory address has been set in the register. The pointer operation will be unreliable if the registers are used without setting their values.

The values in Index Registers are unpredictable at the start of an interrupt task. When an Index Register will be used in an interrupt task, always set a PC memory address in the Index Register with MOVR(560) or MOVRW(561) before using the register in that task.

Each Index Register task is processed independently, so they do not affect each other. For example, IR0 used in Task 1 and IR0 used in Task 2 are different. Consequently, each Index Register task has 16 Index Registers.

Limitations when Using Index Registers

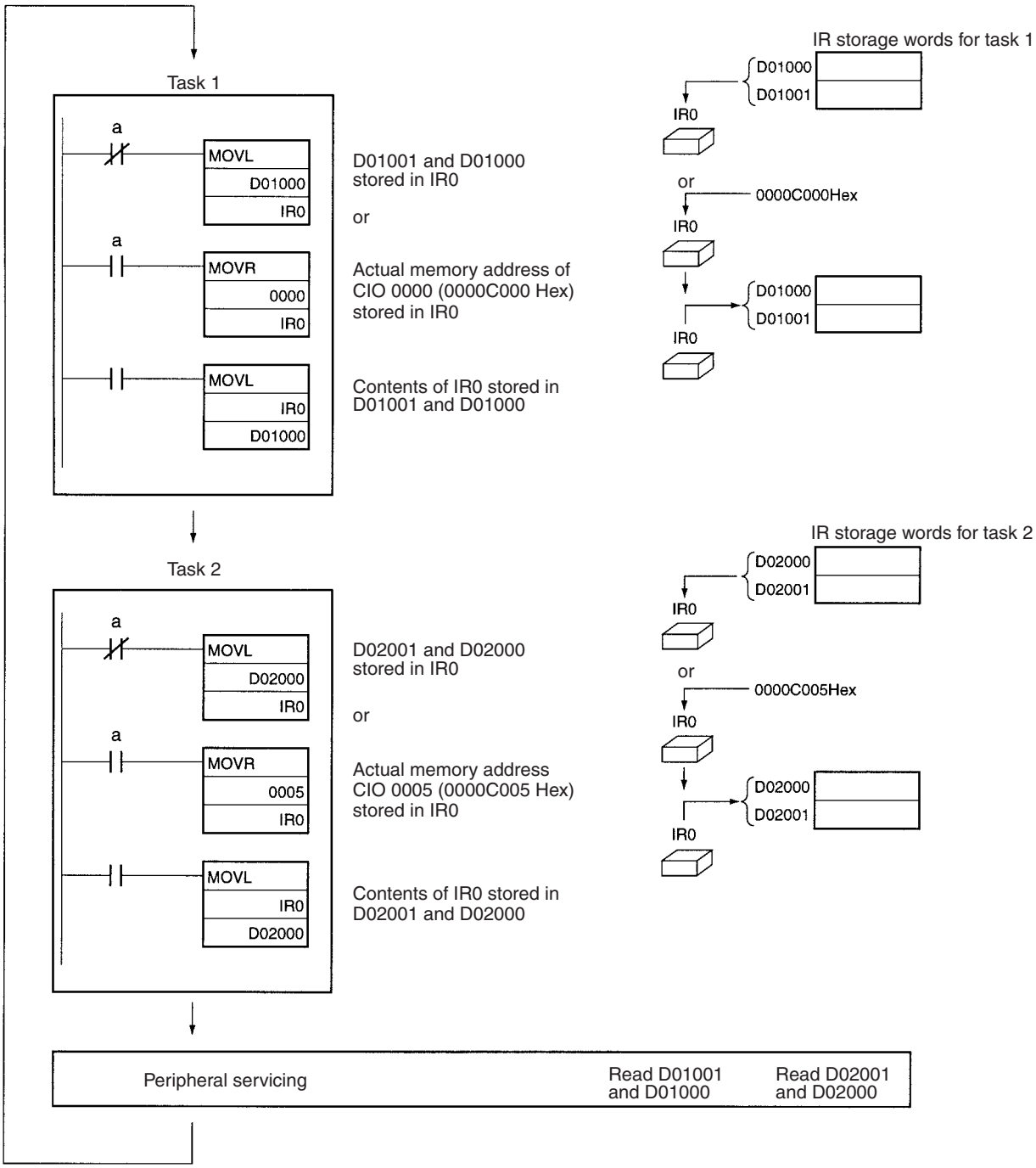
- It is only possible to read the Index Register for the last task executed within the cycle from the Programming Devices (CX-Programmer or Programming Console). If using Index Registers with the same number to perform multiple tasks, it is only possible with the Programming Devices to read the Index Register value for the last task performed within the cycle from the multiple tasks. Nor is it possible to write the Index Register value from the Programming Devices.
- It is not possible to either read or write to the Index Registers using Host Link commands or FINS commands.
- The Index Registers cannot be shared between tasks for CJ1 CPU Units. (With CJ1-H CPU Units, a PC Setup setting can be made from the CX-Programmer to share Index Registers between tasks.)

Monitoring Index Registers

It is possible to monitor Index Registers as follows:

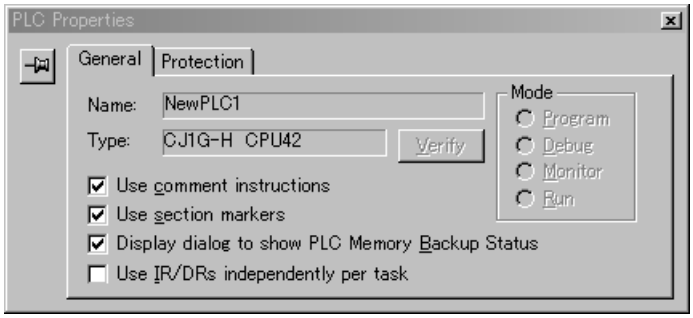
To use the Programming Devices to monitor the final Index Register values for each task, or to monitor the Index Register values using Host Link commands or FINS commands, write a program to store Index Register values from each task to another area (e.g., DM area) at the end of each task, and to read Index Register values from the storage words (e.g., DM area) at the beginning of each task. The values stored for each task in other areas (e.g., DM area) can then be edited using the Programming Devices, Host Link commands, or FINS commands.

Note Be sure to use PC memory addresses in Index Registers.



Sharing Index Registers with CJ1-H CPU Units

The following setting can be made from the PC properties dialog box on the CX-Programmer to control sharing index and data registers between tasks.



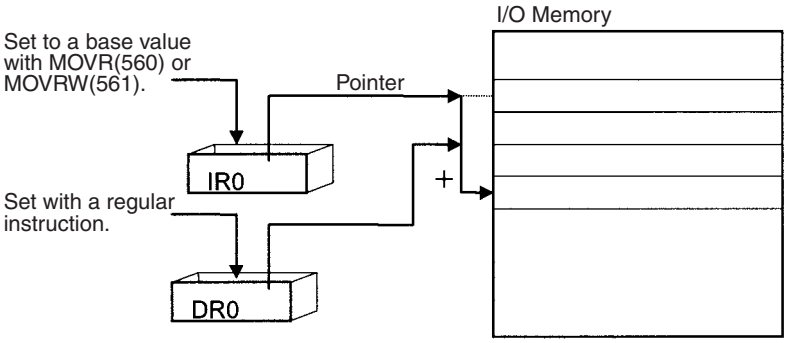
9-17 Data Registers

The sixteen Data Registers (DR0 to DR15) are used to offset the PC memory addresses in Index Registers when addressing words indirectly.

The value in a Data Register can be added to the PC memory address in an Index Register to specify the absolute memory address of a bit or word in I/O memory. Data Registers contain signed binary data, so the content of an Index Register can be offset to a lower or higher address.

Normal instructions can be use to store data in Data Registers.

Bits in Data Registers cannot be force-set and force-reset.



Examples

The following examples show how Data Registers are used to offset the PC memory addresses in Index Registers.

LD DR0 ,IR0	Adds the contents of DR0 to the contents of IR0 and loads the bit at that PC memory address.
MOV(021) #0001 DR0 ,IR1	Adds the contents of DR0 to the contents of IR1 and writes #0001 to that PC memory address.

Range of Values

The contents of data registers are treated as signed binary data and thus have a range of –32,768 to 32,767.

Hexadecimal content	Decimal equivalent
8000 to FFFF	–32,768 to –1
0000 to 7FFF	0 to 32,767

Data Register Initialization

The Data Registers will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.

2. The PC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PC Setup.

IOM Hold Bit Operation

If the IOM Hold BIt (A50012) is ON, the Data Registers won't be cleared when a FALS error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the Data Registers won't be cleared when the PC's power supply is reset (ON →OFF →ON).

Precautions

Data Registers are normally local to each task. For example, DR0 used in task 1 is different from DR0 used in task 2. (With CJ1-H CPU Units, a PC Setup setting can be made from the CX-Programmer to share Data Registers between tasks.)

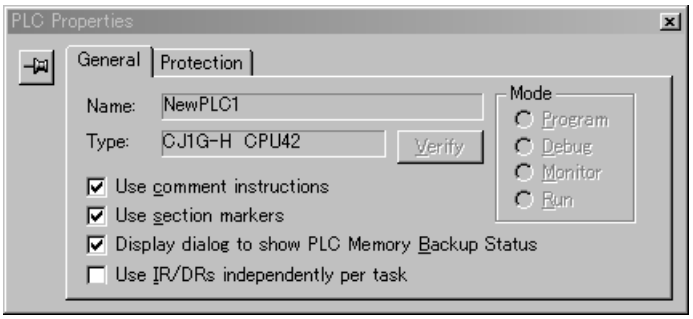
The content of Data Registers cannot be accessed (read or written) from a Programming Device.

Do not use Data Registers until a value has been set in the register. The register's operation will be unreliable if they are used without setting their values.

The values in Data Registers are unpredictable at the start of an interrupt task. When a Data Register will be used in an interrupt task, always set a value in the Data Register before using the register in that task.

Sharing Data Registers with CJ1-H CPU Units

The following setting can be made from the PC properties dialog box on the CX-Programmer to control sharing index and data registers between tasks.



9-18 Task Flags

Task Flags range from TK00 to TK31 and correspond to cyclic tasks 0 to 31. A Task Flag will be ON when the corresponding cyclic task is in executable (RUN) status and OFF when the cyclic task hasn't been executed (INI) or is in standby (WAIT) status.

Note These flags indicate the status of cyclic tasks only, they do not reflect the status of interrupt tasks.

Task Flag Initialization

The Task Flags will be cleared in the following cases, regardless of the status of the IOM Hold Bit.

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.
2. The PC's power supply is cycled.

Forcing Bit Status

The Task Flags **cannot** be force-set and force-reset.

9-19 Condition Flags

These flags include the Arithmetic Flags such as the Error Flag and Equals Flag which indicate the results of instruction execution. In earlier PCs, these flags were in the SR Area.

The Condition Flags are specified with labels, such as CY and ER, or with symbols, such as P_Carry and P_Instr_Error, rather than addresses. The status of these flags reflects the results of instruction execution, but the flags are read-only; they cannot be written directly from instructions or Programming Devices (CX-Programmer or Programming Console).

Note The CX-Programmer treats condition flags as global symbols beginning with P_.

All Condition Flags are cleared when the program switches tasks, so the status of the ER and AER flags are maintained only in the task in which the error occurred.

The Condition Flags **cannot** be force-set and force-reset.

Summary of the Condition Flags

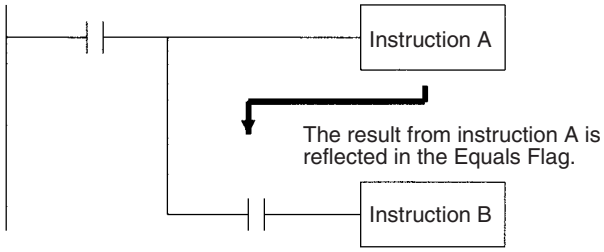
The following table summarizes the functions of the Condition Flags, although the functions of these flags will vary slightly from instruction to instruction. Refer to the description of the instruction for complete details on the operation of the Condition Flags for a particular instruction.

Name	Label	Symbol	Function
Error Flag	ER	P_ER	Turned ON when the operand data in an instruction is incorrect (an instruction processing error) to indicate that an instruction ended because of an error. When the PC Setup is set to stop operation for an instruction error (Instruction Error Operation), program execution will be stopped and the Instruction Processing Error Flag (A29508) will be turned ON when the Error Flag is turned ON.
Access Error Flag	AER	P_AER	Turned ON when an Illegal Access Error occurs. The Illegal Access Error indicates that an instruction attempted to access an area of memory that should not be accessed. When the PC Setup is set to stop operation for an instruction error (Instruction Error Operation), program execution will be stopped and the Instruction Processing Error Flag (A429510) will be turned ON when the Access Error Flag is turned ON.
Carry Flag	CY	P_CY	Turned ON when there is a carry in the result of an arithmetic operation or a “1” is shifted to the Carry Flag by a Data Shift instruction. The Carry Flag is part of the result of some Data Shift and Symbol Math instructions.
Greater Than Flag	>	P_GT	Turned ON when the first operand of a Comparison Instruction is greater than the second or a value exceeds a specified range.
Equals Flag	=	P_EQ	Turned ON when the two operands of a Comparison Instruction are equal the result of a calculation is 0.
Less Than Flag	<	P_LT	Turned ON when the first operand of a Comparison Instruction is less than the second or a value is below a specified range.
Negative Flag	N	P_N	Turned ON when the most significant bit (sign bit) of a result is ON.
Overflow Flag	OF	P_OF	Turned ON when the result of calculation overflows the capacity of the result word(s).
Underflow Flag	UF	P_UF	Turned ON when the result of calculation underflows the capacity of the result word(s).
Greater Than or Equals Flag	>=	P_GE	Turned ON when the first operand of a Comparison Instruction is greater than or equal to the second.
Not Equal Flag	< >	P_NE	Turned ON when the two operands of a Comparison Instruction are not equal.

Name	Label	Symbol	Function
Less Than or Equals Flag	< =	P_LE	Turned ON when the first operand of a Comparison Instruction is less than or equal to the second.
Always ON Flag	ON	P_On	Always ON. (Always 1.)
Always OFF Flag	OFF	P_Off	Always OFF. (Always 0.)

Using the Condition Flags

The Condition Flags are shared by all of the instructions, so their status may change often in a single cycle. Be sure to read the Condition Flags immediately after the execution of instruction, preferably in a branch from the same execution condition.



Instruction	Operand
LD	
Instruction A	
AND	=
Instruction B	

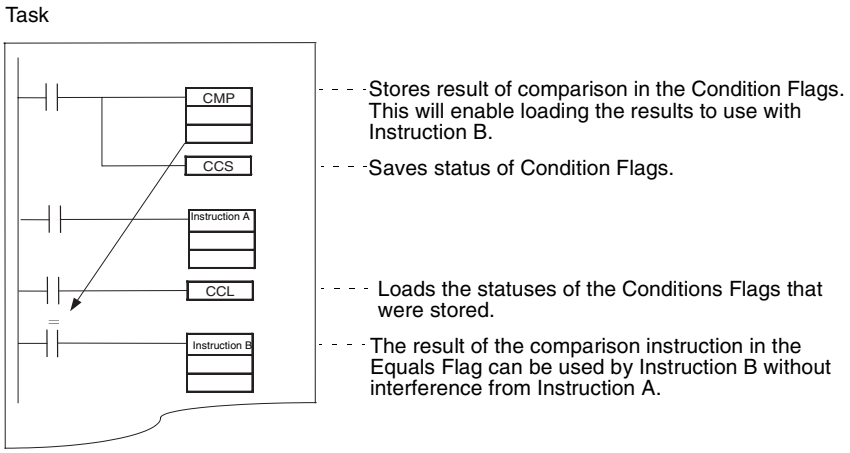
Since the Condition Flags are shared by all of the instructions, program operation can be changed from its expected course by interruption of a single task. Be sure to consider the effects of interrupts when writing the program. Refer to *SECTION 2 Programming* of *CS/CJ Series Programmable Controllers* (W394) for more details.

The Condition Flags are cleared when the program switches tasks, so the status of a Condition Flag cannot be passed to another task. For example the status of a flag in task 1 cannot be read in task 2.

Saving and Loading Condition Flag Status

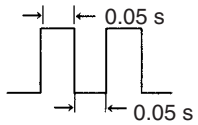
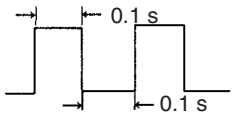
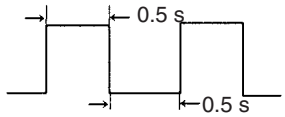
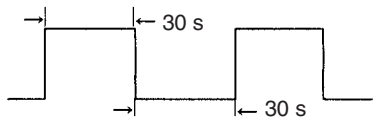
The CJ1-H CPU Units support instructions to save and load the Condition Flag status (CCS(282) and CCL(283)). These can be used to access the status of the Condition Flags at other locations in a task or in a different task.

The following example shows how the Equals Flag is used at a different location in the same task.



9-20 Clock Pulses

The Clock Pulses are flags that are turned ON and OFF at regular intervals by the system.

Name	Label	Symbol	Operation	
0.02 s Clock Pulse	0.02s	P_0_02_s		ON for 0.01 s OFF for 0.01 s
0.1 s Clock Pulse	0.1s	P_0_1s		ON for 0.05 s OFF for 0.05 s
0.2 s Clock Pulse	0.2s	P_0_2s		ON for 0.1 s OFF for 0.1 s
1 s Clock Pulse	1s	P_1s		ON for 0.5 s OFF for 0.5 s
1 min Clock Pulse	1min	P_1min		ON for 30 s OFF for 30 s

The Clock Pulses are specified with labels (or symbols) rather than addresses.

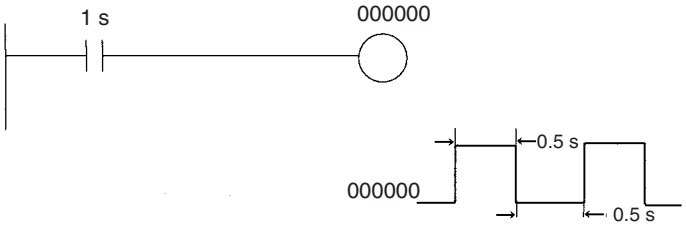
Note The CX-Programmer treats condition flags as global symbols beginning with P_.

The Clock Pulses are read-only; they cannot be overwritten from instructions or Programming Devices (CX-Programmer or Programming Console).

The Clock Pulses are cleared at the start of operation.

Using the Clock Pulses

The following example turns CIO 000000 ON and OFF at 0.5 s intervals.



Instruction	Operand
LD	1 s
OUT	000000

9-21 Parameter Areas

Unlike the data areas in I/O memory which can be used in instruction operands, the Parameter Area can be accessed only from a Programming Device. The Parameter Area is made up of the following parts.

- The PC Setup
- The Registered I/O Table
- The Routing Table
- The CPU Bus Unit Settings

9-21-1 PC Setup

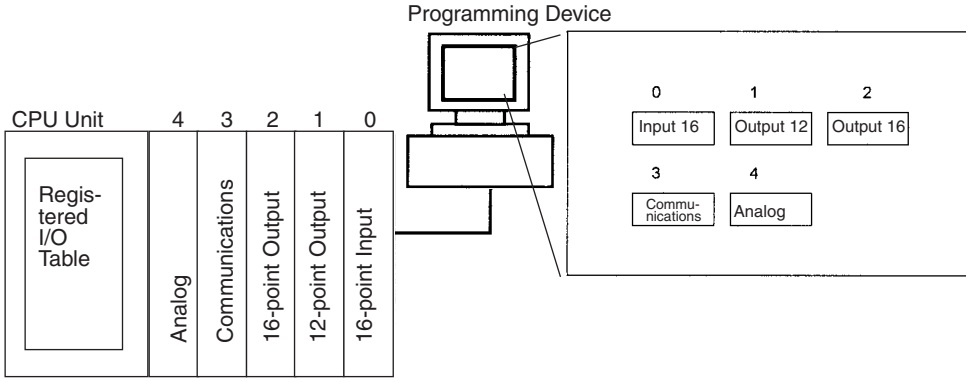
The user can customize the basic specifications of the CPU Unit with the settings in the PC Setup. The PC Setup contains settings such as the serial port communications settings and minimum cycle time setting.

Note Refer to the Programming Device's Operation Manual for details on changing these settings.

9-21-2 Registered I/O Tables

The Registered I/O Tables are tables in the CPU Unit that contain the information on the model and slot location of all of the Units mounted to the CPU Rack and Expansion Rack. The I/O Tables are written to the CPU Unit with a Programming Device operation.

The CPU Unit allocates I/O memory to I/O points on Basic I/O Unit and CPU Bus Units based on the information in the Registered I/O Tables. Refer to the Programming Device's Operation Manual for details on registering the I/O Tables.



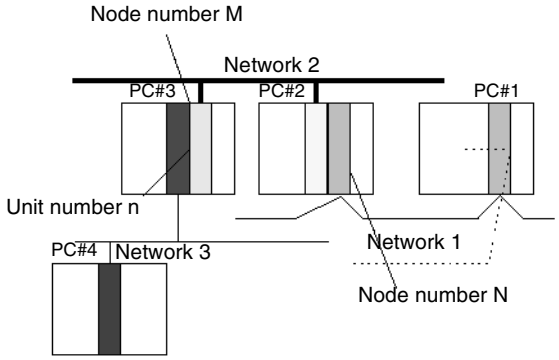
The I/O Setting Error Flag (A40110) will be turned ON if the models and locations of the Units actually mounted to the PC (CPU Rack and Expansion Racks) do not match the information in the Registered I/O Table.

By default, the CJ-series CPU Unit will automatically create I/O tables at startup and operate according to them. I/O tables do not necessarily need to be created by the user.

9-21-3 Routing Tables

When transferring data between networks, it is necessary to create a table in each CPU Unit that shows the communications route from the local PC's Communications Unit to the other networks. These tables of communications routes are called "Routing Tables."

Create the Routing Tables with a Programming Device or the Controller Link Support Software and transfer the tables to each CPU Unit. The following diagram shows the Routing Tables used for a data transfer from PC #1 to PC #4.



1,2,3... 1. Relay Network Table of PC #1:

Destination network	Relay network	Relay node
3	1	N

2. Relay Network Table of PC #2:

Destination network	Relay network	Relay node
3	2	M

3. Local Network Table of PC #3:

Local network	Unit number
3	n

Relay Network Table

This table lists the network address and node number of the first relay node to contact in order to reach the destination network. The destination network is reached through these relay nodes.

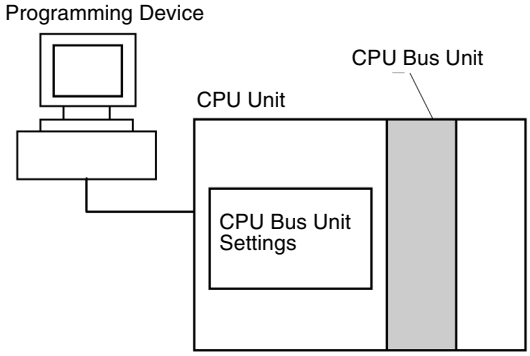
Local Network Table

This table lists the network address and unit number of the Communications Unit connected to the local PC.

These are settings for the CPU Bus Units which are controlled by the CPU Unit. The actual settings depend on the model of CPU Bus Unit being used; refer to the Unit's Operation Manual for details.

9-21-4 CPU Bus Unit Setting

These settings are not managed directly like the I/O memory's data areas, but are set from a Programming Device (CX-Programmer or Programming Console) like the Registered I/O Table. Refer to the Programming Device's operation manual for details on changing these settings.



SECTION 10
CPU Unit Operation and the Cycle Time

This section describes the internal operation of the CPU Unit and the cycle used to perform internal processing.

10-1 CPU Unit Operation

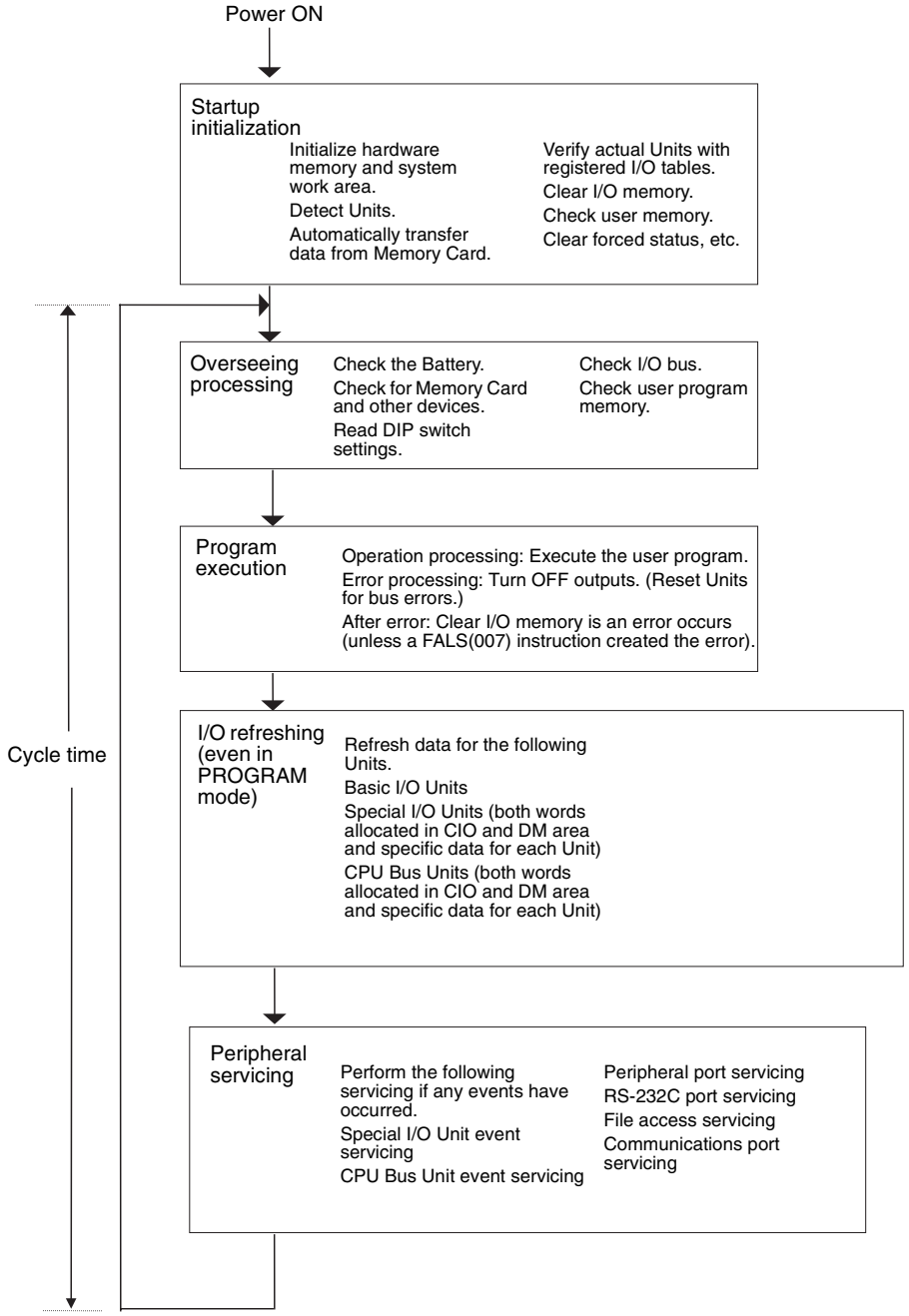
10-1-1 General Flow

The following flowchart shows the overall operation of the CPU Unit.

Note The CPU Unit's processing mode is set to Normal Mode, Parallel Processing with Synchronous Memory Access, or Parallel Processing with Asynchronous Memory Access in the PC Setup (Programming Console address 219, bits 08 to 15). This setting is also possible from the CX-Programmer.

Normal Mode

In the normal mode, the program is executed before I/O is refreshed and peripherals are serviced. This cycle is executed repeatedly.



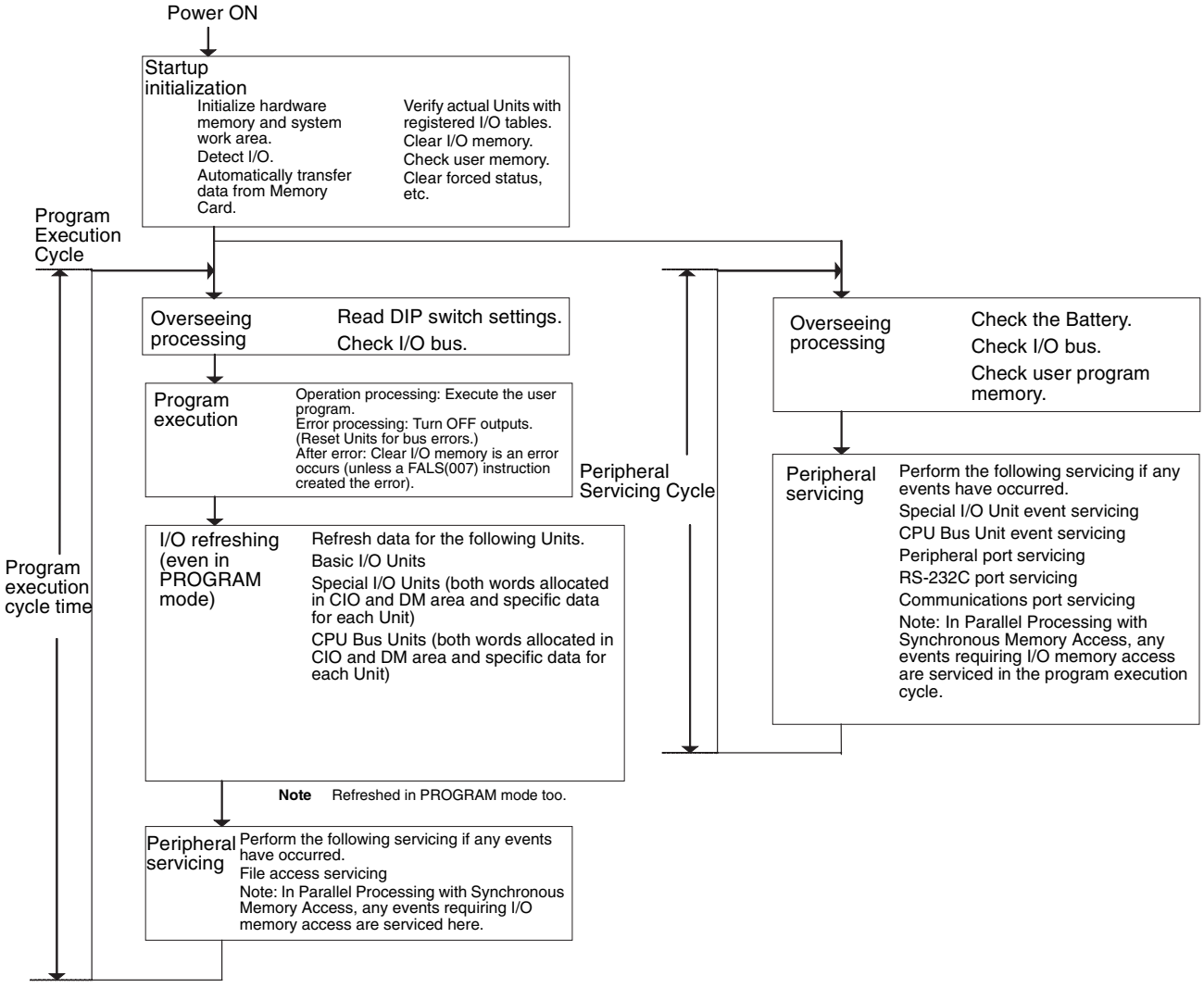
Parallel Processing (CJ1-H CPU Units Only)

The following two types of processing are performed in parallel in either of the Parallel Processing Modes.

1,2,3... 1. Program execution: Includes user program execution and I/O refreshing. It is this cycle time that is monitored from a Programming Device.

2. Peripheral servicing: Programming Devices and events from Special I/O Units and CPU Bus Units are serviced when they occur.

There are two different Parallel Processing Modes. Parallel Processing with Synchronous Memory Access refreshes I/O memory in the program execution cycle and Parallel Processing with Asynchronous Memory Access refreshes I/O memory in the peripheral servicing cycle.



Note Always disconnect the Programming Console from the peripheral port during actual system operation in a Parallel Processing Mode. If the Programming Console is left attached, excess time will be allocated to increase key response for the Programming Console, adversely affecting performance.

10-1-2 I/O Refreshing and Peripheral Servicing

I/O Refreshing

I/O refreshing involves cyclically transferring data with external devices using preset words in memory. I/O refreshing includes the following:

- Refreshing between Basic I/O Units and I/O words in the CIO Area
- Refreshing between Special I/O Units and CPU Bus Units, and the words allocated to these in the CIO Area (and for CPU Bus Units, words allocated in the DM Area)
- Refreshing Unit-specific data for Special I/O Units and CPU Bus Units.

All I/O refreshing is performed in the same cycle (i.e., time slicing is not used). I/O refreshing is always performed after program execution (even in a Parallel Processing Mode for CJ1-H CPU Units).

Units			Max. data exchange	Data exchange area
Basic I/O Units			Depends on the Unit.	I/O Bit Area
Special I/O Units	Words allocated in CIO Area		10 words/Unit (Depends on the Unit.)	Special I/O Unit Area
	Unit-specific data	DeviceNet Master Unit	Depends on the Unit.	Words set for remote I/O communications (for either fixed or user-set allocations)
		CompoBus/S Master Unit	Depends on the Unit.	Special I/O Units Area
CPU Bus Units	Words allocated in CIO Area		25 words/Unit	CJ-series CPU Bus Unit Area
	Words allocated in DM Area		100 words/Unit	CJ-series CPU Bus Unit Area
	Unit-specific data	Controller Link Unit and SYSMAC LINK Unit	Depends on the Unit.	Words set for data links (for either fixed or user-set allocations)
		DeviceNet Unit	Depends on the Unit.	Words set for remote I/O communications (for either fixed or user-set allocations)
		Serial Communications Unit	Depends on the protocol macros.	Communications data set for protocol macros
		Ethernet Unit	Depends on the Unit.	Communications data for socket services initiated by specific control bit operations.

Peripheral Servicing

Peripheral servicing involves servicing non-scheduled events for external devices. This includes both events from external devices and service requests to external devices.

Most peripheral servicing for CJ-series PCs involved FINS commands. The specific amount of time set in the system is allocated to each type of servicing

and executed every cycle. If all servicing cannot be completed within the allocated time, the remaining servicing is performed the next cycle.

Units	Servicing
Event servicing for Special I/O Units	Non-scheduled servicing for FINS commands from CJ-series Special I/O Units and CJ-series CPU Bus Units (e.g., requests to start external interrupt tasks)
Event servicing for CPU Bus Units	Non-scheduled servicing for FINS commands from the CPU Unit to the above Units.
Peripheral port servicing	Non-scheduled servicing for FINS or Host Link commands received via the peripheral or RS-232C ports from Programming Devices, PTs, or host computers (e.g., requests to transfer programming, monitoring, forced-set/reset operations, or online editing
RS-232C port servicing	Non-scheduled servicing from the CPU Unit transmitted from the peripheral or RS-232C port (non-solicited communications)
Communications port servicing	Servicing to execute network communications, serial communications, or file memory access for the SEND, RECV, CMND or PMCR instructions using communications ports 0 to 7 (internal logical ports) Servicing to execute background execution using communications ports 0 to 7 (internal logical ports) (CJ1-H CPU Unit only)
File access servicing	File read/write operations for Memory Cards or EM file memory.

Note

1. Special I/O Units, CPU Bus Units, RS-232C communications ports, and file servicing is allocated 4% of the cycle time by default (the default can be changed). If servicing is separated over many cycles, delaying completion of the servicing, set the same allocated time (same time for all services) rather than a percentage under execute time settings in the PC Setup.
2. In either of the Parallel Processing Modes for the CJ1-H CPU Unit, all peripheral servicing except for file access is performed in the peripheral servicing cycle.

10-1-3 Startup Initialization

The following initializing processes will be performed once each time the power is turned ON.

- Detect mounted Units.
- Compare the registered I/O tables and the actual Units.
- Clear the non-holding areas of I/O memory according to the status of the IOM Hold Bit. (See note 1.)
- Clear forced status according to the status of the Forced Status Hold Bit. (See note 2.)
- Autoboot using the autotransfer files in the Memory Card if one is inserted.
- Perform self-diagnosis (user memory check).
- Restore the user program. (See note 3.)

Note

1. The I/O memory is held or cleared according to the status of the IOM Host Bit and the setting for IOM Hold Bit Status at Startup in the PC Setup (read only when power is turned ON).

Auxiliary bit / **PC Setup setting**		**IOM Hold Bit (A50012)**	
		Clear (OFF)	**Hold (ON)**
IOM Hold Bit Status at Startup (Programming Console address: Word 80, bit 15)	**Clear (OFF)**	At power ON: Clear At mode change: Clear	At power ON: Clear At mode change: Hold
	Hold (ON)		At power ON: Hold At mode change: Hold

Mode Change: Between PROGRAMMING mode and RUN or MONITOR mode

2. The forced status held or cleared according to the status of the Force Status Hold Bit and the setting for Forced Status Hold Bit Status at Startup in the PC Setup.

Auxiliary bit / PC Setup setting		Forced Status Hold Bit (A50013)	
		Clear (OFF)	Hold (ON)
Forced Status Hold Bit Status at Startup (Programming Console address: Word 80, bit 14)	Clear (OFF)	At power ON: Clear At mode change: Clear	At power ON: Clear At mode change: Hold
	Hold (ON)		At power ON: Hold At mode change: Hold

Mode Change: Between PROGRAMMING mode and RUN or MONITOR mode

3. If the CPU Unit is turned OFF after online editing before the backup process has been competed, an attempt will be made to recover the program when power is turned ON again. The BKUP indicator will light during this process. Refer to the *CS/CJ Series Programming Manual* for details.

10-2 CPU Unit Operating Modes

10-2-1 Operating Modes

The CPU Unit has three operating modes that control the entire user program and are common to all tasks.

PROGRAM: Programs are not executed and preparations, such as creating I/O tables, initializing the PC Setup and other settings, transferring programs, checking programs, force-setting and force-resetting can be executed prior to program execution.

MONITOR: Programs are executed, but some operations, such as online editing, forced-set/reset, and changes to present values in I/O memory, are enabled for trial operation and other adjustments.

RUN: Programs are executed and some operations are disabled.

10-2-2 Status and Operations in Each Operating Mode

PROGRAM, RUN, and MONITOR are the three operating modes available in the CPU Unit. The following lists status and operations for each mode.

Overall Operation

Mode	Program (See note)	I/O refresh	External outputs	I/O Memory	
				Non-holding areas	Holding areas
PROGRAM	Stopped	Executed	OFF	Clear	Hold
RUN	Executed	Executed	Controlled by program	Controlled by program	
MONITOR	Executed	Executed	Controlled by program	Controlled by program	

Programming Console Operations

Mode	Monitor I/O Memory	Monitor Program	Transfer Program		Check Program	Create I/O Table
			PC to Programming Device	Programming Device to PC		
PROGRAM	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**
MONITOR	**OK**	**OK**	**OK**	X	X	X
RUN	**OK**	**OK**	**OK**	X	X	X

Mode	PC Setup	Modify Program	Force- set/ reset	Changing Timer/Counter SV	Changing Timer/Counter PV	Changing I/O Memory PV
PROGRAM	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**
RUN	X	X	X	X	X	X
MONITOR	X	**OK**	**OK**	**OK**	**OK**	**OK**

Note The following table shows the relationship of operating modes to tasks.

Mode	Cyclic task status	Interrupt task status
PROGRAM	Disabled status (INI)	Stopped
RUN MONITOR	• Any task that has not yet been executed, will be in disabled status (INI). • A task will go to READY status if the task is set to go to READY status at startup or the TASK ON (TKON) instruction has been executed for it. • A task in READY status will be executed (RUN status) when it obtains the right to execute. • A status will go to Standby status if a READY task is put into Standby status by a TASK OFF (TKOF) instruction.	Executed if interrupt condition is met.

Operating Mode Changes and I/O Memory

Mode Changes	Non-holding areas	Holding Areas
	• I/O bits • Data Link bits • CPU Bus Unit bits • Special I/O Unit bits • Work bits • Timer PV/Completion Flags • Index Registers • Data Registers • Task Flags (Auxiliary Area bits/words are holding or non-holding depending on the address.)	• HR Area • DM Area • EM Area • Counter PV and Completion Flags (Auxiliary Area bits/words are holding or non-holding depending on the address.)
RUN or MONITOR to PROGRAM	Cleared (See note 1.)	Held
PROGRAM to RUN or MONITOR	Cleared (See note 1.)	Held
RUN to MONITOR or MONITOR to RUN	Held (See note 2.)	Held

Note 1. The following processing is performed depending on the status of the I/O Memory Hold Bit. Output from Output Units will be turned OFF when operation stops even if I/O bit status is held in the CPU Unit.

2. The cycle time will increase by approximately 10 ms when the operating mode is changed from MONITOR to RUN mode. This will not, however, cause an error for exceeding the maximum cycle time limit.

I/O Memory Hold Bit status (A50012)	I/O Memory			Output bits allocated to Output Units		
	Mode changed between PROGRAM and RUN/ MONITOR	Operation stopped		Mode changed between PROGRAM and RUN/ MONITOR	Operation stopped	
		Fatal error other than FALS	FALS executed		Fatal error other than FALS	FALS executed
OFF	Cleared	Cleared	Held	OFF	OFF	OFF
ON	Held	Held	Held	Held	OFF	OFF

Note See *Chapter 7 Memory Areas*, etc. for more details on I/O Memory.

10-3 Power OFF Operation

The following processing is performed if CPU Unit power is turned OFF. Power OFF processing will be performed if the power supply falls below 85% of the minimum rated voltage while the CPU Unit is in RUN or MONITOR mode.

1,2,3... 1. The CPU Unit will stop.

2. Outputs from all Output Units will be turned OFF.

Note All output will turn OFF despite an I/O Memory Hold Bit or I/O Memory Hold Bit at power ON settings in the PC Setup.

85% of the rated voltage:
85 V AC for 100 to 240 V (wide range)

The following processing will be performed if power drops only momentarily (momentary power interruption).

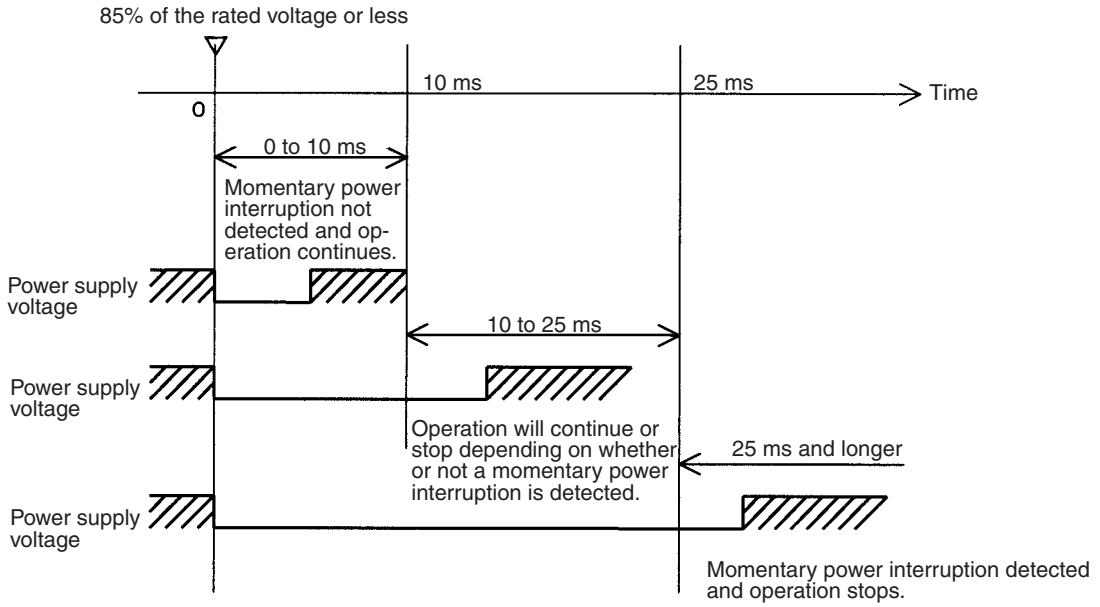
1,2,3... 1. The system will continue to run unconditionally if the momentary power interruption lasts less than 10 ms, i.e., the time it takes the minimum rated voltage at 85% or less to return to 85% or higher is less than 10 ms.

2. A momentary power interruption that lasts more than 10 ms but less than 25 ms is difficult to determine and a power interruption may or may not be detected.

3. The system will stop unconditionally if the momentary power interruption lasts more than 25 ms.

If operation stops under the conditions given in items 2 and 3 above, the timing used to stop operation (or the timing used to start execution of the Power OFF Interrupt Task) can be delayed by setting the Power OFF Detection Delay Time (0 to 10 ms) in the PC Setup. Operation, however, will always be

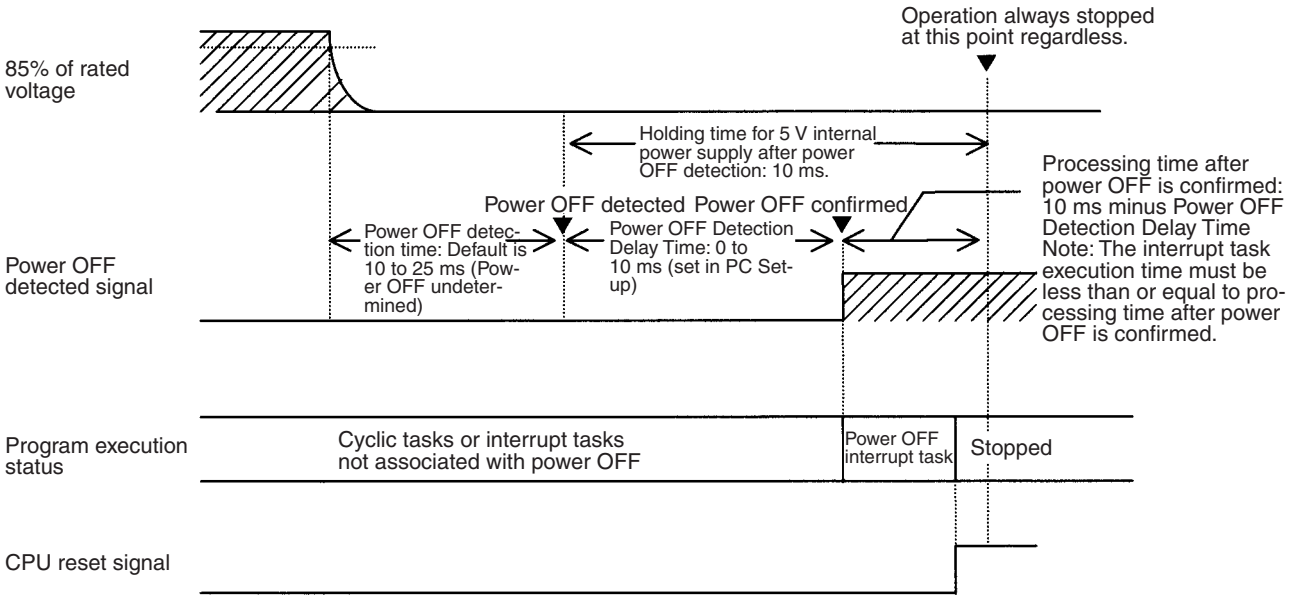
stopped 10 ms after detecting a momentary power interruption regardless of the setting in the PC Setup.



Note The above timing chart shows an example when the power OFF detection time is set to 0 ms.

The following timing chart shows the CPU Unit power OFF operation in more detail.

Power OFF Timing Chart



Power OFF Detection Time

The time it takes to detect power OFF after the power supply falls below 85% of the minimum rated voltage.

Power OFF Detection Delay Time

The delay time after power OFF is detected until it is confirmed. This can be set in the PC Setup within a range from 0 to 10 ms.

If the power OFF interrupt task is disabled, then the CPU reset signal will turn ON and the CPU will be reset when this time expires.

If the power OFF interrupt task is enabled in the PC Setup, then the CPU reset signal will turn ON and the CPU will be reset only after the power OFF interrupt task has been executed.

If an unstable power supply is causing power interruptions, set a longer Power OFF Detection Delay Time (10 ms max.) in the PC Setup.

Power Holding Time
The maximum amount of time (fixed at 10 ms) that 5 V will be held internally after power shuts OFF. The time that it takes for the power OFF interrupt task to execute must not exceed 10 ms minus the Power OFF Detection Delay Time (processing time after power OFF is confirmed). The power OFF interrupt task will be ended even if it has not been completely executed the moment this time expires.

Description of Operation

1,2,3...

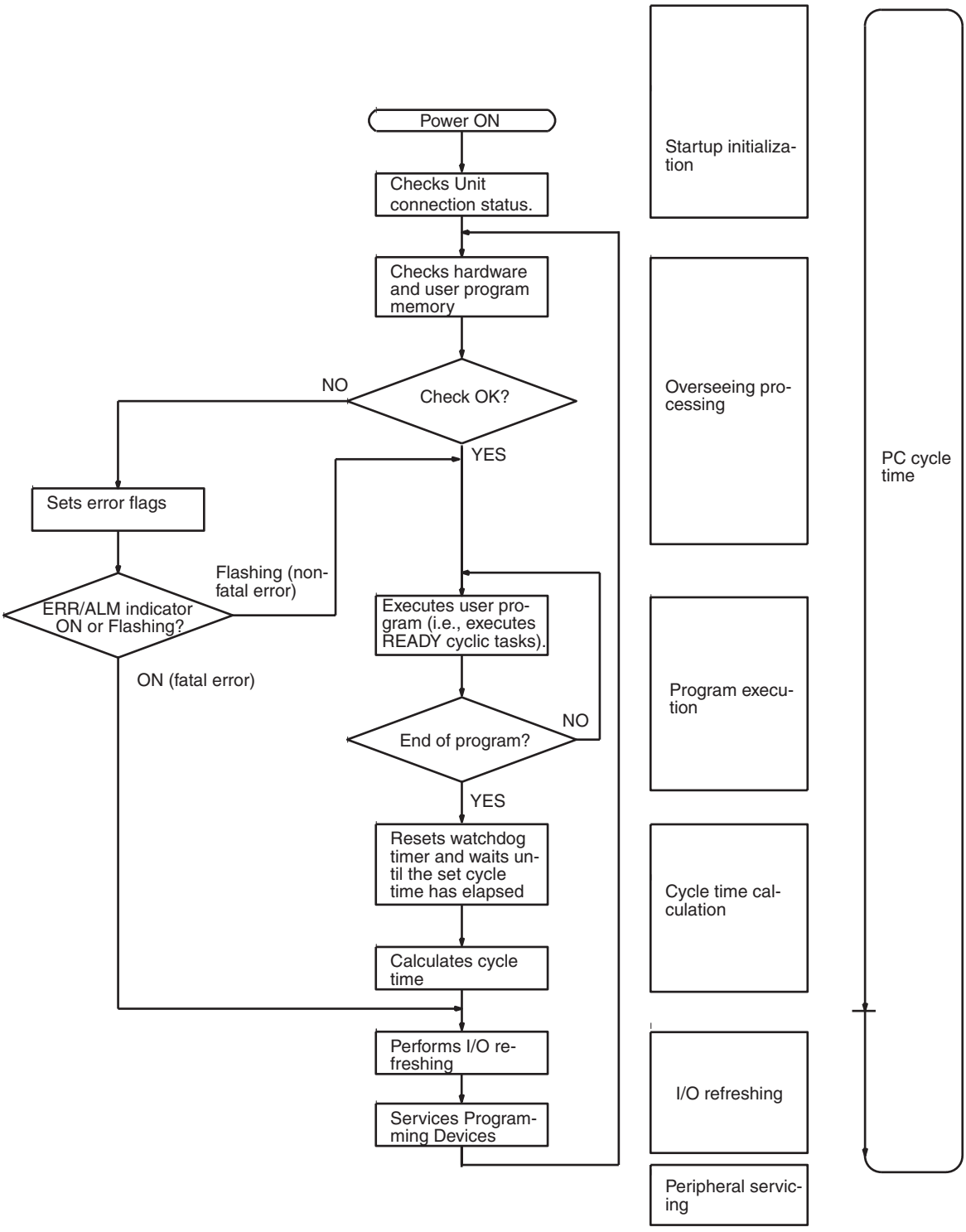
1. Power OFF will be detected if the 100 to 120 V AC, 200 to 240 V AC or 24-V DC power supply falls below 85% of the minimum rated voltage for the power OFF detection time (somewhere between 10 to 25 ms).
2. If the Power OFF Detection Delay Time is set (0 to 10 ms) in the PC Setup, then the following operations will be performed when the set time expires.
   a) If the power OFF interrupt task is disabled (default PC Setup setting) The CPU reset signal will turn ON and the CPU will be reset immediately.
   b) If the power OFF interrupt task is enabled (in the PC Setup), the CPU reset signal will turn ON and the CPU will be reset after the power OFF interrupt task has been executed. Make sure that the power OFF interrupt task will finish executing within 10 ms minus the Power OFF Detection Delay Time = processing time after power OFF. The 5-V internal power supply will be maintained only for 10 ms after power OFF is detected.

10-4 Computing the Cycle Time

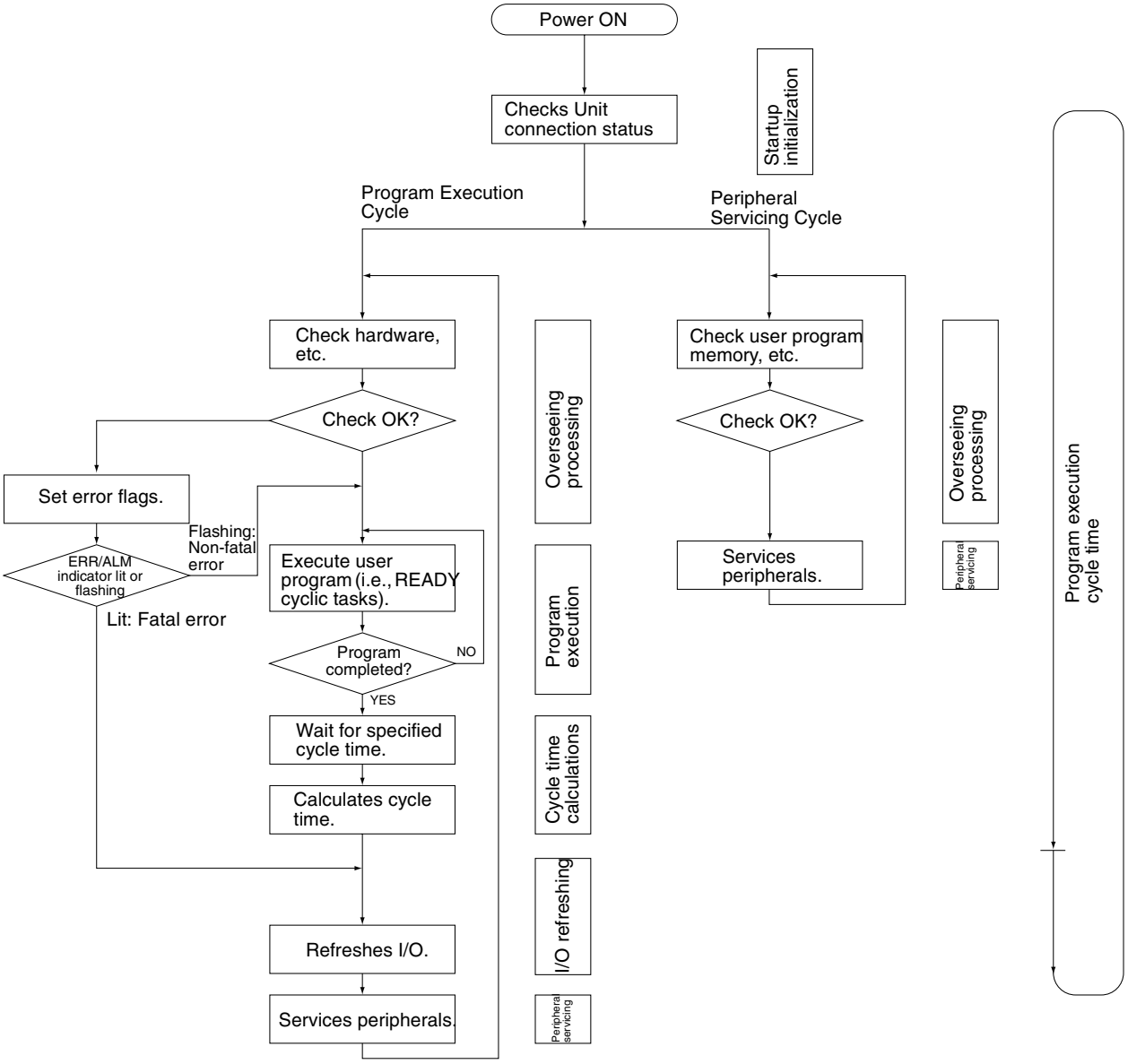
10-4-1 CPU Unit Operation Flowchart

The CJ-series CPU Units process data in repeating cycles from the overseeing processing up to peripheral servicing as shown in the following diagram.

Normal Processing Mode



Parallel Processing Mode



10-4-2 Cycle Time Overview

Normal Processing Mode

The cycle time depends on the following conditions.

- Type and number of instructions in the user program (in all cyclic tasks that are executed during a cycle, and within interrupt tasks for which the execution conditions have been satisfied).
- Type and number of Basic I/O Units
- Type and number of Special I/O Units, CPU Bus Units, and type of services being executed.
- Specific servicing for the following Units
  - Data link refreshing and the number of data link words for Controller Link and SYSMAC LINK Units

- Remote I/O for DeviceNet (Master) Units and the number of remote I/O words
- Use of protocol macros and the largest communications message
- Socket services for specific control bits for Ethernet Units and the number of send/receive words

- Fixed cycle time setting in the PC Setup
- File access in file memory, and the amount of data transferred to/from file memory
- Event servicing for Special I/O Units, CPU Bus Units, and communications ports
- Use of peripheral and RS-232C ports
- Fixed peripheral servicing time in the PC Setup

Note

1. The cycle time is not affected by the number of tasks that are used in the user program. The tasks that affect the cycle time are those cyclic tasks that are READY in the cycle.
2. When the mode is switched from MONITOR mode to RUN mode, the cycle time will be extended by 10 ms (this will not, however, take the cycle time over its limit).

The cycle time is the total time required for the PC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2) + (3) + (4) + (5)

1: Overseeing

Details	Processing time and fluctuation cause
Checks the I/O bus and user program memory, checks for battery errors and refreshes the clock.	CJ1-H CPU Unit: 0.3 ms CJ1 CPU Unit: 0.5 ms

2: Program Execution

Details	Processing time and fluctuation cause
Executes the user program, and calculates the total time time taken for the instructions to execute the program.	Total instruction execution time

3: Cycle Time Calculation

Details	Processing time and fluctuation cause
Waits for the specified cycle time to elapse when a minimum (fixed) cycle time has been set in the PC Setup. Calculates the cycle time.	When the cycle time is not fixed, the time for step 3 is approximately 0. When the cycle time is fixed, the time for step 3 is the preset fixed cycle time minus the actual cycle time ((1) + (2) + (4) + (5)).

4: I/O Refreshing

Details			Processing time and fluctuation cause
Basic I/O Units	Basic I/O Units are refreshed. Outputs from the CPU Unit to the I/O Unit are refreshed first for each Unit, and then inputs.		I/O refresh time for each Unit multiplied by the number of Units used.
Special I/O Units	Words allocated in CIO Area		I/O refresh time for each Unit multiplied by the number of Units used.
	Unit- specific data	CompoBus/S remote I/O	

Details			Processing time and fluctuation cause
CPU Bus Units	Words allocated in CIO and DM Areas		I/O refresh time for each Unit multiplied by the number of Units used.
	Unit- specific data	Data links for Controller Link and SYSMAC LINK Units, DeviceNet remote I/O for CJ-series DeviceNet Units, send/receive data for protocol macros, and socket services for specific control bits for Ethernet Units	I/O refresh time for each Unit multiplied by the number of Units used.

5: Peripheral Servicing

Details	Processing time and fluctuation cause
Services events for Special I/O Units. **Note** Peripheral servicing does not include I/O refreshing,	If a uniform peripheral servicing time hasn't been set in the PC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If no Units are mounted, the servicing time is 0 ms.
Services events for CPU Bus Units. **Note** Peripheral servicing does not include I/O refreshing.	Same as above.
Services events for peripheral ports.	If a uniform peripheral servicing time hasn't been set in the PC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If the ports are not connected, the servicing time is 0 ms.
Services RS-232C ports.	Same as above.
Services file access (Memory Card or EM file memory).	If a uniform peripheral servicing time hasn't been set in the PC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If there is no file access, the servicing time is 0 ms.
Services communications ports.	If a uniform peripheral servicing time hasn't been set in the PC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If no communications ports are used, the servicing time is 0 ms.

Parallel Processing with Asynchronous Memory Access

Program Execution Cycle

The program execution cycle time depends on the following conditions.

- Type and number of instructions in the user program (in all cyclic tasks that are executed during a cycle, and within interrupt tasks for which the execution conditions have been satisfied).
- Type and number of Basic I/O Units
- Type and number of Special I/O Units, CJ-series CPU Bus Units, and type of services being executed.

- Specific servicing for the following Units
  - Data link refreshing and the number of data link words for Controller Link and SYSMAC LINK Units
  - Remote I/O for DeviceNet (Master) Units and the number of remote I/O words
  - Use of protocol macros and the largest communications message
  - Socket services for specific control bits for Ethernet Units and the number of send/receive words
- Fixed cycle time setting in the PC Setup
- File access in file memory, and the amount of data transferred to/from file memory
- Fixed peripheral servicing time in the PC Setup

The program execution cycle time is the total time required for the PC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2) + (3) + (4) + (5)

Details			Processing time and fluctuation cause
(1)	Overseeing	I/O bus check, etc.	0.3 ms
(2)	Program execution	Same as for Normal Mode.	Same as for Normal Mode.
(3)	Cycle time calculation	Waits for the specified cycle time.	Same as for Normal Mode.
(4)	I/O refreshing	Same as for Normal Processing Mode.	Same as for Normal Processing Mode.
(5)	Partial peripheral servicing	Servicing file access	Same as for Normal Processing Mode.

Peripheral Servicing Cycle Time

The peripheral servicing execution cycle time depends on the following conditions.

- Type and number of Special I/O Units, CJ-series CPU Bus Units, and type of services being executed.
- Type and frequency of event servicing requiring communications ports.
- Use of peripheral and RS-232C ports

The peripheral servicing cycle time is the total time required for the PC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2)

Name		Processing		Processing time and fluctuation cause
(1)	Overseeing processing	Checks user program memory, checks for battery errors, etc.		0.2 ms
(2)	Peripheral servicing	Performs services for the events give at the right, including I/O memory access.	Events with CJ-series Special I/O Units (does not include I/O refreshing)	1.0 ms for each type of service If servicing ends before 1 ms has expired, the next type of servicing will be started immediately without waiting.
			Events with CJ-series CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events using communications ports	

Note

1. The cycle time display on a Programming Device is the Program Execution Cycle Time.
2. The peripheral service cycle time varies with the event load and number of Units that are mounted. In a Parallel Processing Mode, however, this variation will not affect the program execution cycle time.

Parallel Processing with Synchronous Memory Access

Program Execution Cycle

The program execution cycle time depends on the same conditions as Parallel Processing with Synchronous Memory Access.

The program execution cycle time is the total time required for the PC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2) + (3) + (4) + (5)

Details				Processing time and fluctuation cause
(1)	Overseeing	I/O bus check, etc.		0.3 ms
(2)	Program execution	Same as for Normal Mode.		Same as for Normal Mode.
(3)	Cycle time calculation	Waits for the specified cycle time.		Same as for Normal Mode.
(4)	I/O refreshing	Same as for Normal Processing Mode.		Same as for Normal Mode.
.(5)	Partial peripheral servicing	Servicing file access (Memory Card or EM file memory)		Same as for Normal Mode.
		Performs services for the events give at the right that requires I/O memory access	Events with Special I/O Units (does not include I/O refreshing)	
			Events with CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events using communications ports	

Peripheral Servicing Cycle Time

The peripheral servicing execution cycle time depends on the same conditions as Parallel Processing with Synchronous Memory Access.

The peripheral servicing cycle time is the total time required for the PC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2)

Name		Processing		Processing time and fluctuation cause
(1)	Overseeing processing	Checks user program memory, checks for battery errors, etc.		0.2 ms
(2)	Peripheral servicing	Performs services for the events give at the right, excluding those that require I/O memory access.	Events with Special I/O Units (does not include I/O refreshing)	1.0 ms for each type of service If servicing ends before 1 ms has expired, the next type of servicing will be started immediately without waiting.
			Events with CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events using communications ports	

Note

1. The cycle time display on a Programming Device is the Program Execution Cycle Time.
2. The peripheral service cycle time varies with the event load and number of Units that are mounted. In a Parallel Processing Mode, however, this variation will not affect the program execution cycle time.

10-4-3 I/O Unit Refresh Times for Individual Units

Typical Basic I/O Unit Refresh Times

Name	Model	I/O refresh time per Unit
16-point DC Input Units	CJ1W-ID211	0.004 ms
32-point DC Input Units	CJ1W-ID231/232	0.006 ms
64-point DC Input Units	CJ1W-ID261/262	0.012 ms
8/16-point DC Input Units	CJ1W-IA201/111	0.004 ms
16-point Interrupt Input Units	CJ1W-INT01	0.004 ms
8/16-point Transistor Output Units	CJ1W-OD201/202/ 211/212	0.005 ms
32-point Transistor Output Units	CJ1W-OD231/232/ 233	0.008 ms
64-point Transistor Output Units	CJ1W-OD261/263	0.015 ms
8/16-point Relay Output Units	CJ1W-OC201/211	0.005 ms
8-point Triac Output Units	CJ1W-OA201	0.005 ms

Typical Special I/O Unit Refresh Times

Name	Model		I/O refresh time per Unit	
			CJ1	CJ1-H
Analog Input Units	CJ1W-AD041/081(-V1)		0.2 ms	0.12 ms
Analog Output Units	CJ1W-DA021/041		0.2 ms	0.12 ms
Temperature Control UnitS	CJ1W-TC□□□		0.4 ms	0.3 ms
Position Control Units	CJ1W-NC113/133		0.29 ms (+ 0.7 ms for each instruction (IOWR/ IORD) used to transfer data)	
	CJ1W-NC213/233		0.32 ms (+ 0.7 ms for each instruction (IOWR/ IORD) used to transfer data)	
	CJ1W-NC413/433		0.41 ms (+ 0.6 ms for each instruction (IOWR/ IORD) used to transfer data)	
High-speed Counter Unit	CJ1W-CT021		0.2 ms	0.14 ms
CompoBus/S Master Unit	CJ1W-SRM21	Assigned 1 unit number	0.15 ms	0.12 ms
		Assigned 2 unit numbers	0.17 ms	0.13 ms

Increase in Cycle Time Caused by CPU Bus Units

The increase in the cycle time will be the I/O refresh times from the following table plus the refresh time required for specific Unit functions.

Name	Model	Increase	Remarks
Controller Link Unit	CJ1W-CLK/21	CJ1: 0.2 ms CJ1-H: 0.1 ms	There will be an increase of 1.5 ms + 1 μs x number of data link words for CJ1 CPU Units and of 0.1 ms + 0.7 μs x number of data link words for CJ1 CPU Units. (See note 2.) There will be an additional increase of the event execution times when message services are used.
Serial Communications Unit	CJ1W-SCU41	CJ1: 0.25 ms CJ1-H: 0.22 ms	There will be an increase of up to the following time when a protocol macro is executed: CJ1 CPU Units: 1 μs x maximum number of data words sent or received (0 to 500 words) CJ1 CPU Units: 0.7 μs x maximum number of data words sent or received (0 to 500 words) There will be an increase of the event execution times when Host Links or 1:N NT Links are used.
Ethernet Unit	CJ1W-ETN11	CJ1: 0.25 ms CJ1-H: 0.1 ms	If socket services are executed with software switches, there will be an increase of 2 μs x the number of bytes sent/received for CJ1 CPU Units and of 1.4 μs x the number of bytes sent/received for CJ1-H CPU Units. (See note 2.) There will be an increase of the event execution times when FINS communications services, socket services for CMND instructions, or FTP services are performed.
DeviceNet Unit	CJ1W-DRM21	CJ1: 0.7 ms + 1 μs for each allocated word CJ1-H: 0.4 ms + 0.7 μs for each allocated word	Include all words allocated to the slaves, including unused ones. For message communications, add the number of communications words to the calculations as the left.

Note The times given show the performance of the CPU6□H.

10-4-4 Cycle Time Calculation Example

The following example shows the method used to calculate the cycle time when Basic I/O Units only are connected in the PC. Here, a CJ1G-CPU4□H CPU Unit is used.

Conditions

Item	Details	
CPU Rack	CJ1W-ID211 16-point Input Units	4 Units
	CJ1W-OD211 16-point Output Units	4 Units
Expansion Rack	CJ1W-ID211 16-point Input Units	4 Units
	CJ1W-OD211 16-point Output Units	4 Units
User program	5 K steps	LD instruction 2.5 K steps, OUT instruction 2.5 K steps
Peripheral port connection	Yes and no	
Fixed cycle time processing	No	
RS-232C port connection	No	
Peripheral servicing with other devices (Special I/O Units, CPU Bus Units, and file access)	No	

Calculation Example

Process name	Calculation	Processing time	
		With Programming Device	Without Programming Device
(1) Overseeing	---	0.3 ms	0.3 ms
(2) Program execution	0.04 μs × 2,500 + 0.04 μs × 2,500	0.2 ms	0.2 ms
(3) Cycle time calculation	(Fixed cycle time not set)	0 ms	0 ms
(4) I/O refreshing	0.004 ms × 8 + 0.005 ms × 8	0.072 ms	0.072 ms
(5) Peripheral servicing	(Peripheral port connected only)	0.1 ms	0 ms
Cycle time	(1) + (2) + (3) + (4) + (5)	0.672 ms	0.572 ms

10-4-5 Online Editing Cycle Time Extension

When online editing is executed from a Programming Device (such as Programming Console or CX-Programmer) while the CPU Unit is operating in MONITOR mode to change the program, the CPU Unit will momentarily suspend operation while the program is being changed. The period of time that the cycle time is extended is determined by the following conditions.

- Editing operations (insert/delete/overwrite).
- Types of instructions used.

The cycle time extension for online editing will be negligibly affected by the size of task programs.

If the maximum program size for each task is 64 Ksteps, the online editing cycle time extension will be as shown in the following table. (See note.)

CPU Unit	Increase in cycle time for online editing
CJ1 CPU-V	Maximum: 80 ms, Normal: 12 ms
CPU4□H CJ1-H CPU4□	Maximum: 75 ms, Normal: 11 ms
CPU6□H CJ1-H CPU6□	Maximum: 55 ms, Normal: 8 ms

When editing online, the cycle time will be extended by the time that operation is stopped.

Note The above cycle time extensions assume that a lot of instructions requiring time are being used in the program. The cycle time extension normally be 12 ms max.

When editing online, the cycle time will be extended by the time that operation is stopped.

Note
1. The above cycle time extensions assume that a lot of instructions requiring time are being used in the program. The cycle time extension would be 12 ms max.
2. When there is one task, online editing is processed all in the cycle time following the cycle in which online editing is executed (written). When there are multiple tasks (cyclic tasks and interrupt tasks), online editing is separated, so that for n tasks, processing is executed over n to n ×2 cycles max.

10-4-6 I/O Response Time

The I/O response time is the time it takes from when an Input Unit's input turns ON, the data is recognized by the CJ-series CPU Unit, and the user program is executed, up to the time for the result to be output to an Output Unit's output terminals.

The length of the I/O response time depends on the following conditions.

- Timing of Input Bit turning ON.
- Cycle time.
- Type of Rack to which Input and Output Units are mounted (CPU Rack, CPU Expansion Rack, Expansion Rack).

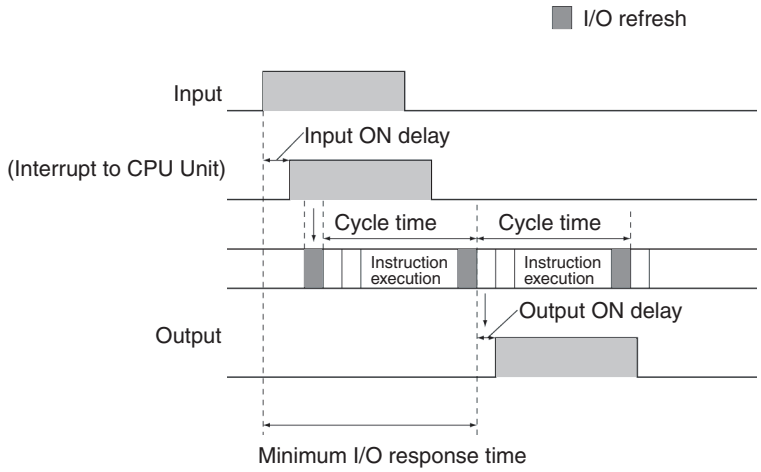
Basic I/O Units

Minimum I/O Response Time

The I/O response time is shortest when data is retrieved immediately before I/O refresh of the CPU Unit.

The minimum I/O response time is the total of the Input ON delay, the cycle time, and the Output ON delay.

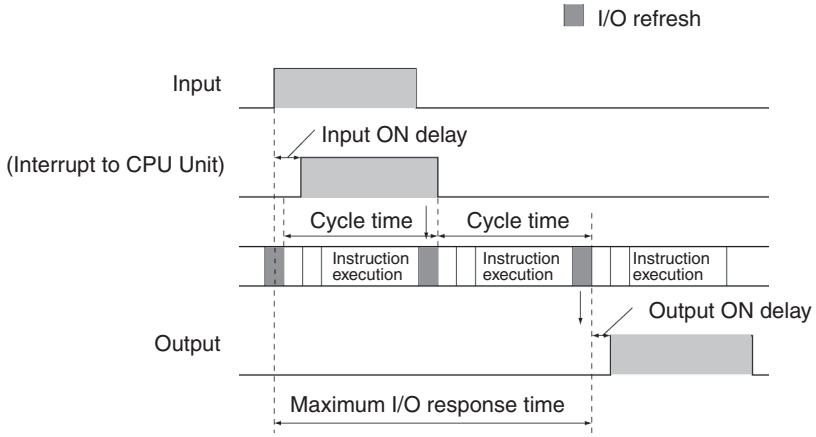
Note The Input and Output ON delay differs according to the Unit used.



Maximum I/O Response Time

The I/O response time is longest when data is retrieved immediately after I/O refresh of the Input Unit.

The maximum I/O response time is the total of the Input ON delay, (the cycle time × 2), and the Output ON delay.



Calculation Example

Conditions:	Input ON delay	1.5 ms
	Output ON delay	0.2 ms
	Cycle time	20.0 ms

Minimum I/O response time = 1.5 ms + 20 ms + 0.2 ms = 21.7 ms

Maximum I/O response time = 1.5 ms + (20 ms ×2) + 0.2 ms = 41.7 ms

10-4-7 Interrupt Response Times

I/O Interrupt Tasks

The interrupt response time for I/O interrupt tasks is the time taken from when an input from a CJ1W-INT01 Interrupt Input Unit has turned ON (or OFF) until the I/O interrupt task has actually been executed.

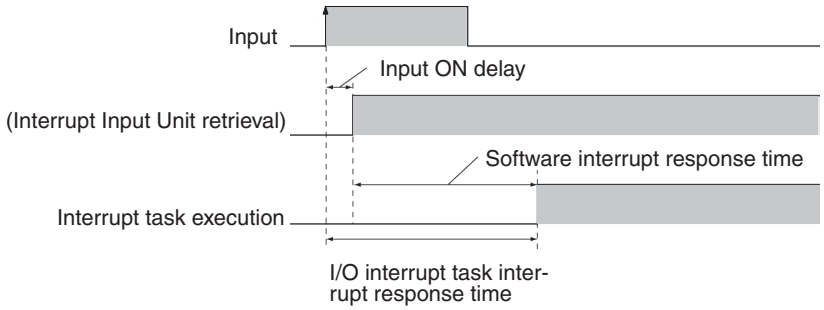
The length of the interrupt response time for I/O interrupt tasks depends on the following conditions.

Item	CPU Unit	Time
Hardware response	CJ1 CPU Unit	Upward differentiation: 0.05 ms, Downward differentiation: 0.5 ms
	CJ1-H CPU Units	

Item	CPU Unit	Time
Software interrupt response	CJ1 CPU Unit	320 μs
	CJ1-H CPU Units	124 μs

Note I/O interrupt tasks can be executed (while an instruction is being executed, or by stopping the execution of an instruction) during execution of the user program, I/O refresh, peripheral servicing, or overseeing. The interrupt response time is not affected by the Input of the Interrupt Input Unit turning ON during any of the above processing operations.

Some I/O interrupts, however, are not executed during interrupt tasks even if the I/O interrupt conditions are satisfied. Instead, the I/O interrupts are executed in order of priority after the other interrupt task has completed execution and the software interrupt response time (1 ms max.) has elapsed.



Scheduled Interrupt Tasks

The interrupt response time of scheduled interrupt tasks is the time taken from after the scheduled time specified by the MSKS(690) instruction has elapsed until the interrupt task has actually been executed.

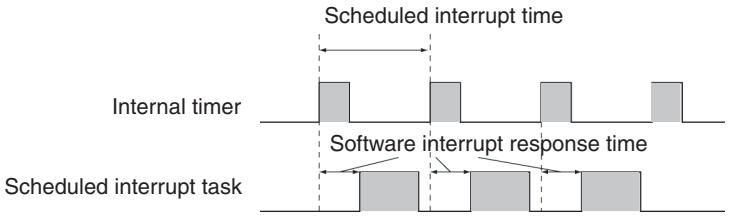
The length of the interrupt response time for scheduled interrupt tasks depends on the following conditions.

- The software interrupt response time is 1 ms max.

Note Scheduled interrupt tasks can be executed (while an instruction is being executed, or by stopping the execution of an instruction) during execution of the user program, I/O refresh, peripheral servicing, or overseeing. The interrupt response time is not affected by the scheduled time elapsing during any of the above processing operations.

Some scheduled interrupts, however, are not executed during other interrupt tasks even if the scheduled interrupt conditions are satisfied. Instead, the scheduled interrupt is executed after the other interrupt task has completed execution and the software interrupt response time (1 ms max.) has elapsed.

The interrupt response time for scheduled interrupt tasks is the software interrupt response time (1 ms max.).



External Interrupt Tasks

The interrupt response time for external interrupt tasks differs depending on the Unit (Special I/O Unit or CJ-series CPU Bus Unit) that is requesting the external interrupt task of the CPU Unit and the type of service requested by

the interrupt. For details, refer to the appropriate operation manual for the Unit being used.

Power OFF Interrupt Tasks Power OFF interrupt tasks are executed within 0.1 ms of the power being confirmed as OFF.

10-5 Instruction Execution Times and Number of Steps

The following table lists the execution times for all instructions that are available for CJ PCs.

The total execution time of instructions within one whole user program is the process time for program execution when calculating the cycle time (See note.).

Note User programs are allocated tasks that can be executed within cyclic tasks and interrupt tasks that satisfy interrupt conditions.

Execution times for most instructions differ depending on the CPU Unit used (CJ1H-CPU6□H, CJ1H-CPU4□H, andCJ1G-CPU4□) and the conditions when the instruction is executed. The top line for each instruction in the following table shows the minimum time required to process the instruction and the necessary execution conditions, and the bottom line shows the maximum time and execution conditions required to process the instruction.

The execution time can also vary when the execution condition is OFF.

The following table also lists the length of each instruction in the *Length (steps)* column. The number of steps required in the user program area for each of the CJ-series instructions varies from 1 to 7 steps, depending upon the instruction and the operands used with it. The number of steps in a program is not the same as the number of instructions.

Note

1. Program capacity for CJ-series PCs is measured in steps, whereas program capacity for previous OMRON PCs, such as the C-series and CV-series PCs, was measured in words. Basically speaking, 1 step is equivalent to 1 word. The amount of memory required for each instruction, however, is different for some of the CJ-series instructions, and inaccuracies will occur if the capacity of a user program for another PC is converted for a CJ-series PC based on the assumption that 1 word is 1 step. Refer to the information at the end of *10-5 Instruction Execution Times and Number of Steps* for guidelines on converting program capacities from previous OMRON PCs.
2. Most instructions are supported in differentiated form (indicated with ↑, ↓, @, and %). Specifying differentiation will increase the execution times by the following amounts.

Symbol	CJ1-H CPU Units		CJ1 CPU Units
	CPU6□H	CPU4□H	CPU4□
↑ or ↓	+0.24 μs	+0.32 μs	+0.45 μs
@ or %	+0.24 μs	+0.32 μs	+0.33 μs

3. Use the following times as guidelines when instructions are not executed.

CJ1-H CPU Units		CJ1 CPU Units
CPU6□H	CPU4□H	CPU4□
Approx. 0.1 μs	Approx. 0.2 μs	Approx. 0.2 to 0.4 μs

10-5-1 Sequence Input Instructions

Instruction	Mnemonic	Code	Length (steps)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
LOAD	LD	---	1	0.02	0.04	0.08	---
	!LD	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
LOAD NOT	LD NOT	---	1	0.02	0.04	008	---
	!LD NOT	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
AND	AND	---	1	0.02	0.04	0.08	---
	!AND	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
AND NOT	AND NOT	---	1	0.02	0.04	0.08	---
	!AND NOT	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
OR	OR	---	1	0.02	0.04	0.08	---
	!OR	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
OR NOT	OR NOT	---	1	0.02	0.04	0.08	---
	!OR NOT	---	2	+21.14	+21.16	+21.16	Increase for immediate refresh
AND LOAD	AND LD	---	1	0.02	0.04	0.08	---
OR LOAD	OR LD	---	1	0.02	0.04	0.08	---
NOT	NOT	520	1	0.02	0.04	0.08	---
CONDITION ON	UP	521	3	0.3	0.42	0.54	---
CONDITION OFF	DOWN	522	4	0.3	0.42	0.54	---
LOAD BIT TEST	LD TST	350	4	0.14	0.24	0.37	---
LOAD BIT TEST NOT	LD TSTN	351	4	0.14	0.24	0.37	---
AND BIT TEST NOT	AND TSTN	351	4	0.14	0.24	0.37	---
OR BIT TEST	OR TST	350	4	0.14	0.24	0.37	---
OR BIT TEST NOT	OR TSTN	351	4	0.14	0.24	0.37	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table

10-5-2 Sequence Output Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
OUTPUT	OUT	---	1	0.02	0.04	0.21	---
	!OUT	---	2	+21.37	+21.37	+21.37	Increase for immediate refresh
OUTPUT NOT	OUT NOT	---	1	0.02	0.04	0.21	---
	!OUT NOT	---	2	+21.37	+21.37	+21.37	Increase for immediate refresh
KEEP	KEEP	11	1	0.06	0.08	0.29	---
DIFFERENTIATE UP	DIFU	13	2	0.24	0.40	0.54	---
DIFFERENTIATE DOWN	DIFD	14	2	0.24	0.40	0.54	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SET	SET	---	1	0.02	0.06	0.21	---
	!SET	---	2	+21.37	+21.37	+21.37	Increase for immediate refresh
RESET	RSET	---	1	0.02	0.06	0.21	Word specified
	!RSET	---	2	+21.37	+21.37	+21.37	Increase for immediate refresh
MULTIPLE BIT SET	SETA	530	4	5.8	6.1	7.8	With 1-bit set
				25.7	27.2	38.8	With 1,000-bit set
MULTIPLE BIT RESET	RSTA	531	4	5.7	6.1	7.8	With 1-bit reset
				25.8	27.1	38.8	With 1,000-bit reset
SINGLE BIT SET	SETB	532	2	0.24	0.34	---	---
	!SETB		3	+21.44	+21.54	---	---
SINGLE BIT RESET	RSTB	533	2	0.24	0.34	---	---
	!RSTB		3	+21.44	+21.54	---	---
SINGLE BIT OUTPUT	OUTB	534	2	0.22	0.32	---	---
	!OUTB		3	+21.42	+21.52	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-3 Sequence Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
END	END	1	1	5.5	6.0	4.0	---
NO OPERATION	NOP	0	1	0.02	0.04	0.12	---
INTERLOCK	IL	2	1	0.06	0.06	0.12	---
INTERLOCK CLEAR	ILC	3	1	0.06	0.06	0.12	---
JUMP	JMP	4	2	0.38	0.48	8.1	---
JUMP END	JME	5	2	---	---	---	---
CONDITIONAL JUMP	CJP	510	2	0.38	0.48	7.4	When JMP condition is satisfied
CONDITIONAL JUMP NOT	CJPN	511	2	0.38	0.48	8.5	When JMP condition is satisfied
MULTIPLE JUMP	JMP0	515	1	0.06	0.06	0.12	---
MULTIPLE JUMP END	JME0	516	1	0.06	0.06	0.12	---
FOR LOOP	FOR	512	2	0.52	0.54	0.21	Designating a constant
BREAK LOOP	BREAK	514	1	0.06	0.06	0.12	---
NEXT LOOP	NEXT	513	1	0.18	0.16	0.17	When loop is continued
				0.22	0.48	0.12	When loop is ended

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-4 Timer and Counter Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
TIMER	TIM	---	3	0.56	0.88	0.42	---
COUNTER	CNT	---	3	0.56	0.88	0.42	---
HIGH-SPEED TIMER	TIMH	15	3	0.88	1.14	0.42	---
ONE-MS TIMER	TMHH	540	3	0.86	1.12	0.42	---
ACCUMULATIVE TIMER	TTIM	87	3	16.1	17.0	21.4	---
				10.9	11.4	14.8	When resetting
				8.5	8.7	10.7	When interlocking
LONG TIMER	TIML	542	4	7.6	10.0	12.8	---
				6.2	6.5	7.8	When interlocking
MULTI-OUTPUT TIMER	MTIM	543	4	20.9	23.3	26.0	---
				5.6	5.8	7.8	When resetting
REVERSIBLE COUNTER	CNTR	12	3	16.9	19.0	20.9	---
RESET TIMER/ COUNTER	CNR	545	3	9.9	10.6	13.9	When resetting 1 word
				4.16 ms	4.16 ms	5.42 ms	When resetting 1,000 words

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-5 Comparison Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
Input Comparison Instructions (unsigned)	LD, AND, OR +=	300	4	0.10	0.16	0.37	---
	LD, AND, OR + <>	305					
	LD, AND, OR + <	310					
	LD, AND, OR +<=	315					
	LD, AND, OR +>	320					
	LD, AND, OR +>=	325					
Input Comparison Instructions (double, unsigned)	LD, AND, OR +=+L	301	4	0.10	0.16	0.54	---
	LD, AND, OR +<>+L	306					
	LD, AND, OR +<+L	311					
	LD, AND, OR +<=+L	316					
	LD, AND, OR +>+L	321					
	LD, AND, OR +>=+L	326					

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
Input Comparison Instructions (signed)	LD, AND, OR +=+S	302	4	0.10	0.16	6.50	---
	LD, AND, OR +<>+S	307					
	LD, AND, OR +<+S	312					
	LD, AND, OR +<=	317					
	LD, AND, OR +>+S	322					
	LD, AND, OR +>=+S	327					
Input Comparison Instructions (double, signed)	LD, AND, OR +=+SL	303	4	0.10	0.16	6.50	---
	LD, AND, OR +<>+SL	308					
	LD, AND, OR +<+SL	313					
	LD, AND, OR +<=+SL	318					
	LD, AND, OR +>+SL	323					
	LD, AND, OR +>=+SL	328					
COMPARE	CMP	20	3	0.04	0.04	0.29	---
	!CMP	20	7	42.1	42.1	42.4	Increase for immediate refresh
DOUBLE COMPARE	CMPL	60	3	0.08	0.08	0.46	---
SIGNED BINARY COMPARE	CPS	114	3	0.08	0.08	6.50	---
	!CPS	114	7	35.9	35.9	42.4	Increase for immediate refresh
DOUBLE SIGNED BINARY COMPARE	CPSL	115	3	0.08	0.08	6.50	---
TABLE COMPARE	TCMP	85	4	14.0	15.2	21.9	---
MULTIPLE COMPARE	MCMP	19	4	20.5	22.8	31.2	---
UNSIGNED BLOCK COMPARE	BCMP	68	4	21.5	23.7	32.6	---
AREA RANGE COMPARE	ZCP	88	3	5.3	5.4	---	---
DOUBLE AREA RANGE COMPARE	ZCPL	116	3	5.5	6.7	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-6 Data Movement Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
MOVE	MOV	21	3	0.18	0.20	0.29	---
	!MOV	21	7	21.38	21.40	42.36	Increase for immediate refresh
DOUBLE MOVE	MOVL	498	3	0.32	0.34	0.50	---
MOVE NOT	MVN	22	3	0.18	0.20	0.29	---
DOUBLE MOVE NOT	MVNL	499	3	0.32	0.34	0.50	---
MOVE BIT	MOVB	82	4	0.24	0.34	7.5	---
MOVE DIGIT	MOVD	83	4	0.24	0.34	7.3	---
MULTIPLE BIT TRANSFER	XFRB	62	4	10.1	10.8	13.6	Transferring 1 bit
				186.4	189.8	269.2	Transferring 255 bits
BLOCK TRANSFER	XFER	70	4	0.36	0.44	11.2	Transferring 1 word
				300.1	380.1	633.5	Transferring 1,000 words
BLOCK SET	BSET	71	4	0.26	0.28	8.5	Setting 1 word
				200.1	220.1	278.3	Setting 1,000 words
DATA EXCHANGE	XCHG	73	3	0.40	0.56	0.7	---
DOUBLE DATA EXCHANGE	XCGL	562	3	0.76	1.04	1.3	---
SINGLE WORD DISTRIBUTE	DIST	80	4	5.1	5.4	7.0	---
DATA COLLECT	COLL	81	4	5.1	5.3	7.1	---
MOVE TO REGISTER	MOVR	560	3	0.08	0.08	0.50	---
MOVE TIMER/ COUNTER PV TO REGISTER	MOVRW	561	3	0.42	0.50	0.50	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-7 Data Shift Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SHIFT REGISTER	SFT	10	3	7.4	10.4	10.4	Shifting 1 word
				433.2	488.0	763.1	Shifting 1,000 words
REVERSIBLE SHIFT REGISTER	SFTR	84	4	6.9	7.2	9.6	Shifting 1 word
				615.3	680.2	859.6	Shifting 1,000 words
ASYNCHRONOUS SHIFT REGISTER	ASFT	17	4	6.2	6.4	7.7	Shifting 1 word
				1.22 ms	1.22 ms	2.01 ms	Shifting 1,000 words
WORD SHIFT	WSFT	16	4	4.5	4.7	7.8	Shifting 1 word
				171.5	171.7	781.7	Shifting 1,000 words
ARITHMETIC SHIFT LEFT	ASL	25	2	0.22	0.32	0.37	---
DOUBLE SHIFT LEFT	ASLL	570	2	0.40	0.56	0.67	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
ARITHMETIC SHIFT RIGHT	ASR	26	2	0.22	0.32	0.37	---
DOUBLE SHIFT RIGHT	ASRL	571	2	0.40	0.56	0.67	---
ROTATE LEFT	ROL	27	2	0.22	0.32	0.37	---
DOUBLE ROTATE LEFT	ROLL	572	2	0.40	0.56	0.67	---
ROTATE LEFT WITHOUT CARRY	RLNC	574	2	0.22	0.32	0.37	---
DOUBLE ROTATE LEFT WITHOUT CARRY	RLNL	576	2	0.40	0.56	0.67	---
ROTATE RIGHT	ROR	28	2	0.22	0.32	0.37	---
DOUBLE ROTATE RIGHT	RORL	573	2	0.40	0.56	0.67	---
ROTATE RIGHT WITHOUT CARRY	RRNC	575	2	0.22	0.32	0.37	---
DOUBLE ROTATE RIGHT WITH-OUT CARRY	RRNL	577	2	0.40	0.56	0.67	---
ONE DIGIT SHIFT LEFT	SLD	74	3	5.9	6.1	8.2	Shifting 1 word
				561.1	626.3	760.7	Shifting 1,000 words
ONE DIGIT SHIFT RIGHT	SRD	75	3	6.9	7.1	8.7	Shifting 1 word
				760.5	895.5	1.07 ms	Shifting 1,000 words
SHIFT N-BIT DATA LEFT	NSFL	578	4	7.5	8.3	10.5	Shifting 1 bit
				7.5	8.2	55.5	Shifting 1,000 bits
SHIFT N-BIT DATA RIGHT	NSFR	579	4	50.5	55.3	10.5	Shifting 1 bit
				7.4	10.4	69.3	Shifting 1,000 bits
SHIFT N-BITS LEFT	NASL	580	3	0.22	0.32	0.37	---
DOUBLE SHIFT N-BITS LEFT	NSLL	582	3	0.40	0.56	0.67	---
SHIFT N-BITS RIGHT	NASR	581	3	0.22	0.32	0.37	---
DOUBLE SHIFT N-BITS RIGHT	NSRL	583	3	0.40	0.56	0.67	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-8 Increment/Decrement Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
INCREMENT BINARY	++	590	2	0.22	0.32	0.37	---
DOUBLE INCRE-MENT BINARY	++L	591	2	0.40	0.56	0.67	---
DECREMENT BINARY	– –	592	2	0.22	0.32	0.37	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DOUBLE DECREMENT BINARY	– –L	593	2	0.40	0.56	0.67	---
INCREMENT BCD	++B	594	2	6.4	4.5	7.4	---
DOUBLE INCREMENT BCD	++BL	595	2	5.6	4.9	6.1	---
DECREMENT BCD	– –B	596	2	6.3	4.6	7.2	---
DOUBLE DECREMENT BCD	– –BL	597	2	5.3	4.7	7.1	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-9 Symbol Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SIGNED BINARY ADD WITHOUT CARRY	+	400	4	0.18	0.20	0.37	---
DOUBLE SIGNED BINARY ADD WITHOUT CARRY	+L	401	4	0.32	0.34	0.54	---
SIGNED BINARY ADD WITH CARRY	+C	402	4	0.18	0.20	0.37	---
DOUBLE SIGNED BINARY ADD WITH CARRY	+CL	403	4	0.32	0.34	0.54	---
BCD ADD WITHOUT CARRY	+B	404	4	8.2	8.4	14.0	---
DOUBLE BCD ADD WITHOUT CARRY	+BL	405	4	13.3	14.5	19.0	---
BCD ADD WITH CARRY	+BC	406	4	8.9	9.1	14.5	---
DOUBLE BCD ADD WITH CARRY	+BCL	407	4	13.8	15.0	19.6	---
SIGNED BINARY SUBTRACT WITHOUT CARRY	–	410	4	0.18	0.20	0.37	---
DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY	–L	411	4	0.32	0.34	0.54	---
SIGNED BINARY SUBTRACT WITH CARRY	–C	412	4	0.18	0.20	0.37	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DOUBLE SIGNED BINARY SUBTRACT WITH CARRY	–CL	413	4	0.32	0.34	0.54	---
BCD SUBTRACT WITHOUT CARRY	–B	414	4	8.0	8.2	13.1	---
DOUBLE BCD SUBTRACT WITHOUT CARRY	–BL	415	4	12.8	14.0	18.2	---
BCD SUBTRACT WITH CARRY	–BC	416	4	8.5	8.6	13.8	---
DOUBLE BCD SUBTRACT WITH CARRY	–BCL	417	4	13.4	14.7	18.8	---
SIGNED BINARY MULTIPLY	*	420	4	0.38	0.40	0.58	---
DOUBLE SIGNED BINARY MULTIPLY	*L	421	4	7.23	8.45	11.19	---
UNSIGNED BINARY MULTIPLY	*U	422	4	0.38	0.40	0.58	---
DOUBLE UNSIGNED BINARY MULTIPLY	*UL	423	4	7.1	8.3	10.63	---
BCD MULTIPLY	*B	424	4	9.0	9.2	12.8	---
DOUBLE BCD MULTIPLY	*BL	425	4	23.0	24.2	35.2	---
SIGNED BINARY DIVIDE	/	430	4	0.40	0.42	0.83	---
DOUBLE SIGNED BINARY DIVIDE	/L	431	4	7.2	8.4	9.8	---
UNSIGNED BINARY DIVIDE	/U	432	4	0.40	0.42	0.83	---
DOUBLE UNSIGNED BINARY DIVIDE	/UL	433	4	6.9	8.1	9.1	---
BCD DIVIDE	/B	434	4	8.6	8.8	15.9	---
DOUBLE BCD DIVIDE	/BL	435	4	17.7	18.9	26.2	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-10 Conversion Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
BCD-TO-BINARY	BIN	023	3	0.22	0.24	0.29	---
DOUBLE BCD-TO-DOUBLE BINARY	BINL	058	3	6.5	6.8	9.1	---
BINARY-TO-BCD	BCD	024	3	0.24	0.26	8.3	---
DOUBLE BINARY-TO-DOUBLE BCD	BCDL	059	3	6.7	7.0	9.2	---
2'S COMPLEMENT	NEG	160	3	0.18	0.20	0.29	---
DOUBLE 2'S COMPLEMENT	NEGL	161	3	0.32	0.34	0.5	---
16-BIT TO 32-BIT SIGNED BINARY	SIGN	600	3	0.32	0.34	0.50	---
DATA DECODER	MLPX	076	4	0.32	0.42	8.8	Decoding 1 digit (4 to 16)
				0.98	1.20	12.8	Decoding 4 digits (4 to 16)
				3.30	4.00	20.3	Decoding 1 digit 8 to 256
				6.50	7.90	33.4	Decoding 2 digits (8 to 256)
DATA ENCODER	DMPX	077	4	7.5	7.9	10.4	Encoding 1 digit (16 to 4)
				49.6	50.2	59.1	Encoding 4 digits (16 to 4)
				18.2	18.6	23.6	Encoding 1 digit (256 to 8)
				55.1	57.4	92.5	Encoding 2 digits (256 to 8)
ASCII CONVERT	ASC	086	4	6.8	7.1	9.7	Converting 1 digit into ASCII
				11.2	11.7	15.1	Converting 4 digits into ASCII
ASCII TO HEX	HEX	162	4	7.1	7.4	10.1	Converting 1 digit
COLUMN TO LINE	LINE	063	4	19.0	23.1	29.1	---
LINE TO COLUMN	COLM	064	4	23.2	27.5	37.3	---
SIGNED BCD-TO-BINARY	BINS	470	4	8.0	8.3	12.1	Data format setting No. 0
				8.0	8.3	12.1	Data format setting No. 1
				8.3	8.6	12.7	Data format setting No. 2
				8.5	8.8	13.0	Data format setting No. 3
DOUBLE SIGNED BCD-TO-BINARY	BISL	472	4	9.2	9.6	13.6	Data format setting No. 0
				9.2	9.6	13.7	Data format setting No. 1
				9.5	9.9	14.2	Data format setting No. 2
				9.6	10.0	14.4	Data format setting No. 3
SIGNED BINARY-TO-BCD	BCDS	471	4	6.6	6.9	10.6	Data format setting No. 0
				6.7	7.0	10.8	Data format setting No. 1
				6.8	7.1	10.9	Data format setting No. 2
				7.2	7.5	11.5	Data format setting No. 3

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DOUBLE SIGNED BINARY-TO-BCD	BDSL	473	4	8.1	8.4	11.6	Data format setting No. 0
				8.2	8.6	11.8	Data format setting No. 1
				8.3	8.7	12.0	Data format setting No. 2
				8.8	9.2	12.5	Data format setting No. 3

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-11 Logic Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
LOGICAL AND	ANDW	034	4	0.18	0.20	0.37	---
DOUBLE LOGICAL AND	ANDL	610	4	0.32	0.34	0.54	---
LOGICAL OR	ORW	035	4	0.22	0.32	0.37	---
DOUBLE LOGICAL OR	ORWL	611	4	0.32	0.34	0.54	---
EXCLUSIVE OR	XORW	036	4	0.22	0.32	0.37	---
DOUBLE EXCLUSIVE OR	XORL	612	4	0.32	0.34	0.54	---
EXCLUSIVE NOR	XNRW	037	4	0.22	0.32	0.37	---
DOUBLE EXCLUSIVE NOR	XNRL	613	4	0.32	0.34	0.54	---
COMPLEMENT	COM	029	2	0.22	0.32	0.37	---
DOUBLE COMPLEMENT	COML	614	2	0.40	0.56	0.67	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-12 Special Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
BINARY ROOT	ROTB	620	3	49.6	50.0	530.7	---
BCD SQUARE ROOT	ROOT	072	3	13.7	13.9	514.5	---
ARITHMETIC PROCESS	APR	069	4	6.7	6.9	32.3	Designating SIN and COS
				17.2	18.4	78.3	Designating line-segment approximation
FLOATING POINT DIVIDE	FDIV	079	4	116.6	176.6	176.6	---
BIT COUNTER	BCNT	067	4	0.3	0.38	22.1	Counting 1 word

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-13 Floating-point Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
FLOATING TO 16-BIT	FIX	450	3	10.6	10.8	14.5	---
FLOATING TO 32-BIT	FIXL	451	3	10.8	11.0	14.6	---
16-BIT TO FLOATING	FLT	452	3	8.3	8.5	11.1	---
32-BIT TO FLOATING	FLTL	453	3	8.3	8.5	10.8	---
FLOATING-POINT ADD	+F	454	4	8.0	9.2	10.2	---
FLOATING-POINT SUB-TRACT	–F	455	4	8.0	9.2	10.3	---
FLOATING-POINT DIVIDE	/F	457	4	8.7	9.9	12.0	---
FLOATING-POINT MULTIPLY	*F	456	4	8.0	9.2	10.5	---
DEGREES TO RADIANS	RAD	458	3	10.1	10.2	14.9	---
RADIANS TO DEGREES	DEG	459	3	9.9	10.1	14.8	---
SINE	SIN	460	3	42.0	42.2	61.1	---
COSINE	COS	461	3	31.5	31.8	44.1	---
TANGENT	TAN	462	3	16.3	16.6	22.6	---
ARC SINE	ASIN	463	3	17.6	17.9	24.1	---
ARC COSINE	ACOS	464	3	20.4	20.7	28.0	---
ARC TANGENT	ATAN	465	3	16.1	16.4	16.4	---
SQUARE ROOT	SQRT	466	3	19.0	19.3	28.1	---
EXPONENT	EXP	467	3	65.9	66.2	96.7	---
LOGARITHM	LOG	468	3	12.8	13.1	17.4	---
EXPONENTIAL POWER	PWR	840	4	125.4	126.0	181.7	---
Floating Symbol Comparison	LD, AND, OR +=F	329	3	6.6	8.3	---	---
	LD, AND, OR +<>F	330					
	LD, AND, OR +<F	331					
	LD, AND, OR +<=F	332					
	LD, AND, OR +>F	333					
	LD, AND, OR +>=F	334					
FLOATING-POINT TO ASCII	FSTR	448	4	48.5	48.9	---	---
ASCII TO FLOAT-ING-POINT	FVAL	449	3	21.1	21.3	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-14 Double-precision Floating-point Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DOUBLE SYMBOL COMPARISON	LD, AND, OR +=D	335	3	8.5	10.3	---	---
	LD, AND, OR +<>D	336					
	LD, AND, OR +<D	337					
	LD, AND, OR +<=D	338					
	LD, AND, OR +>D	339					
	LD, AND, OR +>=D	340					
DOUBLE FLOATING TO 16-BIT BINARY	FIXD	841	3	11.7	12.1	---	---
DOUBLE FLOATING TO 32-BIT BINARY	FIXLD	842	3	11.6	12.1	---	---
16-BIT BINARY TO DOUBLE FLOATING	DBL	843	3	9.9	10.0	---	---
32-BIT BINARY TO DOUBLE FLOATING	DBLL	844	3	9.8	10.0	---	---
DOUBLE FLOATING-POINT ADD	+D	845	4	11.2	11.9	---	---
DOUBLE FLOATING-POINT SUBTRACT	–D	846	4	11.2	11.9	---	---
DOUBLE FLOATING-POINT MULTIPLY	*D	847	4	12.0	12.7	---	---
DOUBLE FLOATING-POINT DIVIDE	/D	848	4	23.5	24.2	---	---
DOUBLE DEGREES TO RADIANS	RADD	849	3	27.4	27.8	---	---
DOUBLE RADIANS TO DEGREES	DEGD	850	3	11.2	11.9	---	---
DOUBLE SINE	SIND	851	3	45.4	45.8	---	---
DOUBLE COSINE	COSD	852	3	43.0	43.4	---	---
DOUBLE TANGENT	TAND	853	3	20.1	20.5	---	---
DOUBLE ARC SINE	ASIND	854	3	21.5	21.9	---	---
DOUBLE ARC COSINE	ACOSD	855	3	24.7	25.1	---	---
DOUBLE ARC TANGENT	ATAND	856	3	19.3	19.7	---	---
DOUBLE SQUARE ROOT	SQRTD	857	3	47.4	47.9	---	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DOUBLE EXPONENT	EXPD	858	3	121.0	121.4	---	---
DOUBLE LOGARITHM	LOGD	859	3	16.0	16.4	---	---
DOUBLE EXPONENTIAL POWER	PWRD	860	4	223.9	224.2	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-15 Table Data Processing Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SET STACK	SSET	630	3	8.0	8.3	8.5	Designating 5 words in stack area
				231.6	251.8	276.8	Designating 1,000 words in stack area
PUSH ONTO STACK	PUSH	632	3	6.5	8.6	9.1	---
FIRST IN FIRST OUT	FIFO	633	3	6.9	8.9	10.6	Designating 5 words in stack area
				352.6	434.3	1.13 ms	Designating 1,000 words in stack area
LAST IN FIRST OUT	LIFO	634	3	7.0	9.0	9.9	---
DIMENSION RECORD TABLE	DIM	631	5	15.2	21.6	142.1	---
SET RECORD LOCATION	SETR	635	4	5.4	5.9	7.0	---
GET RECORD NUMBER	GETR	636	4	7.8	8.4	11.0	---
DATA SEARCH	SRCH	181	4	15.5	19.5	19.5	Searching for 1 word
				2.42 ms	3.34 ms	3.34 ms	Searching for 1,000 words
SWAP BYTES	SWAP	637	3	12.2	13.6	13.6	Swapping 1 word
				1.94 ms	2.82 ms	2.82 ms	Swapping 1,000 words
FIND MAXIMUM	MAX	182	4	19.2	24.9	24.9	Searching for 1 word
				2.39 ms	3.36 ms	3.36 ms	Searching for 1,000 words
FIND MINIMUM	MIN	183	4	19.2	25.3	25.3	Searching for 1 word
				2.39 ms	3.33 ms	3.33 ms	Searching for 1,000 words
SUM	SUM	184	4	28.2	38.5	38.3	Adding 1 word
				1.42 ms	1.95 ms	1.95 ms	Adding 1,000 words
FRAME CHECKSUM	FCS	180	4	20.0	28.3	28.3	For 1-word table length
				1.65 ms	2.48 ms	2.48 ms	For 1,000-word table length
STACK SIZE READ	SNUM	638	3	6.0	6.3	---	---
STACK DATA READ	SREAD	639	4	8.0	8.4	---	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
STACK DATA OVERWRITE	SWRIT	640	4	7.2	7.6	---	---
STACK DATA INSERT	SINS	641	4	7.8	9.9	---	---
				354.0	434.8	---	For 1,000-word table
STACK DATA DELETE	SDEL	642	4	8.6	10.6	---	---
				354.0	436.0	---	For 1,000-word table

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-16 Data Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
PID CONTROL	PID	190	4	436.2	678.2	678.2	Initial execution
				332.3	474.9	474.9	Sampling
				97.3	141.3	141.3	Not sampling
LIMIT CONTROL	LMT	680	4	16.1	22.1	22.1	---
DEAD BAND CONTROL	BAND	681	4	17.0	22.5	22.5	---
DEAD ZONE CONTROL	ZONE	682	4	15.4	20.5	20.5	---
SCALING	SCL	194	4	37.1	53.0	56.8	---
SCALING 2	SCL2	486	4	28.5	40.2	50.7	---
SCALING 3	SCL3	487	4	33.4	47.0	57.7	---
AVERAGE	AVG	195	4	36.3	52.6	53.1	Average of an operation
				291.0	419.9	419.9	Average of 64 operations
PID CONTROL WITH AUTOTUNING	PIDAT	191	4	446.3	712.5	---	Initial execution
				339.4	533.9	---	Sampling
				100.7	147.1	---	Not sampling
				189.2	281.6	---	Initial execution of autotuning
				535.2	709.8	---	Autotuning when sampling

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-17 Subroutine Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SUBROUTINE CALL	SBS	91	2	1.26	1.96	17.0	---
SUBROUTINE ENTRY	SBN	92	2	---	---	---	---
SUBROUTINE RETURN	RET	93	1	0.86	1.60	20.60	---
MACRO	MCRO	99	4	23.3	23.3	23.3	---
GLOBAL SUBROUTINE CALL	GSBN	751	2	---	---	---	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
GLOBAL SUBROUTINE ENTRY	GRET	752	1	1.26	1.96	---	---
GLOBAL SUBROUTINE RETURN	GSBS	750	2	0.86	1.60	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-18 Interrupt Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SET INTERRUPT MASK	MSKS	690	3	25.6	38.4	39.5	---
READ INTERRUPT MASK	MSKR	692	3	11.9	11.9	11.9	---
CLEAR INTERRUPT	CLI	691	3	27.4	41.3	41.3	---
DISABLE INTERRUPTS	DI	693	1	15.0	16.8	16.8	---
ENABLE INTERRUPTS	EI	694	1	19.5	21.8	21.8	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-19 Step Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
STEP DEFINE	STEP	008	2	17.4	20.7	27.1	Step control bit ON
				11.8	13.7	24.4	Step control bit OFF
STEP START	SNXT	009	2	6.6	7.3	10.0	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-20 Basic I/O Unit Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
I/O REFRESH	IORF	097	3	15.5	16.4	23.5	1-word refresh (IN) for Basic I/O Units
				319.9	320.7	377.6	60-word refresh (IN) for Basic I/O Units
				358.00	354.40	460.1	60-word refresh (OUT) for Basic I/O Units
7-SEGMENT DECODER	SDEC	78	4	6.5	6.9	14.1	---
INTELLIGENT I/O READ	IORD	222	4	Read/write times depend on the Special I/O Unit for which the instruction is being executed.			---
INTELLIGENT I/O WRITE	IOWR	223	4				---
CPU BUS I/O REFRESH	DLNK	226	4	287.8	315.5	---	Allocated 1 word

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-21 Serial Communications Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
PROTOCOL MACRO	PMCR	260	5	100.1	142.1	276.8	Sending 0 words, receiving 0 words
				134.2	189.6	305.9	Sending 249 words, receiving 249 words
TRANSMIT	TXD	236	4	68.5	98.8	98.8	Sending 1 byte
				734.3	1.10 ms	1.10 ms	Sending 256 bytes
RECEIVE	RXD	235	4	89.6	131.1	131.1	Storing 1 byte
				724.2	1.11 ms	1.11 ms	Storing 256 bytes
CHANGE SERIAL PORT SETUP	STUP	237	3	341.2	400.0	440.4	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-22 Network Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
NETWORK SEND	SEND	090	4	84.4	123.9	123.9	---
NETWORK RECEIVE	RECV	098	4	85.4	124.7	124.7	---
DELIVER COMMAND	CMND	490	4	106.8	136.8	136.8	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-23 File Memory Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
READ DATA FILE	FREAD	700	5	391.4	632.4	684.1	2-character directory + file name in binary
				836.1	1.33 ms	1.35 ms	73-character directory + file name in binary
WRITE DATA FILE	FWRIT	701	5	387.8	627.0	684.7	2-character directory + file name in binary
				833.3	1.32 ms	1.36 ms	73-character directory + file name in binary

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-24 Display Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
DISPLAY MESSAGE	MSG	046	3	10.1	14.2	14.3	Displaying message
				8.4	11.3	11.3	Deleting displayed message

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-25 Clock Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
CALENDAR ADD	CADD	730	4	38.3	201.9	209.5	---
CALENDAR SUBTRACT	CSUB	731	4	38.6	170.4	184.1	---
HOURS TO SECONDS	SEC	065	3	21.4	29.3	35.8	---
SECONDS TO HOURS	HMS	066	3	22.2	30.9	42.1	---
CLOCK ADJUSTMENT	DATE	735	2	216.0	251.5	120.0	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-26 Debugging Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
TRACE MEMORY SAMPLING	TRSM	045	1	80.4	120.0	120.0	Sampling 1 bit and 0 words
				848.1	1.06 ms	1.06 ms	Sampling 31 bits and 6 words

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-27 Failure Diagnosis Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
FAILURE ALARM	FAL	006	3	15.4	16.7	16.7	Recording errors
				179.8	244.8	244.8	Deleting errors (in order of priority)
				432.4	657.1	657.1	Deleting errors (all errors)
				161.5	219.4	219.4	Deleting errors (individually)
SEVERE FAILURE ALARM	FALS	007	3	---	---	---	---
FAILURE POINT DETECTION	FPD	269	4	140.9	202.3	202.3	When executed
				163.4	217.6	217.6	First time
				185.2	268.9	268.9	When executed
				207.5	283.6	283.6	First time

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-28 Other Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SET CARRY	STC	040	1	0.06	0.06	0.12	---
CLEAR CARRY	CLC	041	1	0.06	0.06	0.12	---
SELECT EM BANK	EMBC	281	2	14.0	15.1	15.1	---
EXTEND MAXIMUM CYCLE TIME	WDT	094	2	15.0	19.7	19.7	---

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
SAVE CONDITION FLAGS	CCS	282	1	8.6	12.5	---	---
LOAD CONDITION FLAGS	CCL	283	1	9.8	13.9	---	---
CONVERT ADDRESS FROM CV	FRMCV	284	3	13.6	19.9	---	---
CONVERT ADDRESS TO CV	TOCV	285	3	11.9	17.2	---	---
DISABLE PERIPHERAL SERVICING	IOSP	287	---	13.9	19.8	---	---
ENABLE PERIPHERAL SERVICING	IORS	288	---	63.6	92.3	---	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-29 Block Programming Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
BLOCK PROGRAM BEGIN	BPRG	096	2	12.1	13.0	13.0	---
BLOCK PROGRAM END	BEND	801	1	9.6	12.3	13.1	---
BLOCK PROGRAM PAUSE	BPPS	811	2	10.6	12.3	14.9	---
BLOCK PROGRAM RESTART	BPRS	812	2	5.1	5.6	8.3	---
CONDITIONAL BLOCK EXIT	(Execution condition) EXIT	806	1	10.0	11.3	12.9	EXIT condition satisfied
				4.0	4.9	7.3	EXIT condition not satisfied
CONDITIONAL BLOCK EXIT	EXIT (bit address)	806	2	6.8	13.5	16.3	EXIT condition satisfied
				4.7	7.2	10.7	EXIT condition not satisfied
CONDITIONAL BLOCK EXIT (NOT)	EXIT NOT (bit address)	806	2	12.4	14.0	16.8	EXIT condition satisfied
				7.1	7.6	11.2	EXIT condition not satisfied
Branching	IF (execution condition)	802	1	4.6	4.8	7.2	IF true
				6.7	7.3	10.9	IF false
Branching	IF (relay number)	802	2	6.8	7.2	10.4	IF true
				9.0	9.6	14.2	IF false
Branching (NOT)	IF NOT (relay number)	802	2	7.1	7.6	10.9	IF true
				9.2	10.1	14.7	IF false
Branching	ELSE	803	1	6.2	6.7	9.9	IF true
				6.8	7.7	11.2	IF false
Branching	IEND	804	1	6.9	7.7	11.0	IF true
				4.4	4.6	7.0	IF false

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
ONE CYCLE AND WAIT	WAIT (execution condition)	805	1	12.6	13.7	16.7	WAIT condition satisfied
				3.9	4.1	6.3	WAIT condition not satisfied
ONE CYCLE AND WAIT	WAIT (relay number)	805	2	12.0	13.4	16.5	WAIT condition satisfied
				6.1	6.5	9.6	WAIT condition not satisfied
ONE CYCLE AND WAIT (NOT)	WAIT NOT (relay number)	805	2	12.2	13.8	17.0	WAIT condition satisfied
				6.4	6.9	10.1	WAIT condition not satisfied
COUNTER WAIT	CNTW	814	4	17.9	22.6	27.4	Default setting
				19.1	23.9	28.7	Normal execution
HIGH-SPEED TIMER WAIT	TMHW	815	3	25.8	27.9	34.1	Default setting
				20.6	22.7	28.9	Normal execution
Loop Control	LOOP	809	1	7.9	9.1	12.3	---
Loop Control	LEND (execution condition)	810	1	7.7	8.4	10.9	LEND condition satisfied
				6.8	8.0	9.8	LEND condition not satisfied
Loop Control	LEND (relay number)	810	2	9.9	10.7	14.4	LEND condition satisfied
				8.9	10.3	13.0	LEND condition not satisfied
Loop Control	LEND NOT (relay number)	810	2	10.2	11.2	14.8	LEND condition satisfied
				9.3	10.8	13.5	LEND condition not satisfied
TIMER WAIT	TIMW	813	3	22.3	25.2	33.1	Default setting
				24.9	27.8	35.7	Normal execution

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-30 Text String Processing Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
MOV STRING	MOV$	664	3	45.6	66.0	84.3	Transferring 1 character
CONCATENATE STRING	+$	656	4	86.5	126.0	167.8	1 character + 1 character
GET STRING LEFT	LEFT$	652	4	53.0	77.4	94.3	Retrieving 1 character from 2 characters
GET STRING RIGHT	RGHT$	653	4	52.2	76.3	94.2	Retrieving 1 character from 2 characters
GET STRING MIDDLE	MID$	654	5	56.5	84.6	230.2	Retrieving 1 character from 3 characters
FIND IN STRING	FIND$	660	4	51.4	77.5	94.1	Searching for 1 character from 2 characters
STRING LENGTH	LEN$	650	3	19.8	28.9	33.4	Detecting 1 character

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
REPLACE IN STRING	RPLC$	661	6	175.1	258.7	479.5	Replacing the first of 2 characters with 1 character
DELETE STRING	DEL$	658	5	63.4	94.2	244.6	Deleting the leading character of 2 characters
EXCHANGE STRING	XCHG$	665	3	60.6	87.2	99.0	Exchanging 1 character with 1 character
CLEAR STRING	CLR$	666	2	23.8	36.0	37.8	Clearing 1 character
INSERT INTO STRING	INS$	657	5	136.5	200.6	428.9	Inserting 1 character after the first of 2 characters
String Comparison Instructions	LD, AND, OR +=$	670	4	48.5	69.8	86.2	Comparing 1 character with 1 character
	LD, AND, OR +<>$	671					
	LD, AND, OR +<$	672					
	LD, AND, OR +>$	674					
	LD, AND, OR +>=$	675					

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

10-5-31 Task Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note.)	ON execution time (μs)			Conditions
				CPU6□H	CPU4□H	CPU4□	
TASK ON	TKON	820	2	19.5	26.3	26.3	---
TASK OFF	TKOF	821	2	13.3	19.0	26.3	---

10-5-32 Guidelines on Converting Program Capacities from Previous OMRON PCs

Guidelines are provided in the following table for converting the program capacity (unit: words) of previous OMRON PCs (SYSMAC C200HX/HG/HE, CVM1, or CV-series PCs) to the program capacity (unit: steps) of the CJ-series PCs.

Add the following value (n) to the program capacity (unit: words) of the previous PCs for each instruction to obtain the program capacity (unit: steps) of the CJ-series PCs.

CJ-series steps = "a" (words) of previous PC + n			
Instructions	**Variations**	**Value of n when converting from C200HX/HG/HE to CJ Series**	**Value of n when converting from CV-series PC or CVM1 to CJ Series**
Basic instructions	None	OUT, SET, RSET, or KEEP(011): –1 Other instructions: 0	0
	Upward Differentiation	None	+1
	Immediate Refreshing	None	0
	Upward Differentiation and Immediate Refreshing	None	+2
Special instructions	None	0	–1
	Upward Differentiation	+1	0
	Immediate Refreshing	None	+3
	Upward Differentiation and Immediate Refreshing	None	+4

For example, if OUT is used with an address of CIO 000000 to CIO 25515, the program capacity of the previous PC would be 2 words per instruction and that of the CJ-series PC would be 1 (2 – 1) step per instruction.

For example, if !MOV is used (MOVE instruction with immediate refreshing), the program capacity of a CV-series PC would be 4 words per instruction and that of the CJ-series PC would be 7 (4 + 3) steps.

SECTION 11
Troubleshooting

This section provides information on hardware and software errors that occur during PC operation.

11-1 Error Log

Each time that an error occurs in a CJ PC, the CPU Unit stores error information in the Error Log Area. The error information includes the error code (stored in A400), error contents, and time that the error occurred. Up to 20 records can be stored in the Error Log.

Errors Generated by FAL(006)/FALS(007)

In addition to system-generated errors, the PC records user-defined FAL(006) and FALS(007) errors, making it easier to track the operating status of the system.

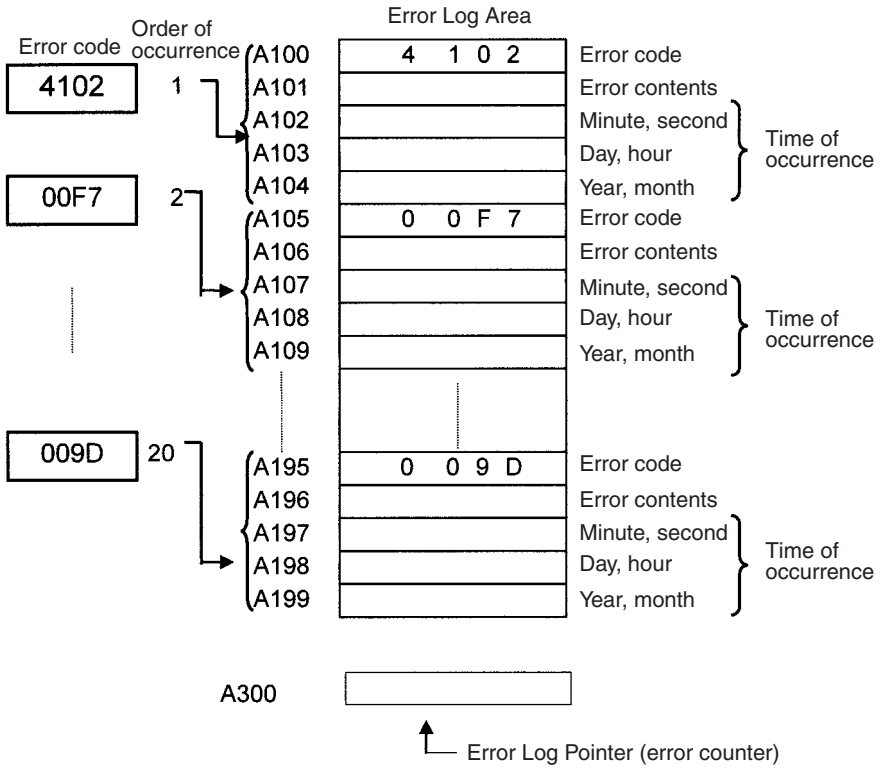
A user-defined error is generated when FAL(006) or FALS(007) is executed in the program. The execution conditions of these instructions constitute the user-defined error conditions. FAL(006) generates a non-fatal error and FALS(007) generates a fatal error that stops program execution.

The following table shows the error codes for FAL(006) and FALS(007).

Instruction	FAL numbers	Error codes
FAL(006)	#0001 to #01FF (1 to 511 decimal)	4101 to 42FF
FALS(007)	#0001 to #01FF (1 to 511 decimal)	C101 to C2FF

Error Log Structure

When more than 20 errors occur, the oldest error data (in A195 to A199) is deleted and the newest record is stored in A100 to A104.



Note The Error Log Pointer can be reset by turning ON the Error Log Pointer Reset Bit (A50014), effectively clearing the error log displays from the Programming Consoles or CX-Programmer. The contents of the Error Log Area will not be cleared by resetting the pointer.

11-2 Error Processing

11-2-1 Error Categories

Errors in CJ-series PCs can be broadly divided into the following three categories.

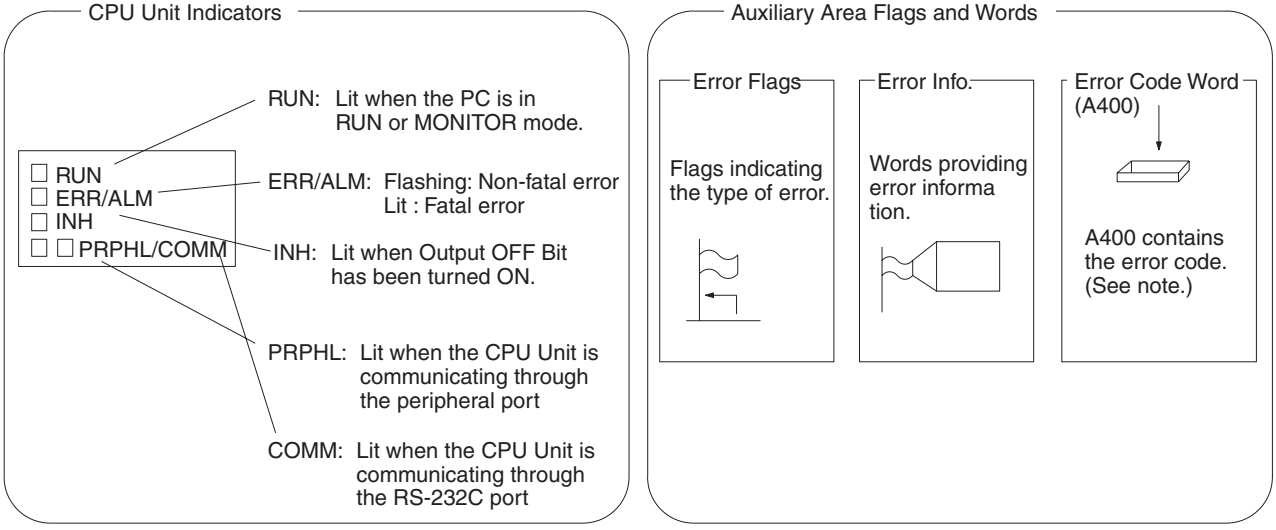
Category	Result	Indicators		Comments
		RUN	ERR/ALM	
CPU Standby	The CPU Unit will not start operation in RUN or MONITOR mode.	OFF	OFF	---
Non-fatal Errors (including FAL(006))	The CPU Unit will continue operating in RUN or MONITOR mode.	ON (Green)	Flashing (Red)	Other indicators will also operate when a communications error has occurred or the Output OFF Bit is ON.
Fatal Errors (including FALS(007))	The CPU Unit will stop operating in RUN or MONITOR mode.	OFF	ON (Red)	The indicators will all be OFF when there is a power interruption.

11-2-2 Error Information

There are basically four sources of information on errors that have occurred:

1,2,3...

1. The CPU Unit's indicators
2. The Auxiliary Area Error Flags
3. The Auxiliary Area Error Information Words
4. The Auxiliary Area Error Code Word



Note When two or more errors occur at the same time, the highest (most serious) error code will be stored in A400.

Indicator Status and Error Conditions

The following table shows the status of the CPU Unit's indicators for errors that have occurred in RUN or MONITOR mode.

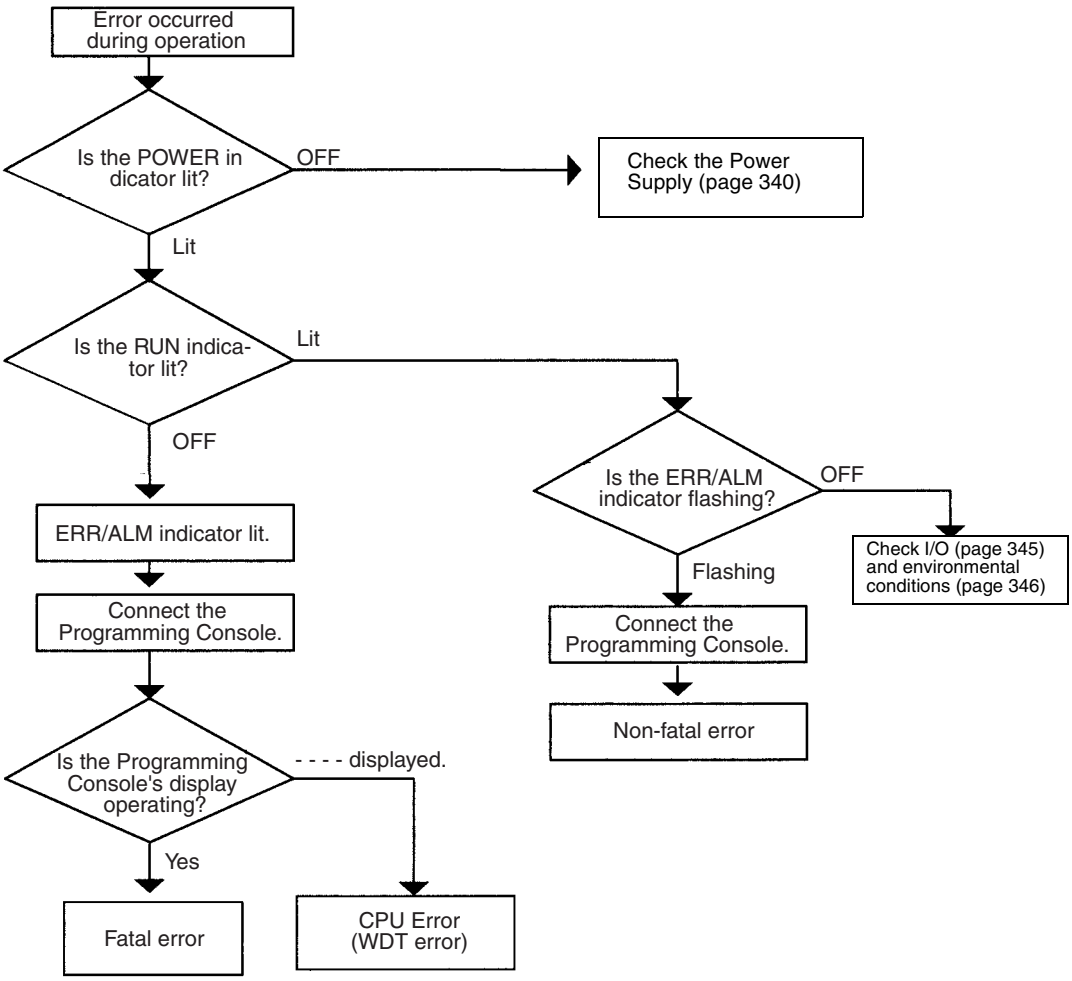
Indicator*	CPU error	CPU standby	Fatal error	Non-fatal error	Communications error		Output OFF Bit ON
					Peripheral	RS-232C	
RUN	OFF	OFF	OFF	ON	ON	ON	ON
ERR/ALM	ON	OFF	ON	Flashing	---	---	---
INH	OFF	---	---	---	---	---	ON
PRPHL	---	---	---	---	OFF	---	---
COMM	---	---	---	---	---	OFF	---

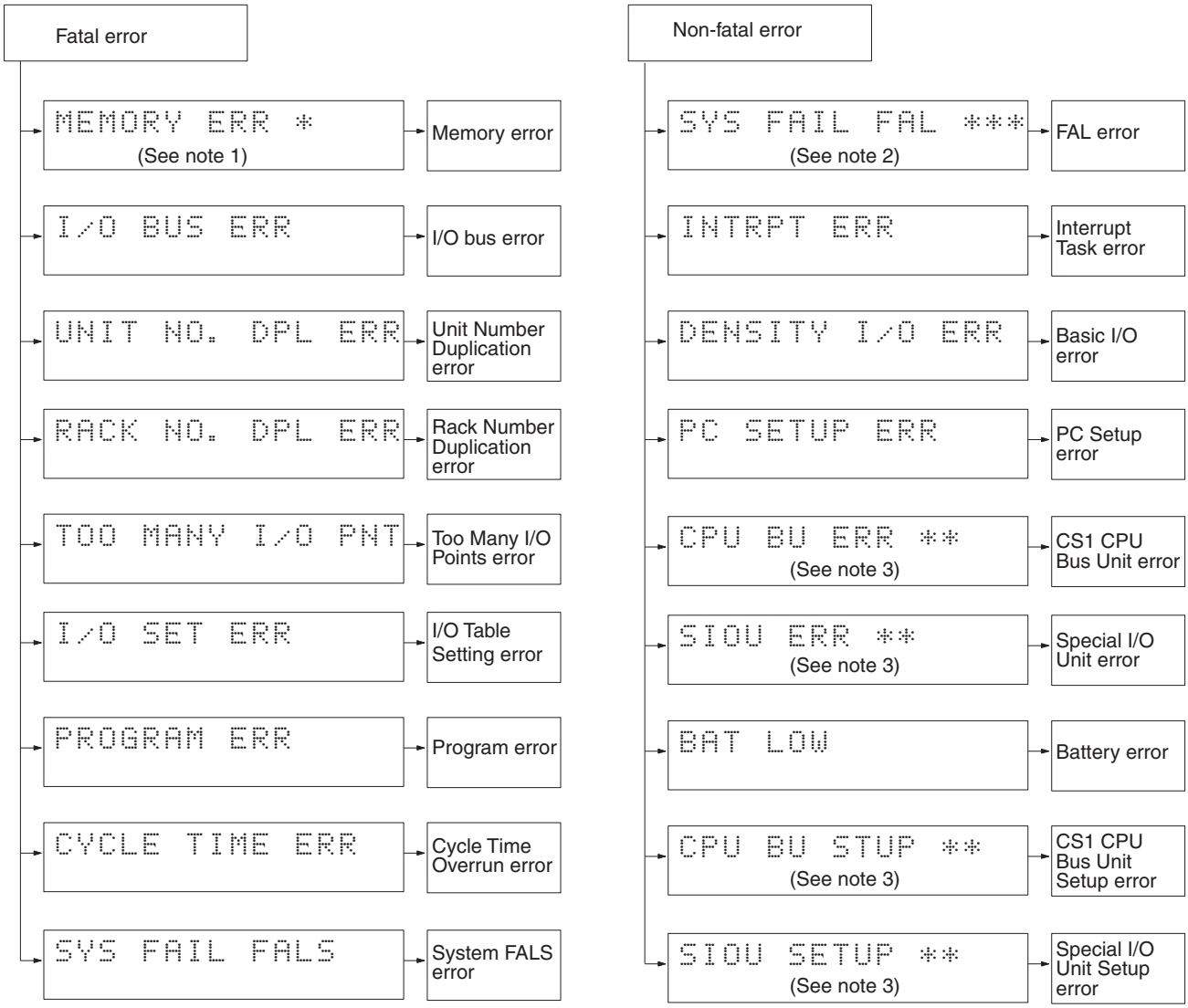
11-2-3 Error Codes and Error Flags

Classification	Error code	Error name	Page
Fatal system errors	80F1	Memory error	332
	80C0 to 80C7, 80CE, 80CF	I/O bus error	332
	80E9	Duplicated number error	333
	80E1	Too many I/O points	335
	80E0	I/O setting error	335
	80F0	Program error	334
	809F	Cycle time too long	336
	80EA	Expansion Rack number duplicated	333
Non-fatal system errors	008B	Interrupt task error	337
	009A	Basic I/O error	337
	009B	PC Setup setting error	337
	00E7	I/O verification error	335
	0200 to 020F	CJ-series CPU Bus Unit error	338
	0300 to 035F, 03FF	Special I/O Unit error	338
	00F7	Battery error	338
	0400 to 040F	CJ-series CPU Bus Unit setting error	338
	0500 to 055F	Special I/O Unit setting error	338
User-defined fatal errors	4101 to 42FF	FAL(006) error (4101 to 42FF are stored for FAL numbers 001 to 511)	337
User-defined non-fatal errors	C101 to C2FF	FALS(007) error (C101 to C2FF are stored for FALS numbers 001 to 511)	336

11-2-4 Error Processing Flowchart

Use the following flowchart as a guide for error processing with a Programming Console.





1. The rack number will be given at *.
2. The FAL./FALS number will be given at ***.
3. The unit number will be given at **.
4. The master number will be given at *.

11-2-5 Error Messages

The following tables show error messages for errors which can occur in CJ-series PCs and indicate the likely cause of the errors.

CPU Errors

A CPU error has occurred if the indicators have the following conditions in RUN or MONITOR mode. A Programming Device cannot be connected to the CPU if an CPU error has occurred.

Note If a fatal operating error occurs, the indicators will be the same as shown below for CPU errors, but a Programming Device can be connected. This will enable distinguishing between the two types of error.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	---	ON	---	---	---

Status	Error	Program-ming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
Stopped	CPU error (WDT error)	– – – –	None	None	None	Watchdog timer has exceeded maxi-mum setting. (This error does not nor-mally occur)	Turn the power OFF and restart. The Unit may be damaged. Contact you OMRON representative.

CPU Reset

The following indictor status shows that the CPU Unit has been reset (not a CPU error). A Programming Device cannot be connected.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	---	---	---	---	---

Status	Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags	Probable cause	Possible remedy
Stopped	CPU reset	– – – –	None	None	None	Power is not being supplied to an Expansion Rack.	Supply power to the Expansion Racks.
						I/O Control Unit is not connected correctly, e.g., more than one is connected or one is connected to an Expansion Rack.	Turn OFF the power supply, correct the connections, and turn the power supply back ON.
						The I/O Connecting cable is not connected correctly, e.g., the connections to the input and output connectors on the I/O Interface Unit are backward.	Turn OFF the power supply, correct the connections, and turn the power supply back ON.

Note When power supply is interrupted to an Expansion Rack, the CPU Unit will stop program execution and the same operations as are performed when the power supply to the CPU Unit is interrupted will be performed. For example, if the power OFF interrupt task is enabled, it will be executed. If power is then restored to the Expansion Rack, the CPU Unit will perform startup processing, i.e., the same operational status as existed before the power interrupt will not necessarily be continued.

CPU Standby Errors

A CPU standby error has occurred if the indicators have the following conditions in RUN or MONITOR mode.

When a CJ-series CPU Unit is turned ON, cyclic servicing is started and RUN mode is entered only after all Special I/O Units and CPU Bus Units have been detected. If the startup mode is RUN or MONITOR mode, the CPU will remain on standby until all Units have been directed.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	OFF	OFF	---	---	---

Status	Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags	Probable cause	Possible remedy
Stopped	CPU standby error	CPU WAIT'G	None	None	None	A CPU Bus Unit has not started properly.	Check the settings of the CPU Bus Unit.
						A Special I/O Unit, or Interrupt Input Unit was not recognized.	Read the I/O table and replace any Special I/O Unit or Interrupt Input Units for which only "$" is displayed.

Startup Condition

The CJ1-H CPU Units support a Startup Condition setting.

To start the CPU Unit in MONITOR or PROGRAM mode even if there is one or more Units that has not completed startup processing, set the Startup Condition to 1.

PC Setup

Programming Console setting address		Name	Settings	Default
Word	Bit			
83	15	Startup Condition	0: Wait for Units. 1: Don't wait.	0: Wait for Units.

Fatal Errors

A fatal error has occurred if the indicators have the following conditions in RUN or MONITOR mode.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	OFF	ON	---	---	---

Connect a Programming Console to display the error message or use the error log window on the CX-Programmer. The cause of the error can be determined from the error message and related Auxiliary Area flags and words.

Errors are listed in order of importance. When two or more errors occur at the same time, the more serious error's error code will be recorded in A400.

If the IOM Hold Bit hasn't been turned ON to protect I/O memory, all non-retained areas of I/O memory will be cleared when a fatal error other than FALS(007) occurs. If the IOM Hold Bit is ON, the contents of I/O memory will be retained but all outputs will be turned OFF.

If the IOM Hold Bit hasn't been turned ON to protect I/O memory, all non-retained areas of I/O memory will be cleared when a fatal error other than FALS(007) occurs. When the IOM Hold Bit is ON, the contents of I/O memory will be retained but all outputs will be turned OFF.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
Memory error	MEMORY ERR	80F1	A40115: Memory Error Flag A403: Memory Error Location	An error has occurred in memory. A bit in A403 will turn ON to show the location of the error as listed below.	See below.
				A40300 ON: A checksum error has occurred in the user program memory. An illegal instruction was detected.	Check the program and correct the error.
				A40304 ON: A checksum error has occurred in the PC Setup.	Clear the entire PC Setup to 0000 and reenter the settings.
				A40305 ON: A checksum error has occurred in the registered I/O table.	Initialize the registered I/O table and generate a new I/O table.
				A40307 ON: A checksum error has occurred in the routing tables.	Initialize the routing tables and reenter the tables.
				A40308 ON: A checksum error has occurred in the CPU Bus Unit setup.	Initialize the CPU Bus Unit setup and reenter the settings.
				A40309 ON: An error occurred during automatic transfer from the Memory Card at startup.	Make sure that the Memory Card is installed properly and that the correct file is on the Card.
				A40310 ON: An error occurred in flash memory (backup memory).	CPU Unit hardware is faulty. Replace the CPU Unit.
I/O Bus error	I/O BUS ERR	80C0 to 80CE or 80CF	A40114: I/O Bus Error Flag A404: I/O Bus Error Slot and Rack Numbers	Error has occurred in the bus line between the CPU and I/O Units or the End Cover is not connected to the CPU Rack or an Expansion Rack. A40400 to A40407 contain the error slot number (00 to 09) in binary. 0F Hex indicates that the slot cannot be determined. 0E Hex indicates the End Cover is not connected to the CPU Rack or an Expansion Rack. A40408 to A40415 contain the error rack number (00 to 03) in binary. 0F Hex indicates that the rack cannot be determined. 0E Hex indicates the End Cover is not connected to the CPU Rack or an Expansion Rack.	Try turning the power OFF and ON again. If the error isn't corrected, turn the power OFF and check cable connections between the I/O Units and Racks and the End Covers. Check for damage to the cable or Units. Turn the Rack's power supply OFF and then ON again.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
Unit/Rack Number Duplication error	UNIT No. DPL ERR	80E9	A40113: Duplication Error Flag A410: CPU Bus Unit Duplicate Number Flags	The same number has been allocated to more than one CPU Bus Unit. Bits A41000 to A41015 correspond to unit numbers 0 to F.	Check the unit numbers, eliminate the duplications, and turn the Rack's power supply OFF and then ON again.
			A40113: Duplication Error Flag A411 to A416: Special I/O Unit Duplicate Number Flags	The same number has been allocated to more than one Special I/O Unit. Bits A41100 to A41615 correspond to unit numbers 0 to 95.	Check the unit numbers, eliminate the duplications, and turn the Rack's power supply OFF and then ON again.
	RACK No. DPL ERR	80EA	A409: Expansion Rack Duplicate Rack Number	The same I/O word has been allocated to more than one Basic I/O Unit.	Check allocations to Units on the rack number whose bit in ON in A40900 to A40903. Correct the allocations so that no words are allocated more than once, including to Units on other Racks, and turn the Rack's power supply OFF and then ON again.
				An Expansion Rack's starting word address exceeds CIO 0901. The corresponding bit in A40900 to A40903 (Racks 0 to 3) will be turned ON.	Check the first word setting for the Rack indicated in A40900 to A40903 and change the setting to a valid word address below CIO 0900 with a Programming Device.
Program error	PROGRAM ERR	80F0	A40109: Program Error Flag A294 to A299: Program error information	The program is incorrect. See the following rows of this table for details. The address at which the program stopped will be output to A298 and A299.	Check A295 to determine the type of error that occurred and check A298/A299 to find the program address where the error occurred. Correct the program and then clear the error.
				A29511: No END error	Be sure that there is an END(001) instruction at the end of the task specified in A294 (program stop task number). The address where the END(001)
				A29515: UM overflow error The last address in UM (user program memory) has been exceeded.	Use a Programming Device to transfer the program again.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
Program error (cont.)	PROGRAM ERR	80F0	A40109: Program Error Flag A294 to A299: Program error information	A29513: Differentiation overflow error Too many differentiated instructions have been inserted or deleted during online editing.	After writing any changes to the program, switch to PROGRAM mode and then return to MONITOR mode to continue editing the program.
				A29512: Task error A task error has occurred. The following conditions will generate a task error. 1) There isn't an executable cyclic task. 2) There isn't a program allocated to the task. Check A294 for the number of the task missing a program. 3) The task specified in a TKON(820), TKOF(821), or MSKS(690) instruction doesn't exist.	Check the startup cyclic task attributes. Check the execution status of each task as controlled by TKON(820) and TKOF(821). Make sure that all of the task numbers specified in TKON(820), TKOF(821), and MSKS(690) instructions have corresponding tasks. Use MSKS(690) to mask any I/O or scheduled interrupt tasks that are not being used and that do not have programs set for them.
				A29510: Illegal access error An illegal access error has occurred and the PC Setup has been set to stop operation for an instruction error. The following are illegal access errors: 1. Reading/writing a parameter area. 2. Writing memory that is not installed. 3. Writing an EM bank that is EM file memory. 4. Writing to a read-only area. 5. Indirect DM/EM address that is not in BCD when BCD mode is specified.	Find the program address where the error occurred (A298/A299) and correct the instruction.
				A29509: Indirect DM/EM BCD error An indirect DM/EM BCD error has occurred and the PC Setup has been set to stop operation for an instruction error.	Find the program address where the error occurred (A298/A299) and correct the indirect addressing or change to binary mode.
				A29508: Instruction error An instruction processing error has occurred and the PC Setup has been set to stop operation for an instruction error.	Find the program address where the error occurred (A298/A299) and correct the instruction.
				A29514: Illegal instruction error The program contains an instruction that cannot be executed.	Retransfer the program to the CPU Unit.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
Too Many I/O Points error	TOO MANY I/O PNT	80E1	A40111: Too Many I/O Points Flag A407: Too Many I/O Points, Details	The probable causes are listed below. The 3-digit binary value (000 to 101) in A40713 to A40715 indicates the cause of the error. The value of these 3 bits is also output to A40700 to A40712. 1) The total number of I/O points set in the I/O Table exceeds the maximum allowed for the CPU Unit 2) The number of Expansion Racks exceeds the maximum (bits: 101). 3) More than 10 I/O Units are connected to one Rack (bits: 111).	Correct the problem and then turn the power supply OFF and back ON.
I/O Table Setting error	I/O SET ERR	80E0	A40110: I/O Setting Error Flag	The Units that are connected do not agree with the registered I/O table or the number of Units that are connected does not agree with the number in the registered I/O table. (The following Units must be set as a 16-point Units in the I/O tables made on the CX-Programmer because they are allocated 1 word each even though they have only 8 points: CJ1W-OC201, CJ1W-I1201, CJ1W-OA201, and CJ1W-OD201/202. An I/O setting error will occur if this Unit is set as an 8-point Unit.)	Any discrepancies in the I/O table will be detected when the I/O verification operation is performed. If this error occurs even when the number Units is correct, there may be a faulty Unit. Automatically create the I/O tables and check for Units that are not being detected. If the number of Units is not correct, turn OFF the power supply and correctly connect the proper Units. If the number of Units is correct, confirm the Unit in discrepancy, turn OFF the power supply, and then correct the Unit connections. If there is a mistake in the I/O tables, recreate or edit them to correct the mistake.
				An Interrupt Input Unit has been connected in the wrong position (not in one of the five positions next to the CPU Unit) or has been registered in the Registered I/O Tables in the wrong position.	A40508 will turn ON if an Interrupt Input Unit is in the wrong position (i.e., either physically in the wrong position in the system or registered in the wrong position in the Registered I/O Tables).

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
Cycle Time Overrun error	CYCLE TIME ERR	809F	A40108: Cycle Time Too Long Flag	The cycle time has exceeded the maximum cycle time (watch cycle time) set in the PC Setup.	Change the program to reduce the cycle time or change the maximum cycle time setting. Check the Maximum Interrupt Task Processing Time in A440 and see if the Cycle Time Watch Time can be changed. The cycle time can be reduced by dividing unused parts of the program into tasks, jumping unused instructions in tasks, and disabling cyclic refreshing of Special I/O Units that don't require frequent refreshing.
	CYCLE TIME OVER	809F	A40515: Peripheral Servicing Cycle Time Too Long	Turns ON when the peripheral servicing time in a Parallel Processing Mode exceeds 2 s.	Change the CPU Processing Mode in the PC Setup to Normal Mode or Peripheral Servicing Priority Mode, or review the system to reduce the event load. Parallel processing may not be possible if the program execution time (given in A66) is too short (e.g., less than 0.2 ms).
System FALS error	SYS FAIL FALS	C101 to C2FF	A40106: FALS Error Flag	FALS(007) has been executed in the program. The error code in A400 will indicate the FAL number. The leftmost digit of the code will be C and the rightmost 3 digits of the code will be from 100 to 2FF Hex and will correspond to FAL numbers 001 to 511.	Correct according to cause indicated by the FAL number (set by user).

Non-fatal Errors

A non-fatal error has occurred if the indicators have the following conditions in RUN or MONITOR mode.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	ON	Flashing	---	---	---

Connect a Programming Console to display the error message or use the error log window on the CX-Programmer. The cause of the error can be determined from the error message and related Auxiliary Area flags and words.

Errors are listed in order of importance. When two or more errors occur at the same time, the more serious error's error code will be recorded in A400.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
System FAL error	SYS FAIL FAL	4101 to 42FF	A40215: FAL Error Flag A360 to A391: Executed FAL Number Flags	FAL(006) has been executed in program. Executed FAL Number Flags A36001 to A39115 correspond to FAL numbers 001 to 511. The error code in A400 will indicate the FAL number. The leftmost digit of the code will be 4 and the rightmost 3 digits of the code will be from 100 to 2FF Hex and will correspond to FAL numbers 001 to 511.	Correct according to cause indicated by FAL number (set by user).
Interrupt Task error	INTRPT ERR	008B	A40213: Interrupt Task Error Flag A426: Interrupt Task Error, Task Number	PC Setup Set to Detect Interrupt Task Errors: Attempted to refresh a Special I/O Unit's I/O from an interrupt task with IORF(097) while the Unit's I/O was being refreshed by cyclic I/O refreshing (duplicate refreshing).	Check the program. Either disable detection of interrupt task errors in the PC Setup (address 128, bit 14) or correct the problem in the program.
Basic I/O error	DENSITY I/O ERR	009A	A40212: Basic I/O Unit Error Flag A408: Basic I/O Unit Error, Slot Number	An error has occurred in a Basic I/O Unit. A408 contains the errant rack/slot number.	Check the errant Unit for blown fuse, etc.
PC Setup error	PC SETUP ERR	009B	A40210: PC Setup Error Flag A406: PC Setup Error Location	There is a setting error in the PC Setup. The location of the error is written to A406.	Change the indicated setting to a valid setting.

Error	Programming Console display	Error code (in A400)	Flag and word data	Probable cause	Possible remedy
CPU Bus Unit error	CPU BU ERR	0200 to 020F	A40207: CPU Bus Unit Error Flag A417: CPU Bus Unit Error, Unit Number Flags	An error occurred in a data exchange between the CPU Unit and a CPU Bus Unit. The corresponding flag in A417 is turned ON to indicate the problem Unit. Bits A41700 to A41715 correspond to unit numbers 0 to F.	Check the Unit indicated in A417. Refer to the Unit's operation manual to find and correct the cause of the error. Restart the Unit by toggling its Restart Bit or turn the power OFF and ON again. Replace the Unit if it won't restart.
Special I/O Unit error	SIOU ERR	0300 to 035F, or 03FF	A40206: Special I/O Unit Error Flag A418 to A423: Special I/O Unit Error, Unit Number Flags	An error occurred in a data exchange between the CPU Unit and a Special I/O Unit. The corresponding flag in A418 to A423 is turned ON to indicate the problem Unit. Bits A41800 to A42315 correspond to unit numbers 0 to 95.	Check the Unit indicated in A418 to A423. Refer to the Unit's operation manual to find and correct the cause of the error. Restart the Unit by toggling its Restart Bit or turn the power OFF and ON again. Replace the Unit if it won't restart.
Battery error	BATT LOW	00F7	A40204: Battery Error Flag	This error occurs when the PC Setup has been set to detect battery errors and the CPU Unit's backup battery is missing or its voltage has dropped.	Check battery and replace if necessary. Change the PC Setup setting if battery-free operation is being used.
CPU Bus Unit Setup error	CPU BU ST ERR	0400 to 040F	A40203: CPU Bus Unit Setting Error Flag A427: CPU Bus Unit Setting Error, Unit Number Flags	An installed CPU Bus Unit does not match the CPU Bus Unit registered in the I/O table. The corresponding flag in A427 will be ON. Bits 00 to 15 correspond to unit numbers 0 to F.	Change the registered I/O table.
Special I/O Unit Setup error	SIOU SETUP ERR	0500 to 055F	A40202: Special I/O Unit Setting Error Flag A428 to A433: Special I/O Unit Setting Error, Unit Number Flags	An installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table. The corresponding flag in A428 to A433 will be ON. Bits A42800 to A43315 correspond to unit numbers 0 to 95.	Change the registered I/O table.

Other Errors

Peripheral Port Communications Error

A communications error has occurred in communications with the device connected to the peripheral port if the indicators have the following conditions.

Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	ON	---	---	OFF	---

Check the setting of pin 4 on the DIP switch and the peripheral port settings in the PC Setup. Also check the cable connections.

RS-232C Port Communications Error

A communications error has occurred in communications with the device connected to the RS-232C port if the indicators have the following conditions.

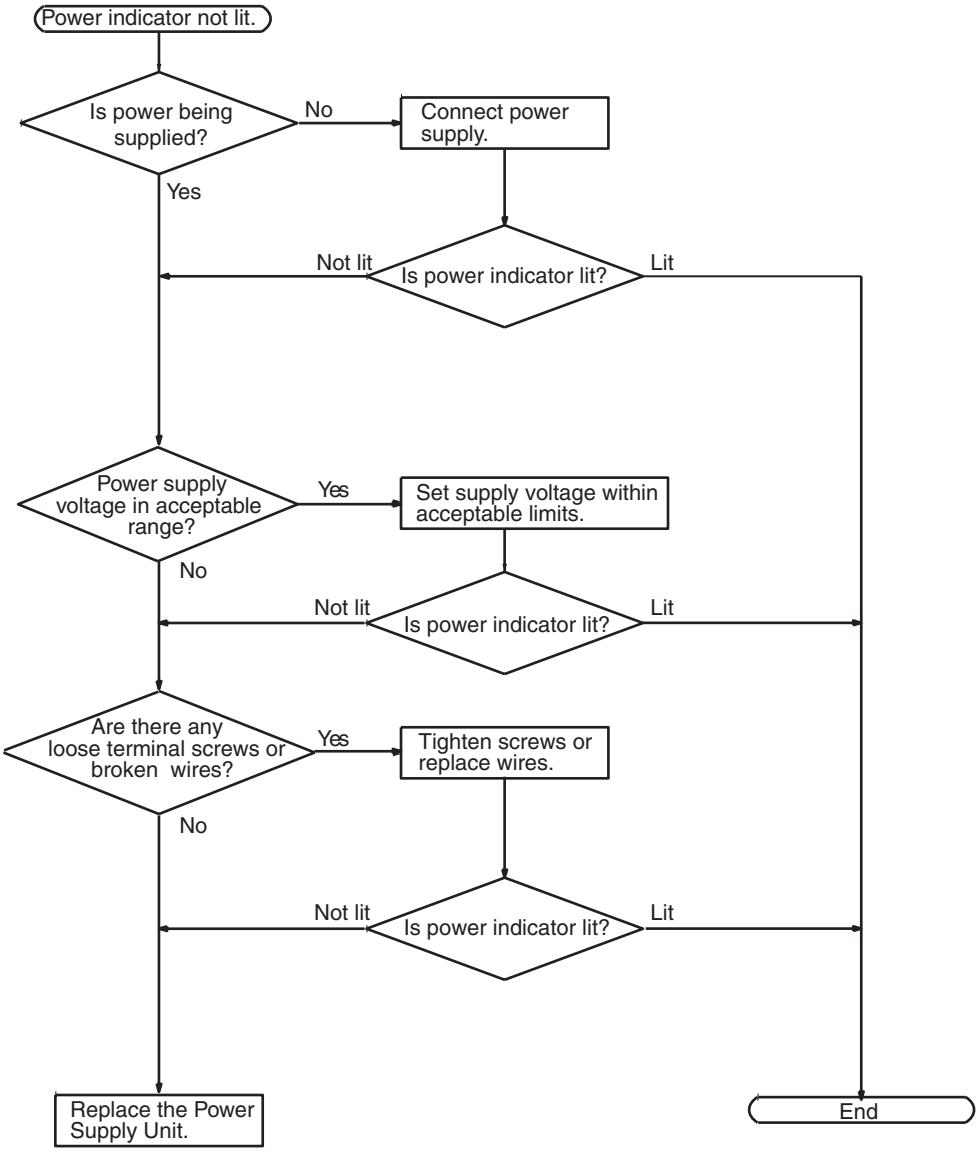
Power Supply Unit Indicator	CPU Unit Indicators				
POWER	RUN	ERR/ALM	INH	PRPHL	COMM
ON	---	---	---	---	OFF

Check the setting of pin 5 on the DIP switch and the RS-232C port settings in the PC Setup. Also check the cable connections. If a host computer is connected, check the communications settings of the serial port on the host computer and the communications program in the host computer.

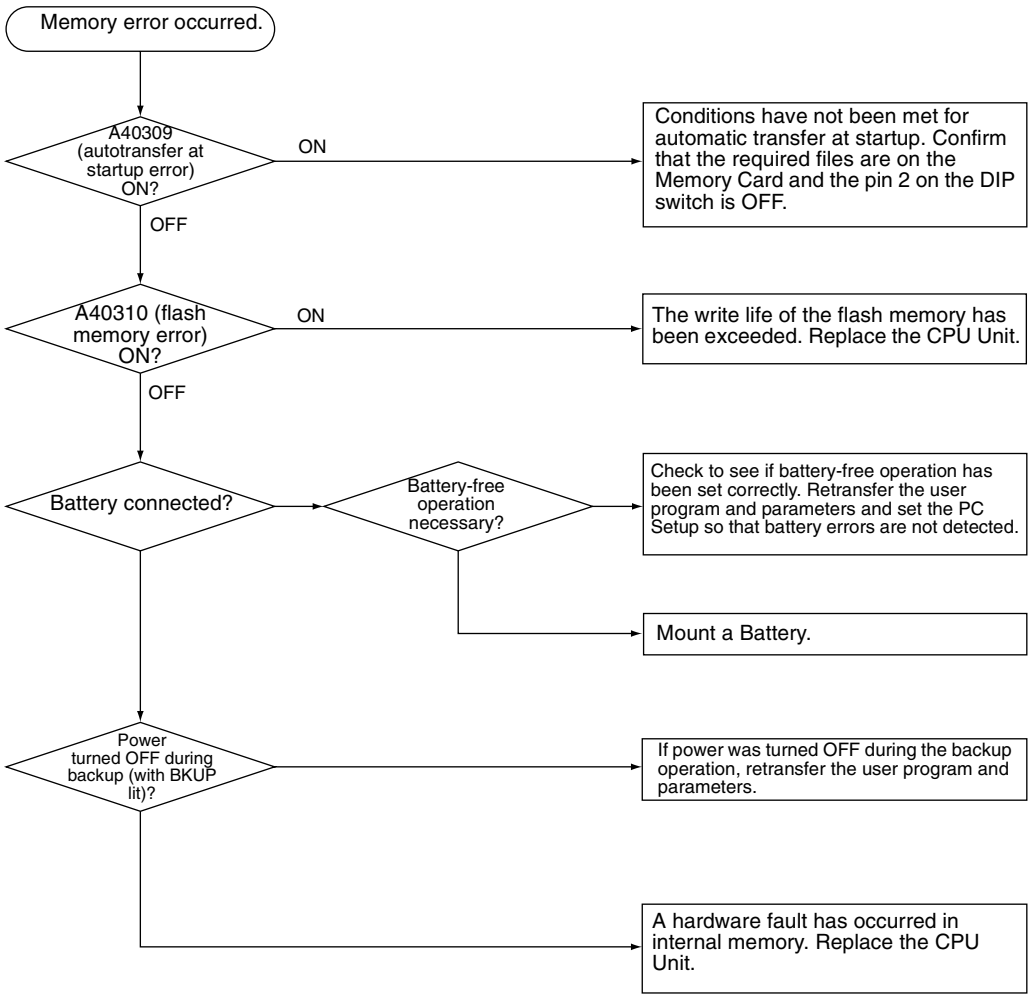
11-2-6 Power Supply Check

The allowable voltage ranges are shown in the following table.

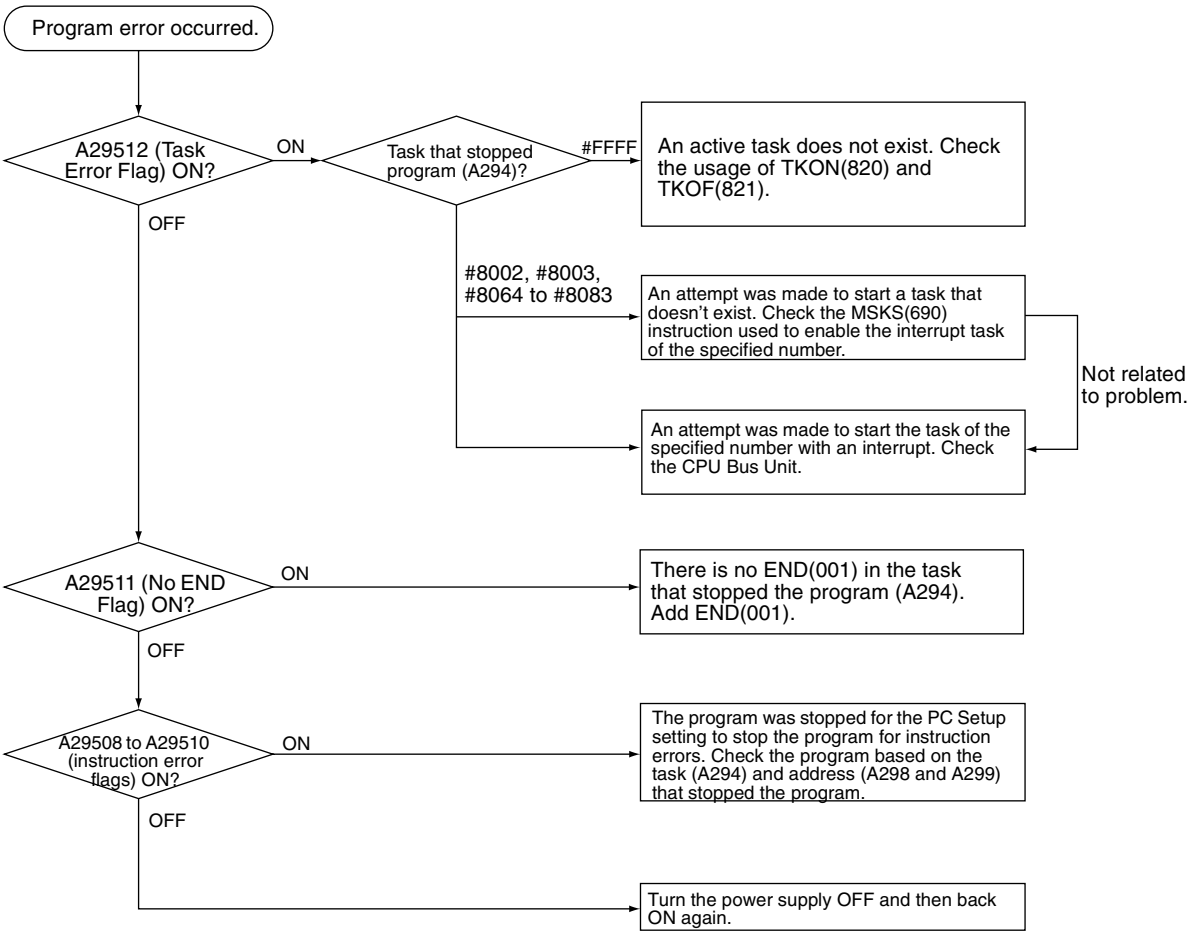
Power Supply Unit	Power supply voltage	Allowable voltage range
CJ1W-PA205R	100 to 240 V AC	85 to 264 V AC
CJ1W-PA202	100 to 240 V AC	85 to 264 V AC
CJ1W-PD025	24 V DC	19.2 to 28.8 V DC



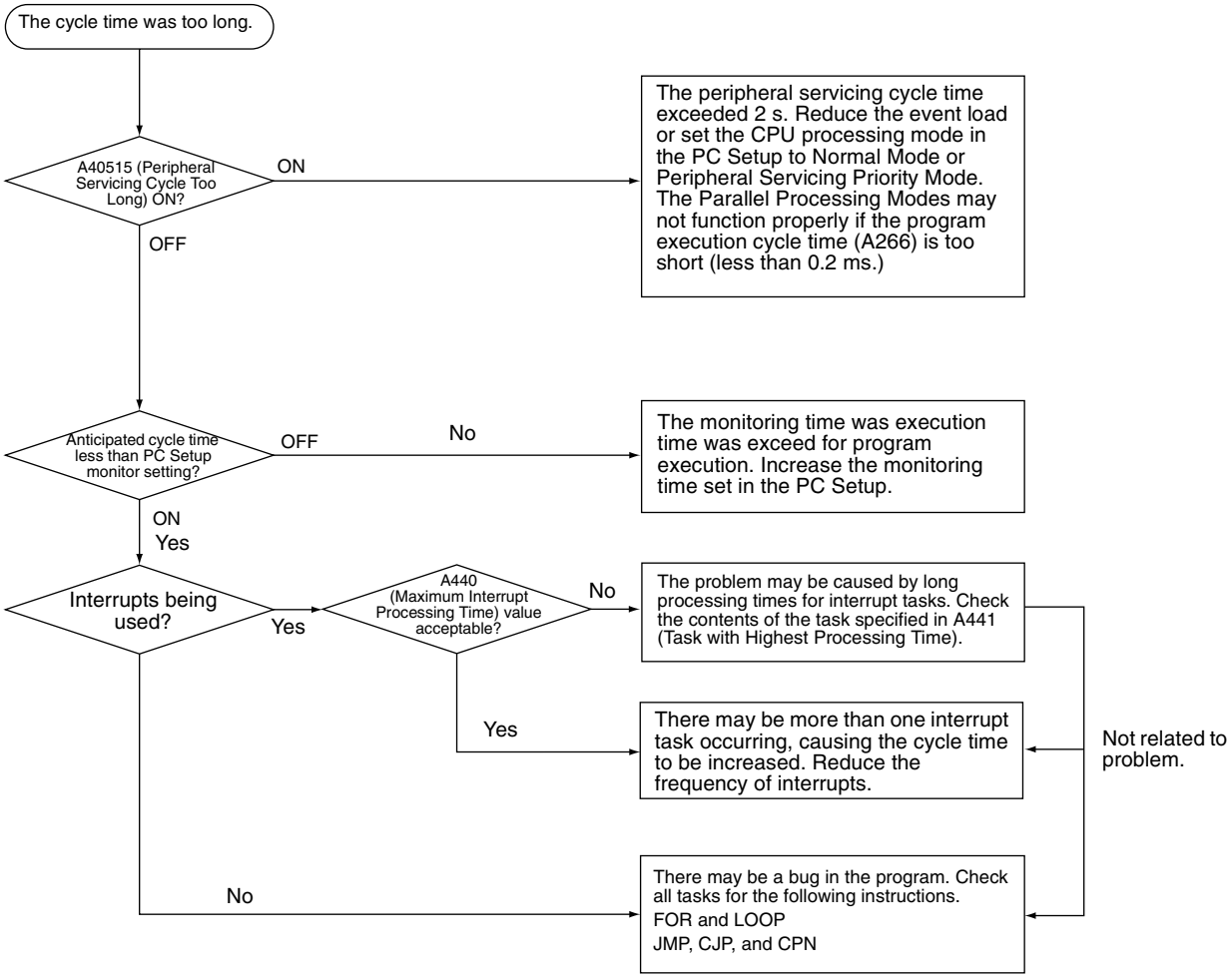
11-2-7 Memory Error Check



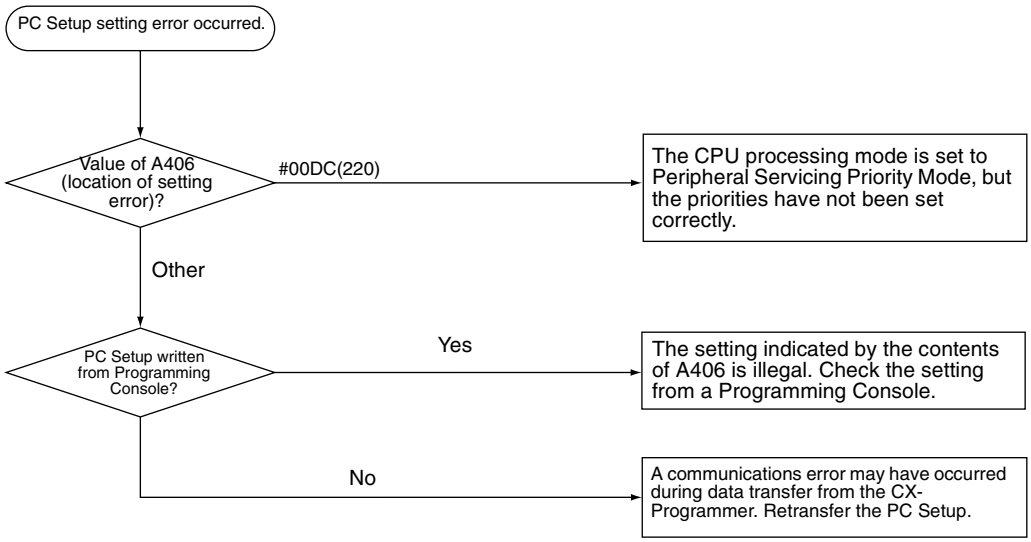
11-2-8 Program Error Check



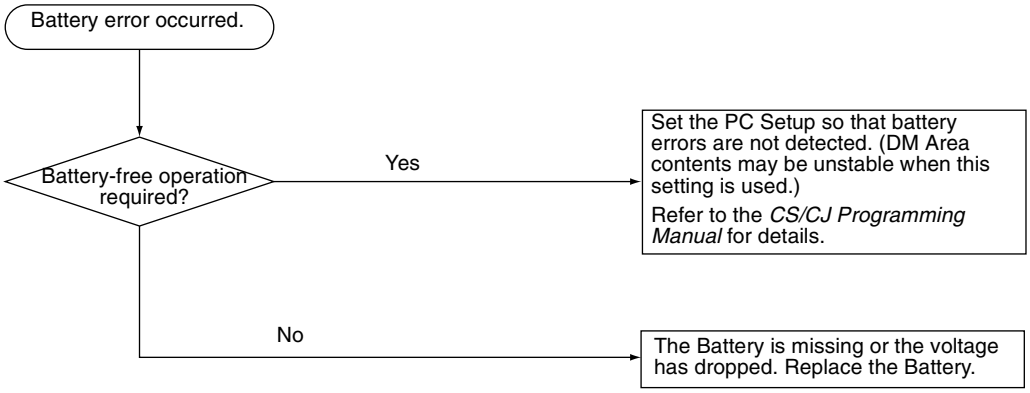
11-2-9 Cycle Time Too Long Error Check



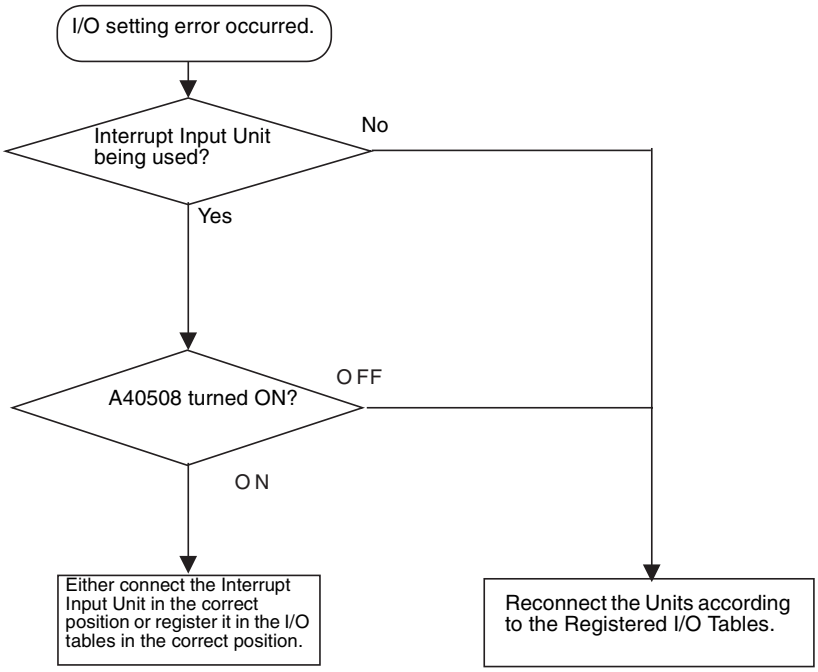
11-2-10 PC Setup Setting Error Check



11-2-11 Battery Error Check

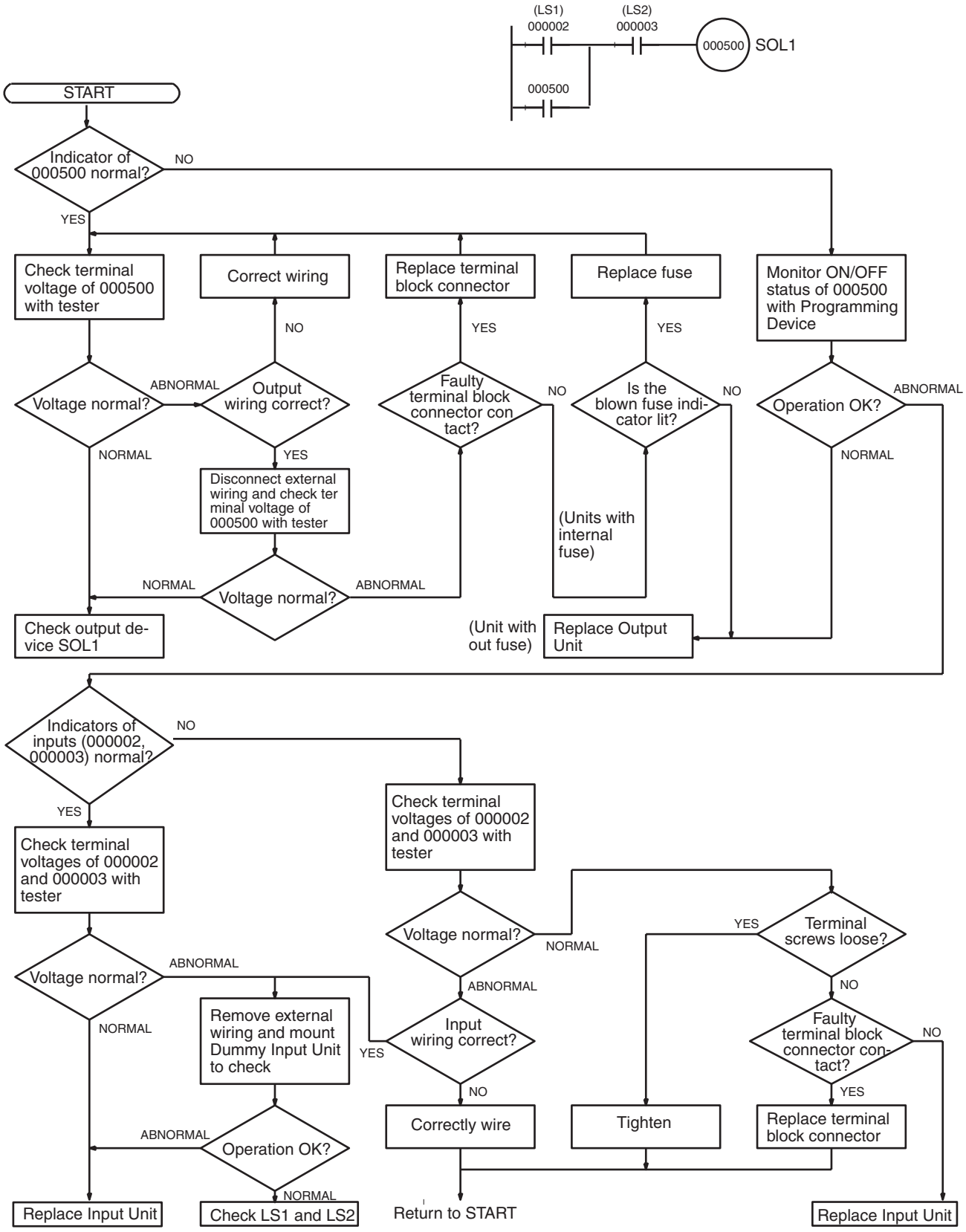


11-2-12 I/O Setting Error Check

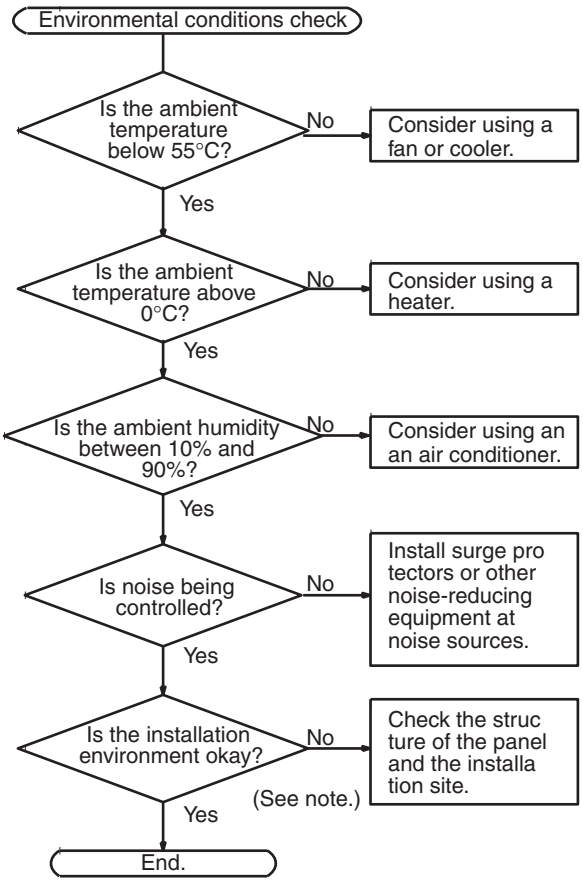


11-2-13 I/O Check

The I/O check flowchart is based on the following ladder diagram section assuming that SOL1 does not turn ON.



11-2-14 Environmental Conditions Check



Note Check for corrosive gases, flammable gases, dust, dirt, salts, metal dust, direct light, water, oils, and chemicals.

11-3 Troubleshooting Racks and Units

CPU Racks and Standard Expansion Racks

Symptom	Cause	Remedy
POWER indicator is not lit.	PCB short-circuited or damaged.	Replace Power Supply Unit.
	(1) Error in program.	Correct program
	(2) Power line is faulty.	Replace Power Supply Unit.
RUN output* does not turn ON. RUN indicator lit. (*CJ1W-PA205R)	Internal circuitry of Power Supply Unit is faulty.	Replace Power Supply Unit.
Serial Communications Unit or CPU Bus Unit does not operate or malfunctions.	(1) The I/O Connecting Cable is faulty. (2) The I/O bus is faulty.	Replace the I/O Connecting Cable Replace the I/O Control Unit or I/O Interface Unit.
Bits do not operate past a certain point.		
Error occurs in units of 8 points.		
I/O bit turns ON		
All bits in one Unit do not turn ON.		

Special I/O Units

Refer to the *Operation Manual* for the Special I/O Unit to troubleshoot any other errors.

Symptom	Cause	Remedy
The ERH and RUN indicators on the Special I/O Unit are lit.	I/O refreshing is not being performed for the Unit from the CPU Unit (CPU Unit monitoring error). It's possible that cyclic refreshing has been disabled for the Special I/O Unit in the Cyclic Refresh Disable Setting in the PC Setup (i.e., the bit corresponding to the unit number has been set to 1).	Change the bit corresponding to the unit number to 0 to enable cyclic refreshing, or make sure that the Unit is refreshed from the program using IORF at least once every 11 s.

CJ Long-distance Expansion Racks

Symptom	Cause	Remedy
CPU Unit won't operate. (No response to Programming Devices and no CPU Unit indicators are lit.)	(1) Power is not turned ON to an Expansion Rack.	Turn ON power to all Expansion Racks.
	(2) An Expansion Rack is not connected correctly.	Recheck the connections and configuration using information in *2-3-2 CJ-series Expansion Racks, 3-5 I/O Control Units and I/O Interface Units.*
	(3) An I/O Connecting Cable is not wired correctly.	Reconnect the I/O Connecting Cables in the correct order for output and input connectors.
	(4) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Power Supply Unit, I/O Units, I/O Control/ Interface Unit, and I/O Connecting Cable.
Expansion Rack not detected.	(1) A Terminator is not connected.	If the TERM indicator is lit, connect a Terminator.
	(2) An Expansion Rack is not connected correctly.	Recheck the connections and configuration using information in *2-3-2 CJ-series Expansion Racks, 3-5 I/O Control Units and I/O Interface Units.*
	(3) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Power Supply Unit, I/O Units, I/O Control/ Interface Unit, and I/O Connecting Cable.
I/O bus error or I/O verification error occurs.	(1) An I/O Connecting Cable or Terminator connection is faulty.	Check that I/O Connecting Cables and Terminators are connected correctly.
	(2) Noise or other external factor.	Separate all cables from possible sources of noise or place them in metal ducts.
	(3) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Power Supply Unit, I/O Units, I/O Control/ Interface Unit, and I/O Connecting Cable.
Cycle time is too long.	(1) A CPU Bus Unit that is allocated many words (e.g., Controller Link Unit) is mounted to a CJ Long-distance Expansion Rack.	Move the CPU Bus Unit to the CPU Rack.
	(2) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Power Supply Unit, I/O Units, I/O Control/ Interface Unit, and I/O Connecting Cable.
I/O Control Unit and I/O Interface Units do not appear on CX-Programmer I/O table.	This is not an error. These Units are not allocated I/O words and thus are not registered in the I/O tables.	---

Input Units

Symptom	Cause	Remedy
Not all inputs turn ON or indicators are not lit.	(1) Power is not supplied to Input Unit.	Supply power
	(2) Supply voltage is low.	Adjust supply voltage to within rated range.
	(3) Terminal block mounting screws are loose.	Tighten screws.
	(4) Faulty contact of terminal block connector.	Replace terminal block connector.
Not all inputs turn ON (indicator lit).	Input circuit is faulty. (There is a short at the load or something else that caused an overcurrent to flow.)	Replace Unit.
Not all inputs turn OFF.	Input circuit is faulty.	Replace Unit.
Specific bit does not turn ON.	(1) Input device is faulty.	Replace input devices.
	(2) Input wiring disconnected.	Check input wiring
	(3) Terminal block screws are loose.	Tighten screws
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
	(5) Too short ON time of external input.	Adjust input device
	(6) Faulty input circuit	Replace Unit.
	(7) Input bit number is used for output instruction.	Correct program.
Specific bit does not turn OFF.	(1) Input circuit is faulty.	Replace Unit.
	(2) Input bit number is used for output instruction.	Correct program.
Input irregularly turns ON/OFF.	(1) External input voltage is low or unstable.	Adjust external input voltage to within rated range.
	(2) Malfunction due to noise.	Take protective measures against noise, such as: (1) Increase input response time (PC Setup) (2) Install surge suppressor. (3) Install insulation transformer. (4) Install shielded cables between the Input Unit and the loads.
	(3) Terminal block screws are loose.	Tighten screws
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
Error occurs in units of 8 points or 16 points, i.e., for the same common.	(1) Common terminal screws are loose.	Tighten screws
	(2) Faulty terminal block connector contact.	Replace terminal block connector.
	(3) Faulty data bus	Replace Unit.
	(4) Faulty CPU	Replace CPU.
Input indicator is not lit in normal operation.	Faulty indicator or indicator circuit.	Replace Unit.

Output Units

Symptom	Cause	Remedy
Not all outputs turn ON	(1) Load is not supplied with power.	Supply power
	(2) Load voltage is low.	Adjust voltage to within rated range.
	(3) Terminal block screws are loose.	Tighten screws
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
	(5) An overcurrent (possibly caused by a short at the load) resulted in a blown fuse in the Output Unit. (Some Output Units provide an indicator for blown fuses.)	Replace fuse or Unit.
	(6) Faulty I/O bus connector contact.	Replace Unit.
	(7) Output circuit is faulty.	Replace Unit.
	(8) If the INH indicator is lit, the Output OFF Bit (A50015) is ON.	Turn A50015 OFF.
Not all outputs turn OFF	Output circuit is faulty.	Replace Unit.
Output of a specific bit number does not turn ON or indicator is not lit	(1) Output ON time too short because of a mistake in programming.	Correct program to increase the time that the output is ON.
	(2) Bit status controlled by multiple instructions.	Correct program so that each output bit is controlled by only one instruction.
	(3) Faulty output circuit.	Replace Unit.
Output of a specific bit number does not turn ON (indicator lit).	(1) Faulty output device.	Replace output device.
	(2) Break in output wiring.	Check output wiring.
	(3) Loose terminal block screws.	Tighten screws.
	(4) Faulty terminal block connector faulty.	Replace terminal block connector.
	(5) Faulty output bit.	Replace relay or Unit.
	(6) Faulty output circuit.	Replace Unit.
Output of a specific bit number does not turn OFF (indicator is not lit).	(1) Faulty output bit.	Replace relay or Unit.
	(2) Bit does not turn OFF due to leakage current or residual voltage.	Replace external load or add dummy resistor.
Output of a specific bit number does not turn OFF (indicator lit).	(1) Bit status controlled by multiple instructions.	Correct program.
	(2) Faulty output circuit.	Replace Unit.
Output irregularly turns ON/OFF.	(1) Low or unstable load voltage.	Adjust load voltage to within rated range
	(2) Bit status controlled by multiple instructions.	Correct program so that each output bit is controlled by only one instruction.
	(3) Malfunction due to noise.	Protective measures against noise: (1) Install surge suppressor. (2) Install insulation transformer. (3) Use shielded cables between the Output Unit and the loads.
	(4) Terminal block screws are loose.	Tighten screws.
	(5) Faulty terminal block connector contact.	Replace terminal block connector.
Error occurs in units of 8 points or 16 points, i.e., for the same common.	(1) Loose common terminal screw.	Tighten screws.
	(2) Faulty terminal block connector contact.	Replace terminal block connector.
	(3) An overcurrent (possibly caused by a short at the load) resulted in a blown fuse in the Output Unit.	Replace fuse or Unit.
	(4) Faulty data bus.	Replace Unit.
	(5) Faulty CPU.	Replace CPU.
Output indicator is not lit (operation is normal).	Faulty indicator.	Replace Unit.

SECTION 12
Inspection and Maintenance

This section provides inspection and maintenance information.

12-1 Inspections

Daily or periodic inspections are required in order to maintain the PC's functions in peak operating condition.

12-1-1 Inspection Points

The major electronic components in CJ-series PCs are semiconductor components, which although have an extremely long life time, can deteriorate under improper environmental conditions. Periodic inspections are thus required to ensure that the required conditions are being kept.

Inspection is recommended at least once every six months to a year, but more frequent inspections will be necessary in adverse environments.

Take immediate steps to correct the situation if any of the conditions in the following table are not met.

No.	Item	Inspection	Criteria	Action
1	Source Power Supply	Check for voltage fluctuations at the power supply terminals.	The voltage must be within the allowable voltage fluctuation range. (See note.)	Use a voltage tester to check the power supply at the terminals. Take necessary steps to bring voltage fluctuations within limits.
2	I/O Power Supply	Check for voltage fluctuations at the I/O terminals.	Voltages must be within specifications for each Unit.	Use a voltage tester to check the power supply at the terminals. Take necessary steps to bring voltage fluctuations within limits.
3	Ambient environment	Check the ambient temperature. (Inside the control panel if the PC is in a control panel.)	0 to 55°C	Use a thermometer to check the temperature and ensure that the ambient temperature remains within the allowed range of 0 to 55°C.
		Check the ambient humidity. (Inside the control panel if the PC is in a control panel.)	Relative humidity must be 10% to 90% with no condensation.	Use a hygrometer to check the humidity and ensure that the ambient humidity remains within the allowed range.
		Check that the PC is not in direct sunlight.	Not in direct sunlight	Protect the PC if necessary.
		Check for accumulation of dirt, dust, salt, metal filings, etc.	No accumulation	Clean and protect the PC if necessary.
		Check for water, oil, or chemical sprays hitting the PC.	No spray on the PC	Clean and protect the PC if necessary.
		Check for corrosive or flammable gases in the area of the PC.	No corrosive or flammable gases	Check by smell or use a sensor.
		Check the level of vibration or shock.	Vibration and shock must be within specifications.	Install cushioning or shock absorbing equipment if necessary.
		Check for noise sources near the PC.	No significant noise sources	Either separate the PC and noise source or protect the PC.

No.	Item	Inspection	Criteria	Action
4	Installation and wiring	Check that each Unit is connected and locked to the next Unit securely.	No looseness	Press the connectors together completely and lock them with the sliders.
		Check that cable connectors are fully inserted and locked.	No looseness	Correct any improperly installed connectors.
		Check for loose screws in external wiring.	No looseness	Tighten loose screws with a Phillips-head screwdriver.
		Check crimp connectors in external wiring.	Adequate spacing between connectors	Check visually and adjust if necessary.
		Check for damaged external wiring cables.	No damage	Check visually and replace cables if necessary.
5	User-serviceable parts	Check whether the CJ1W-BAT01 Battery has reached its service life.	Life expectancy is 5 years at 25°C, less at higher temperatures. (From 0.75 to 5 years depending on model, power supply rate, and ambient temperature.)	Replace the battery when its service life has passed even if a battery error has not occurred. (Battery life depends upon the model, the percentage of time in service, and ambient conditions.)

Note The following table shows the allowable voltage fluctuation ranges for source power supplies.

Supply voltage	Allowable voltage range
100 to 240 V AC	85 to 264 V AC
24 V DC	19.2 to 28.8 V DC

Tools Required for Inspections

Required Tools

- Slotted and Phillips-head screwdrivers
- Voltage tester or digital voltmeter
- Industrial alcohol and clean cotton cloth

Tools Required Occasionally

- Synchroscope
- Oscilloscope with pen plotter
- Thermometer and hygrometer (humidity meter)

12-1-2 Unit Replacement Precautions

Check the following after replacing any faulty Unit.

- Do not replace a Unit until the power is turned OFF.
- Check the new Unit to make sure that there are no errors.
- If a faulty Unit is being returned for repair, describe the problem in as much detail as possible, enclose this description with the Unit, and return the Unit to your OMRON representative.
- For poor contact, take a clean cotton cloth, soak the cloth in industrial alcohol, and carefully wipe the contacts clean. Be sure to remove any lint prior to remounting the Unit.

Note 1. When replacing a CPU Unit, be sure that not only the user program but also all other data required for operation is transferred to or set in the new CPU Unit before starting operation, including DM Area and HR Area settings. If data area and other data are not correct for the user program, unexpected accidents may occur. Be sure to include the routing tables, Controller Link Unit data link tables, network parameters, and other CPU

Bus Unit data, which are stored as parameters in the CPU Unit. Refer to the CPU Bus Unit and Special I/O Unit operation manuals for details on the data required by each Unit.

2. The simple backup operation can be used to store the user program and all parameters for the CJ1-H CPU Unit, DeviceNet Units, Serial Communications Units, and other specific Units in a Memory Card as backup files. A Memory Card and the simple backup operation can be used to easily restore data after replacing any of these Units. Refer to the *CS/CJ Series Programming Manual* (W394) for details.

12-2 Replacing User-serviceable Parts

The following parts should be replaced periodically as preventative maintenance. The procedures for replacing these parts are described later in this section.

- Battery (the CPU Unit's RAM-backup battery)

Battery Functions

The battery retains the following data of the CPU Unit's RAM when the main power supply is OFF.

- The user program
- The PC Setup
- Retained regions of I/O memory (such as the Holding Area and DM Area)

If the battery is not installed or battery voltage drops too low, the data in RAM will be lost when the main power supply goes OFF.

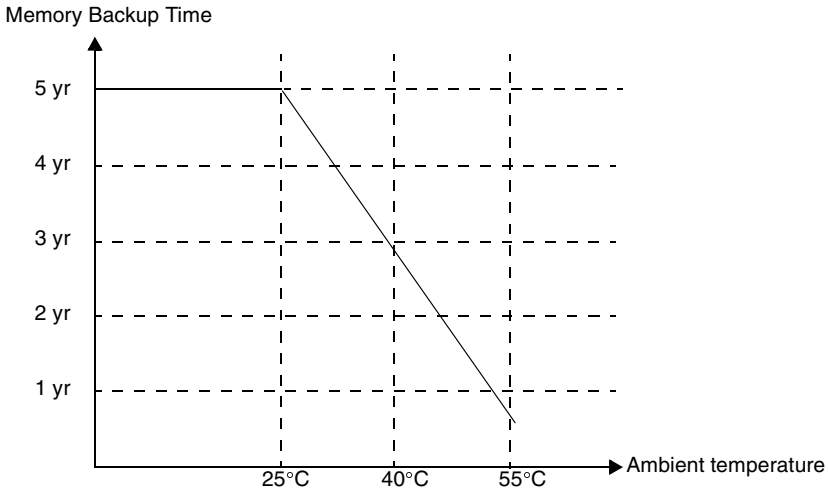
Battery Service Life and Replacement Period

At 25°C, the maximum service life for batteries is 5 years whether or not power is supplied to the CPU Unit while the battery is installed. The battery's lifetime will be shorter when it is used at higher temperatures and when power is not supplied to the CPU Unit for long periods. In the worst case conditions, the battery will last for only 0.75 years.

The following table shows minimum lifetimes and typical lifetimes for the backup battery (total time with power not supplied).

Model	Maximum lifetime	Minimum lifetime (See note.)	Typical lifetime (See note.)
CJ1G-CPU□□	5 years	6,500 hours (0.75 years)	43,000 hours (5 years)

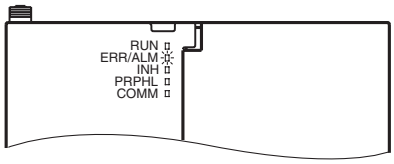
Note The minimum lifetime is the memory backup time at an ambient temperature of 55°C. The typical lifetime is the memory backup time at an ambient temperature of 25°C.



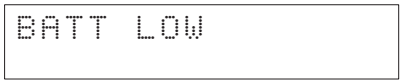
This graphic is for reference only.

Low Battery Indicators

If the PC Setup has been set to detect a low-battery error, the ERR/ALM indicator on the front of the CPU Unit will flash when the battery is nearly discharged.



When the ERR/ALM indicator flashes, connect a Programming Console to the peripheral port and read the error message. If the message “BATT LOW” appears on the Programming Console* and the Battery Error Flag (A40204) is ON*, first check whether the battery is properly connected to the CPU Unit. If the battery is properly connected, replace the battery as soon as possible.



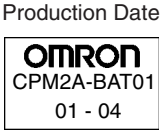
Once a low-battery error has been detected, it will take 5 days before the battery fails assuming that power has been supplied at lease once a day. Battery failure and the resulting loss of data in RAM can be delayed by ensuring that the CPU Unit power is not turned OFF until the battery has been replaced.

Note

1. *The PC Setup must be set to detect a low-battery error (Detect Low Battery). If this setting has not been made, the BATT LOW error message will not appear on the Programming Console and the Battery Error Flag (A40204) will not go ON when the battery fails.
2. The battery will discharge faster at higher temperatures, e.g., 4 days at 40°C and 2 days at 55°C.

Replacement Battery

Use the CPM2A-BAT01 Battery Set. Be sure to install a replacement battery within 2 years of the production date shown on the battery's label.



Replacement Procedure

Use the following procedure to replace the battery when the previous battery has become completely discharged. You must complete this procedure within five minutes after turning OFF the power to the CPU Unit to ensure memory backup.

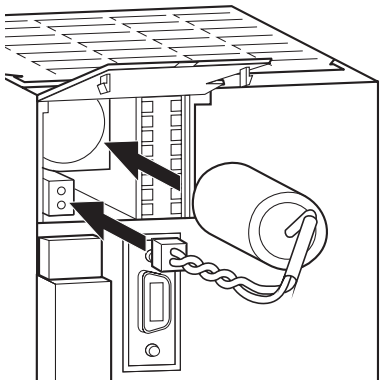
1,2,3...

1. Turn OFF the power to the CPU Unit.

or If the CPU Unit has not been ON, turn it ON for at least five minutes and then turn it OFF.

Note If power is not turned ON for at least five minutes before replacing the battery, the capacitor that backs up memory when the battery is removed will not be fully charged and memory may be lost before the new battery is inserted.

2. Open the compartment on the upper left of the CPU Unit and carefully draw out the battery.
3. Remove the battery connector.
4. Connect the new battery, place it into the compartment, and close the cover.



The battery error will automatically be cleared when a new battery is inserted.

⚠WARNING Never short-circuit the battery terminals; never charge the battery; never disassemble the battery; and never heat or incinerate the battery. Doing any of these may cause the battery to leak, burn, or rupturing resulting in injury, fire, and possible loss of life or property. Also, never use a battery that has been dropped on the floor or otherwise subject to shock. It may leak.

UL standards require that batteries be replaced by experienced technicians. Always place an experienced technician in charge or battery replacement.

Appendix A
Specifications of Basic I/O Units

Basic Input Units

Name	Specifications	Model	Number of input bits allocated	Page
DC Input Units	Terminal block, 24 V DC, 16 inputs	CJ1W-ID211	16	358
	Fujitsu-compatible connector,	CJ1W-ID231	32	359
	MIL connector, 24 V DC	CJ1W-ID232	32	361
	Fujitsu-compatible connector, 24 V DC	CJ1W-ID261	64	363
	MIL connector, 24 V DC	CJ1W-ID262	64	364
AC Input Units	Terminal block, 200 to 240 VDC	CJ1W-IA201	8	366
	Terminal block, 100 to 120 VDC	CJ1W-IA111	16	367
Interrupt Input Unit	Terminal block, 24 VDC	CJ1W-INT01	16	368

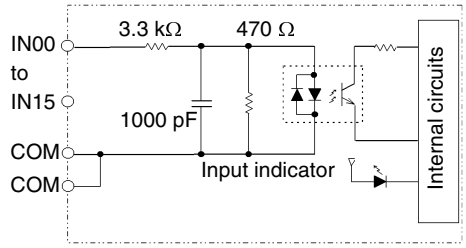
Basic Output Units

Name		Specifications	Model	Number of bits allocated	Page
Relay Output Units		Terminal block, 250 V AC/24 V DC, 2 A, independent contacts	CJ1W-OC201	8	369
		Terminal block, 250 V AC/24 V DC, 2 A	CJ1W-OC211	16	370
Triac Output Unit		Terminal block, 250 V AC, 0.6 A/24 V DC,	CJ1W-OA201	8	371
Transistor Output Units	Sinking outputs	Terminal block, 12 to 24 V DC, 2 A, 8 outputs	CJ1W-OD201	8	372
		Terminal block, 12 to 24 V DC, 0.5 A	CJ1W-OD211	16	373
		Fujitsu-compatible connector, 12 to 24 V DC, 0.5 A	CJ1W-OD231	32	374
		MIL connector, 12 to 24 V DC, 0.5 A	CJ1W-OD233	32	376
		Fujitsu-compatible connector, 12 to 24 V DC, 0.3 A	CJ1W-OD261	64	377
		MIL connector, 12 to 24 V DC, 0.3 A	CJ1W-OD263	64	378
	Sourcing outputs	Terminal block, 24 V DC, 2 A, load short-circuit protection, line disconnection detection	CJ1W-OD202	8	380
		Terminal block, 24 V DC, 0.5 A, load short-circuit protection	CJ1W-OD212	16	378
		MIL connector, 24 V DC, 0.5 A, load short-circuit protection	CJ1W-OD232	32	382

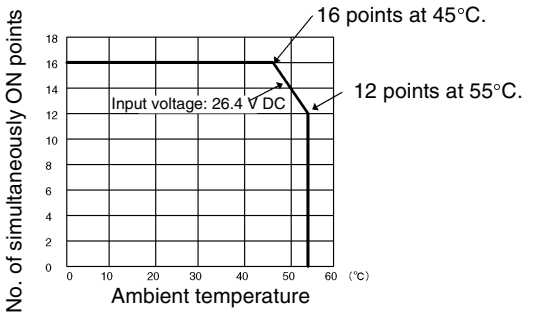
CJ1W-ID211 24-V DC Input Unit (Terminal Block, 16 Points)

Rated Input Voltage	24 V DC $^{+10\%}/_{-15\%}$
Input Impedance	3.3 kΩ
Input Current	7 mA typical (at 24 V DC)
ON Voltage/ON Current	14.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Possible to set to between 0 and 32 ms in the PC Setup.)
OFF Response Time	8.0 ms max. (Possible to set to between 0 and 32 ms using PC)
No. of Circuits	16 (16 points/common, 1 circuit)
Number of Simultaneously ON Points	100% simultaneously ON (at 24 V DC) (Refer to the following illustration.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	80 mA max.
Weight	110 g max.

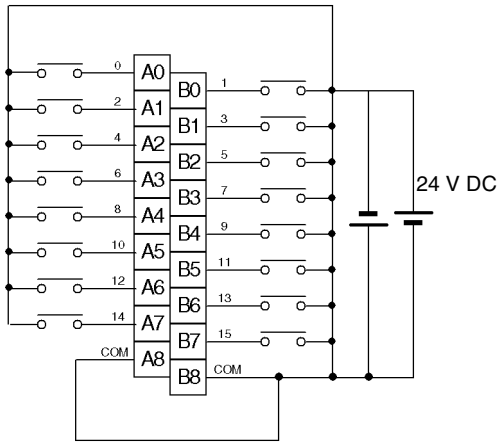
Circuit Configuration



Temperature characteristics for simultaneously ON points



Terminal Connections



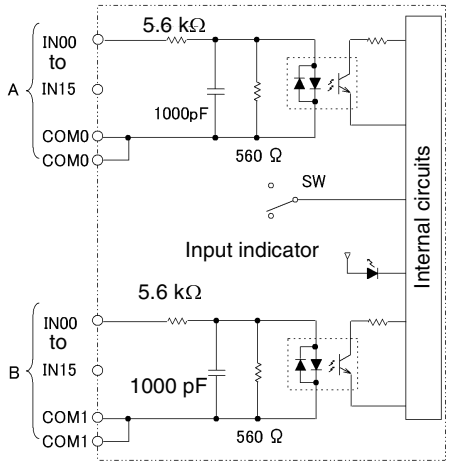
Polarity of the input power supply can connected in either direction.

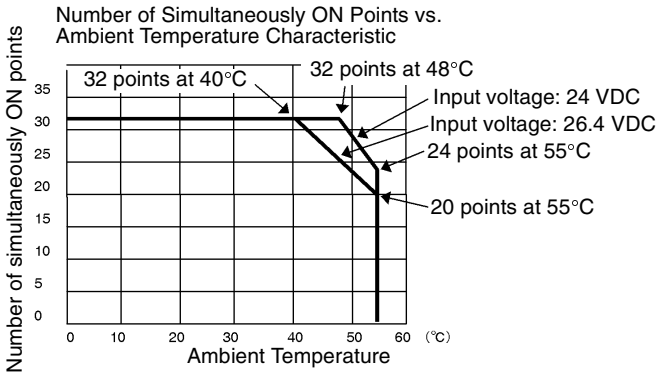
Note The ON response time will be 20 μs maximum and OFF response time will be 400 μs maximum even if the response times are set to 0 ms due to internal element delays.

CJ1W-ID231 DC Input Unit (Fujitsu Connector, 32 Points)

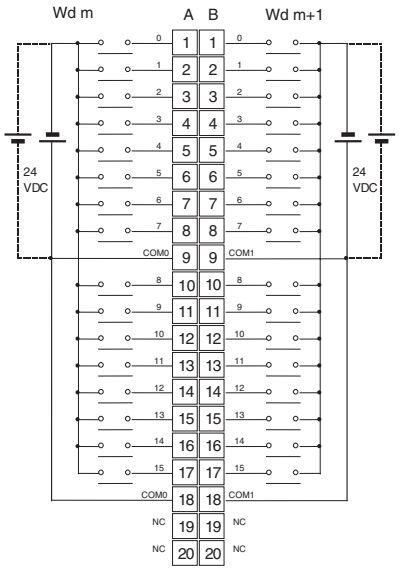
Rated Input Voltage	24 V DC $^{+10\%}/_{-15\%}$
Input Impedance	5.6 kΩ
Input Current	4.1 mA typical (at 24 V DC)
ON Voltage/ON Current	19.0 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup)
No. of Circuits	32 (16 points/common, 2 circuits)
Number of Simultaneously ON Points	75% (12 points/common) (at 24 V DC) (Refer to the following illustration.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA max.
Weight	70 g max.
Accessories	None

Circuit Configuration





Terminal Connections



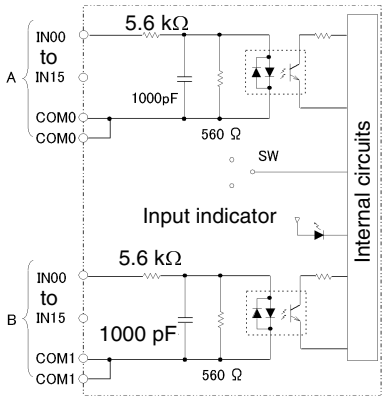
- The input power polarity can be connected in either direction provided that the same polarity is set for rows A and B.
- Both COM0 and COM1 have two pins each. Although they are internally connected, wire all points completely.

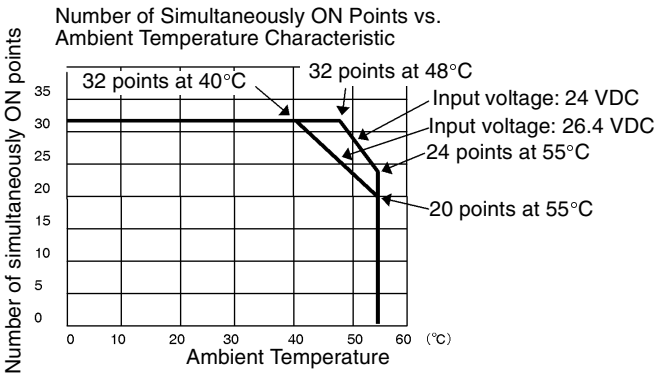
Note The ON response time will be 20 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

CJ1W-ID232 DC Input Unit (MIL Connector, 32 Points)

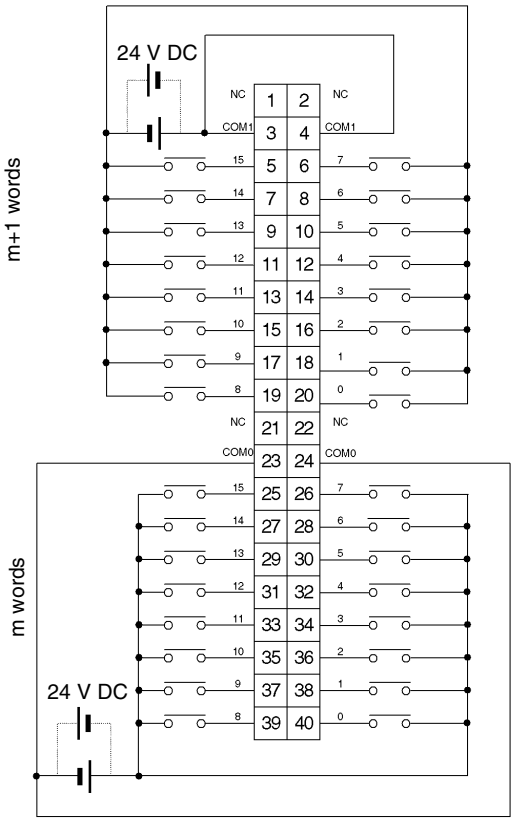
Rated Input Voltage	24 V DC $^{+10\%}/_{-15\%}$
Input Impedance	5.6 kΩ
Input Current	4.1 mA typical (at 24 V DC)
ON Voltage/ON Current	19.0 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup)
No. of Circuits	32 (16 points/common, 2 circuits)
Number of Simultaneously ON Points	75% (12 points/common) (at 24 V DC) (Refer to the following illustration.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA max.
Weight	70 g max.
Accessories	None

Circuit Configuration





Terminal Connections



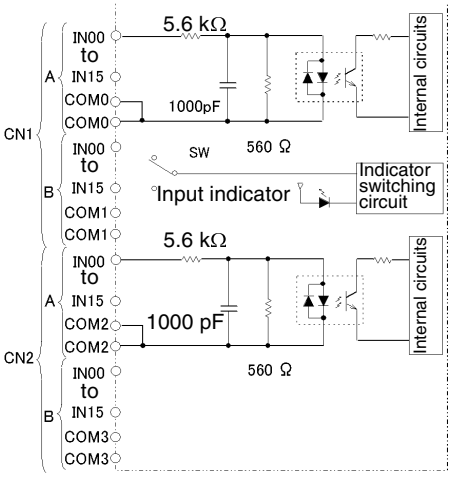
- The input power polarity can be connected in either direction.
- Both COM0 and COM1 have two pins each. Although they are internally connected, wire all points completely.

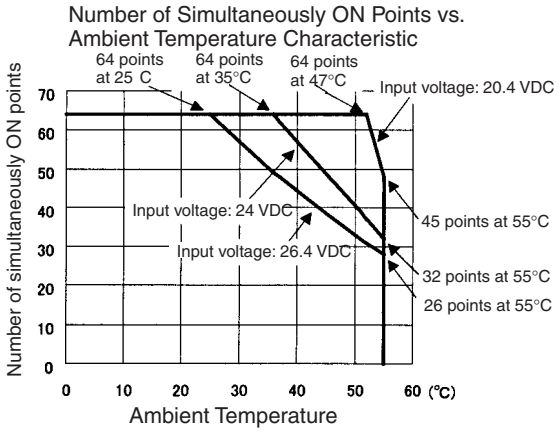
Note The ON response time will be 20 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

CJ1W-ID261 DC Input Unit (Fujitsu Connectors, 64 Points)

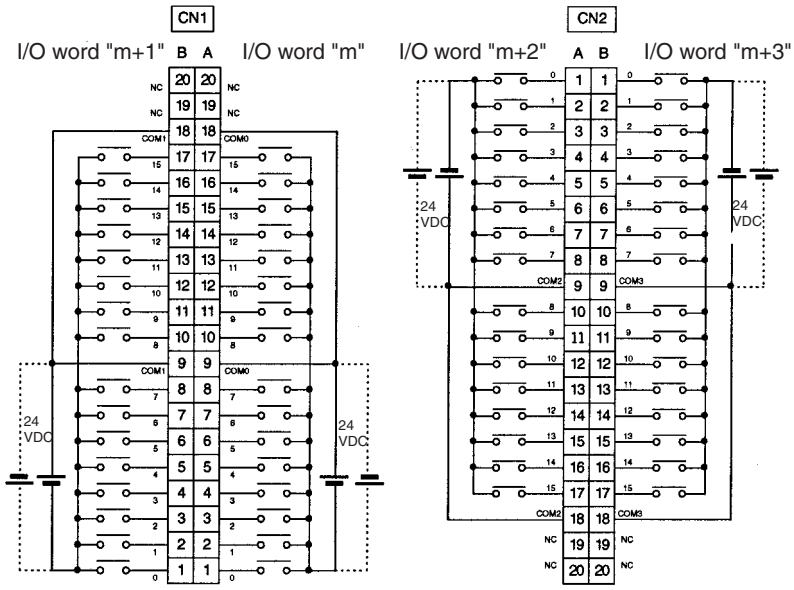
Rated Input Voltage	24 V DC $^{+10\%}/_{-15\%}$
Input Impedance	5.6 kΩ
Input Current	4.1 mA typical (at 24 V DC)
ON Voltage/ON Current	19.0 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
No. of Circuits	64 (16 points/common, 4 circuits)
Number of Simultaneously ON Points	50% (16 points/common) (at 24 V DC) (Refer to the following illustrations.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA max.
Weight	110 g max.
Accessories	None

Circuit Configuration





Terminal Connections



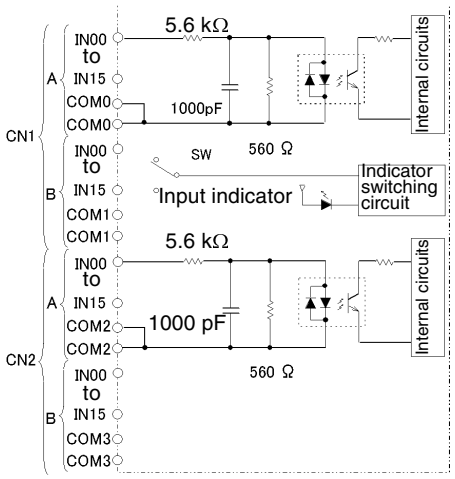
- The input power polarity can be connected in either direction provided that the same polarity be set for rows A and B.
- COM0, COM1, COM2, and COM3 have two pins each. Although they are internally connected, wire all points completely.

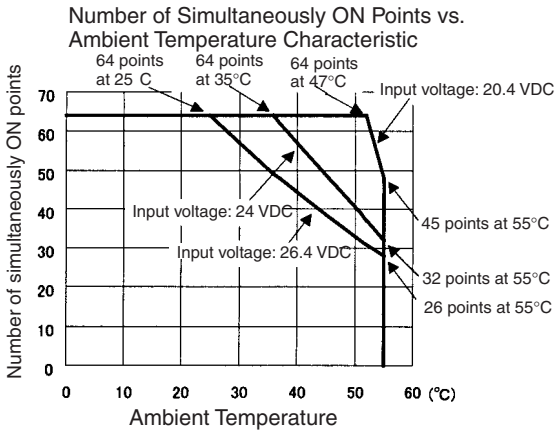
Note The ON response time will be 20 μs maximum and OFF response time will be 400 μs maximum even if the response times are set to 0 ms due to internal element delays.

CJ1W-ID262 DC Input Unit (MIL Connectors, 64 Points)

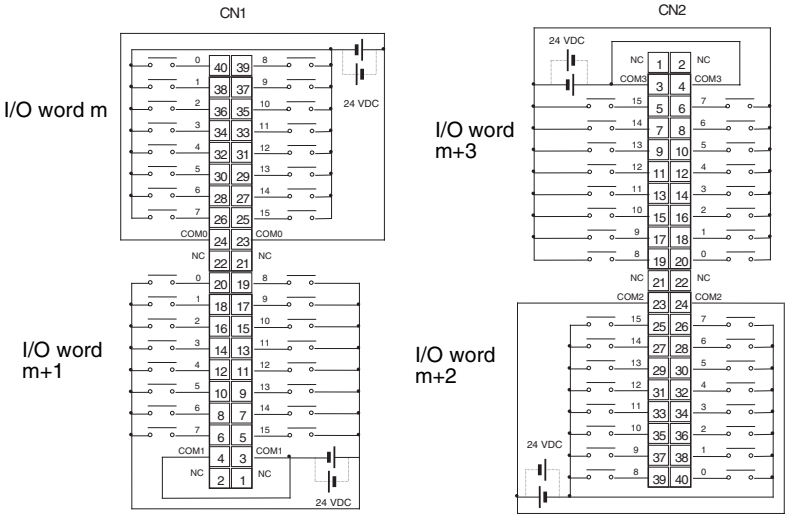
Rated Input Voltage	24 V DC $^{+10\%}/_{-15\%}$
Input Impedance	5.6 kΩ
Input Current	4.1 mA typical (at 24 V DC)
ON Voltage/ON Current	19.0 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PC Setup.)
No. of Circuits	64 (16 points/common, 4 circuits)
Number of Simultaneously ON Points	50% (8 points/common) (at 24 V DC) (Refer to the following illustrations.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA max.
Weight	110 g max.
Accessories	None

Circuit Configuration





Terminal Connections



- The input power polarity can be connected in either direction provided that the same polarity be set for rows A and B.
- COM0, COM1, COM2, and COM3 have two pins each. Although they are internally connected, wire all points completely.

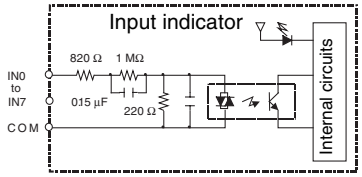
Note The ON response time will be 20 μs maximum and OFF response time will be 400 μs maximum even if the response times are set to 0 ms due to internal element delays.

CJ1W-IA201 DC Input Unit (Terminal Block, 8 Points)

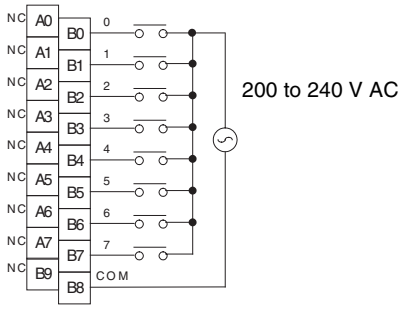
Rated Input Voltage	200 to 240 V AC $^{+10\%}/_{-15\%}$ 50/60 Hz
Input Impedance	21 kΩ (50 Hz), 18 kΩ (60 Hz)
Input Current	9 mA typical (at 200 V AC, 50 Hz), 11 mA typical (at 200 V AC, 60 Hz)
ON Voltage/ON Current	120 V AC min./4 mA min.
OFF Voltage/OFF Current	40 V AC max./2 mA max.
ON Response Time	18.0 ms max. (PC Setup default setting: 8 ms) (See note.)
OFF Response Time	48.0 ms max. (PC Setup default setting: 8 ms) (See note.)
No. of Circuits	8 (8 points/common)
Number of Simultaneously ON Points	100% (8 points/common)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	80 mA max.
Weight	130 g max.
Accessories	None

Note The Input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PC Setup. When the response times have been set to 0 ms, the ON response time will be 10 ms maximum and the OFF response time will be 40 ms maximum due to internal element delays.

Circuit Configuration



Terminal Connections

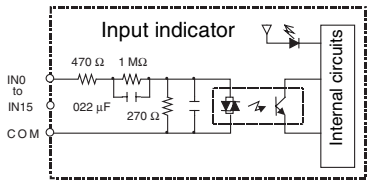


CJ1W-IA111 100 VAC Input Unit (16 points)

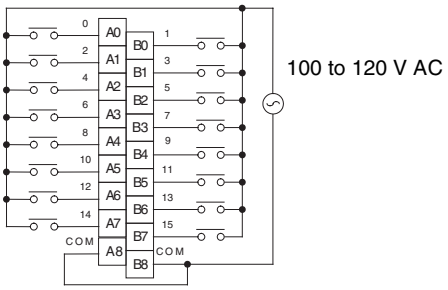
Rated input voltage	100 to 120 VAC $^{+10\%}/_{-15\%}$ 50/60 Hz
Input Impedance	14.5 kΩ (50 Hz), 12 kΩ (60 Hz)
Input Current	7 mA typical (at 100 VAC, 50 Hz), 8 mA typical (at 100 V AC, 60 Hz)
ON Voltage	70 V AC min./4 mA min
OFF Voltage	20 V AC max./2 mA min
ON Response Time	18 ms max. (PC Setup default setting: 8 ms) (See note.)
OFF Response Time	63 ms max. (PC Setup default setting: 8 ms) (See note.)
No. of Circuits	16 (16 points/common)
Number of Inputs ON Simultaneously	100% simultaneously ON (16 points/common)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 VDC)
Dielectric Strength	2,000 VAC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA max.
Weight	130 g max.

Note The Input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PC Setup. When the response times have been set to 0 ms, the ON response time will be 10 ms maximum and the OFF response time will be 40 ms maximum due to internal element delays.

Circuit Layout



Terminal Connections

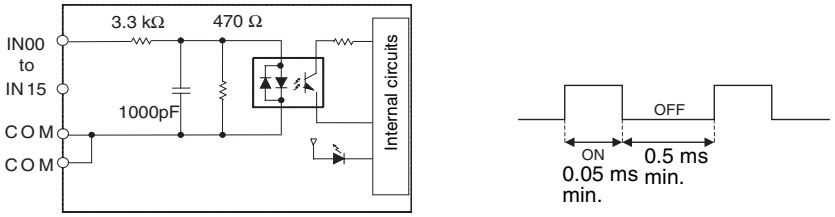


Note Use an input voltage of 90 V AC or less when connecting 2-wire sensors.

CJ1W-INT01 Interrupt Input Unit (16 Points)

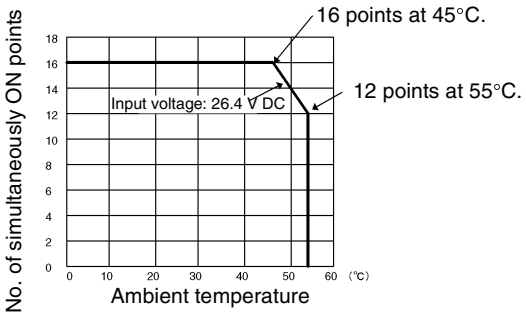
Rated Input Voltage	24 VDC $^{+10\%}/_{-15\%}$
Input Impedance	3.3 kΩ
Input Current	7 mA typical (at 24 VDC)
ON Voltage/ON Current	14.4 VDC min./3 mA min.
OFF Voltage/OFF Current	5 VDC max./1 mA max.
ON Response Time	0.05 ms max.
OFF Response Time	0.5 ms max.
No. of Circuits	16 (16 points/common)
Number of Simultaneously ON Points	100% simultaneously ON (24 V DC)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 VDC)
Dielectric Strength	1,000 VAC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	80 mA max.
Weight	110 g max.

Circuit Configuration

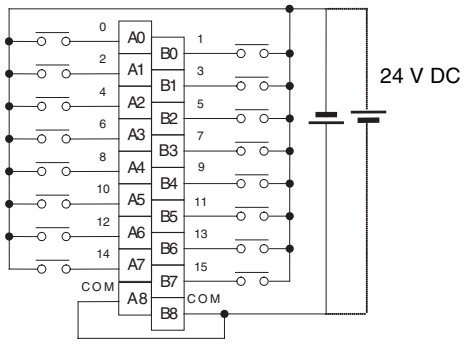


- Up to two Interrupt Input Units can be mounted to the CPU Rack, but they must be connected as one the five Unit immediately next to the CPU Unit. If an Interrupt Input Unit is connected in any other position, an I/O setting error will occur.
- Interrupts cannot be used when an Interrupt Input Unit is mounted to an Expansion Rack.
- Set the pulse width of signals input to the Interrupt Input Unit so they satisfy the above conditions.

Temperature characteristics for simultaneously ON points



Terminal Connections

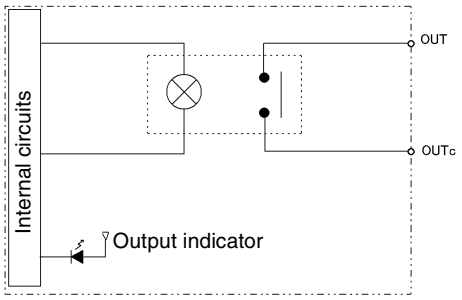


The polarity can be connected in either direction.

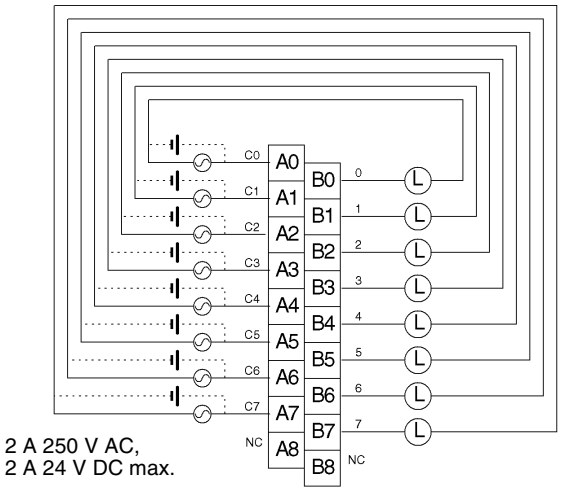
CJ1W-OC201 Contact Output Unit (Terminal Block, 8 Points)

Max. Switching Capacity	2 A 250 V AC ($\cos\phi$ = 1), 2 A 250 V AC ($\cos\phi$ = 0.4), 2 A 24 V DC (16 A/Unit)
Min. Switching Capacity	1 mA 5 V DC
Service Life of Relay	Electrical: 150,000 operations (24 V DC, resistive load)/ 100,000 operations (240 V AC, $\cos\phi$ = 0.4, inductive load) Mechanical: 20,000,000 operations Service life will vary depending on the connected load. Refer to page 386 for information on service life according to the load.
Relay replacement	NY-24W-K-IE (Fujitsu Takamizawa Component Ltd.) Relays cannot be replaced by users.
ON Response Time	15 ms max.
OFF Response Time	15 ms max.
No. of Circuits	8 independent contacts
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	90 mA 5 V DC max. 48 mA 24 V DC (6 mA × No. points ON)
Weight	140 g max.

Circuit Configuration



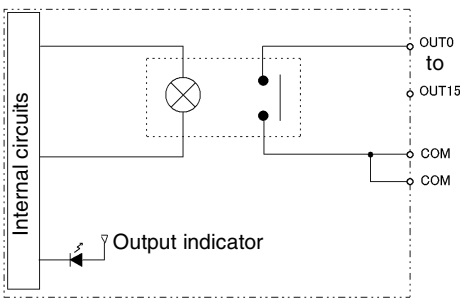
Terminal Connections



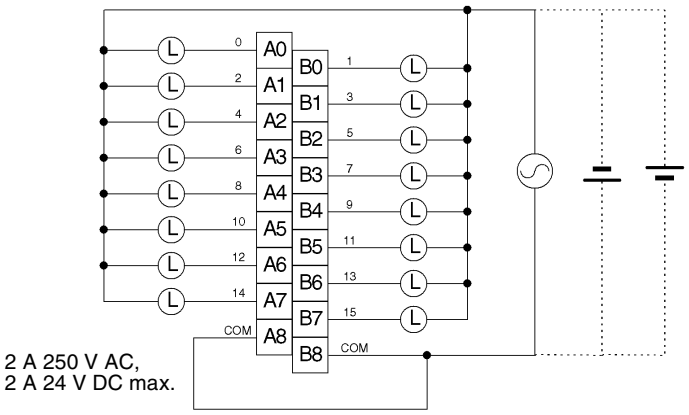
CJ1W-OC211 Contact Output Unit (Terminal Block, 16 Points)

Max. Switching Capacity	2 A 250 V AC (cosϕ = 1), 2 A 250 V AC (cosϕ = 0.4), 2 A 24 V DC (8 A/Unit)
Min. Switching Capacity	1 mA 5 V DC
Service Life of Relay	Electrical: 150,000 operations (24 V DC, resistive load)/ 100,000 operations (250 V AC, cosϕ = 0.4, inductive load) Mechanical: 20,000,000 operations Service life will vary depending on the connected load. Refer to page 386 for information on service life according to the load.
Relay replacement	NY-24W-K-IE (Fujitsu Takamizawa Component Ltd.) Relays cannot be replaced by users.
ON Response Time	15 ms max.
OFF Response Time	15 ms max.
No. of Circuits	16 points/common, 1 circuit
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	110 mA 5 V DC max. 96 mA 24 V DC (6 mA × No. points ON)
Weight	170 g max.

Circuit Configuration



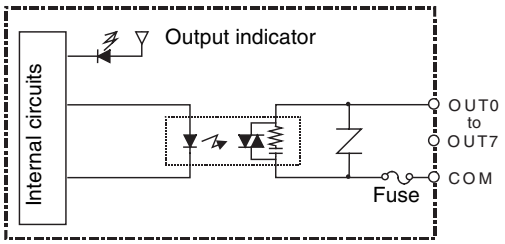
Terminal Connections



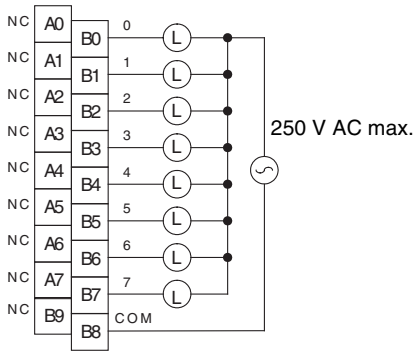
CJ1W-OA201 Triac Output Unit (8 Points)

Max. Switching Capacity	0.6 A 250 VAC, 50/60 Hz (2.4 A/Unit)
Max. Inrush Current	15 A (pulse width: 10 ms)
Min. Switching Capacity	50 mA 75 V AC
Leakage Current	1.5 mA (200 V AC) max.,
Residual Voltage	1.6 VAC max.
ON Response Time	1 ms max.
OFF Response Time	1/2 of load frequency+1 ms or less.
No. of Circuits	1 (8 points/common)
Surge Protector	C.R Absorber + Surge Absorber
Fuses	5 A (1/common, 1 used) The fuse cannot be replaced by the user.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 VDC)
Dielectric Strength	2,000 VAC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	220 mA max.
Weight	150 g max.

Circuit Configuration



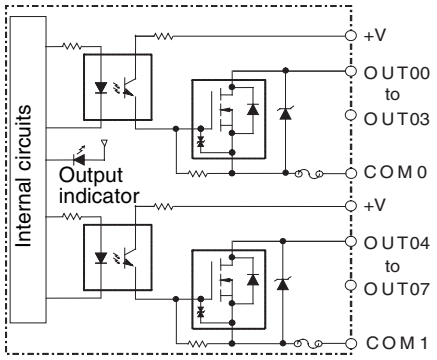
Terminal Connections



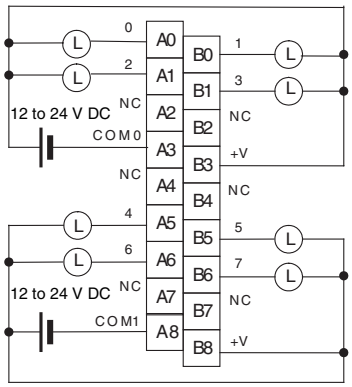
CJ1W-OD201 Transistor Output Unit (Terminal Block, 8 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	2.0 A/point, 8.0 A/Unit
Maximum Inrush Current	10 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	8 (4 points/common, 2 circuits)
Internal Current Consumption	90 mA max.
Fuse	6.3 A (1/common, 2 used) The fuse cannot be replaced by the user.
External Power Supply	12 to 24 V DC, 10 mA min.
Weight	110 g max.

Circuit Configuration



Terminal Connections

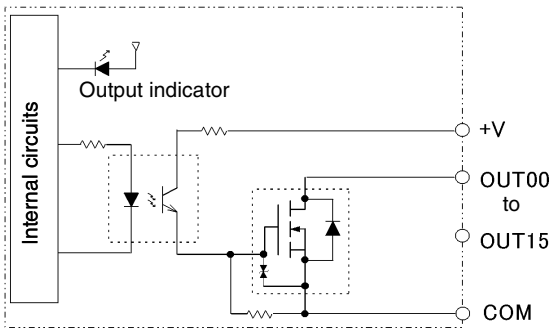


When wiring, pay careful attention to the polarity. The load may operate incorrectly if the polarity is reversed.

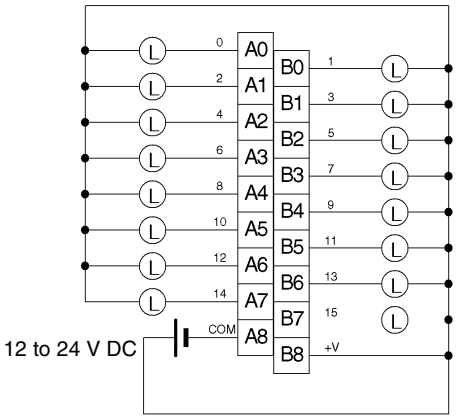
CJ1W-OD211 Transistor Output Unit (Terminal Block, 16 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.5 A/point, 5.0 A/Unit
Maximum Inrush Current	4.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.1 ms max.
OFF Response Time	0.8 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	16 (16 points/common, 2 circuits)
Internal Current Consumption	5 V DC 100 mA max.
Fuse	None
External Power Supply	10.2 to 26.4 V DC, 20 mA min.
Weight	110 g max.

Circuit Configuration



Terminal Connections



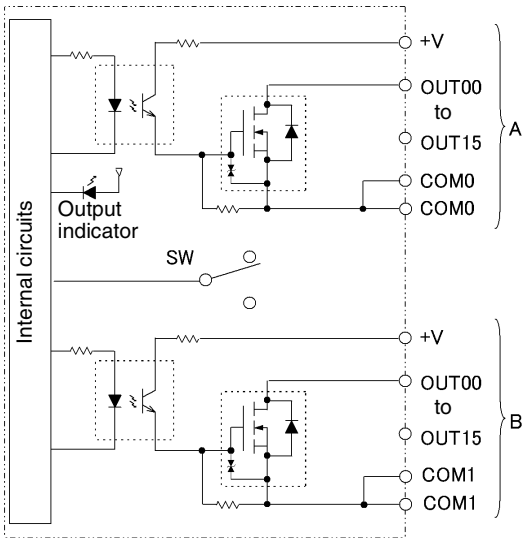
When wiring, pay careful attention to the polarity. The load may operate incorrectly if the polarity is reversed.

CJ1W-OD231 Transistor Output Unit (Fujitsu Connector, 32 Points, Sinking)

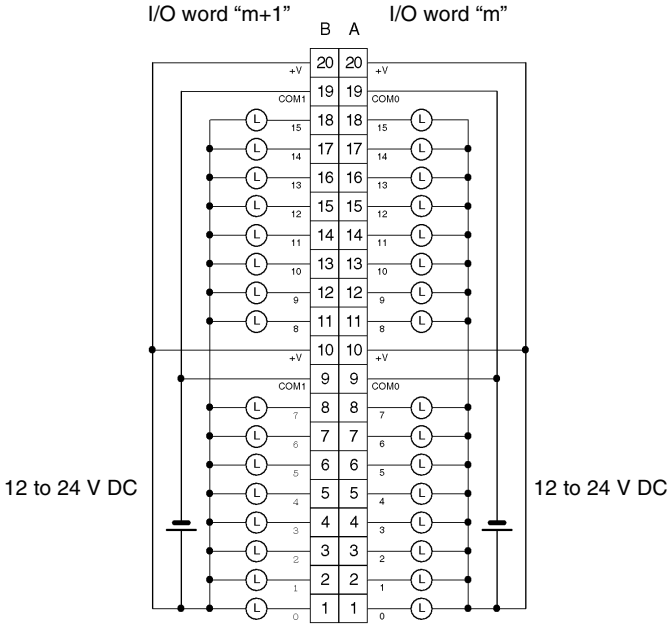
Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2.0 A/common, 4.0 A/Unit
Maximum Inrush Current	4.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.1 ms max.
OFF Response Time	0.8 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	32 (16 points/common, 2 circuits)
Internal Current Consumption	5 V DC 140 mA max.
Fuse	None
External Power Supply	10.2 to 26.4 V DC, 30 mA min.
Weight	70 g max.
Accessories	None

Note The maximum load currents will be 2.0 A/common and 4.0 A/Unit if a pressure-welded connector is used.

Circuit Configuration



Terminal Connections

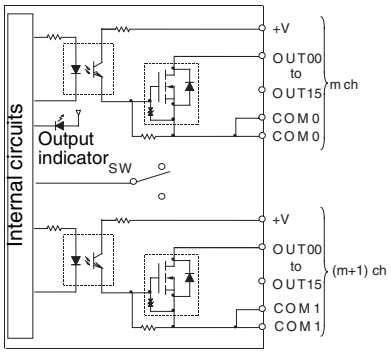


- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.
- Although the +V and COM terminals of rows A and B are internally connected, wire all points completely.

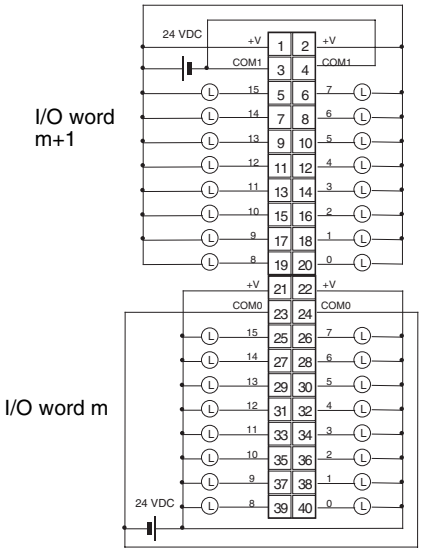
CJ1W-OD233 Transistor Output Unit (MIL Connector, 32 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2 A/common, 4 A/Unit
Maximum Inrush Current	4.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.1 ms max.
OFF Response Time	0.8 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	32 (16 points/common, 2 circuits)
Internal Current Consumption	140 mA max.
Fuse	None
External Power Supply	12 to 24 V DC, 30 mA min.
Weight	70 g max.
Accessories	None

Circuit Configuration



Terminal Connections

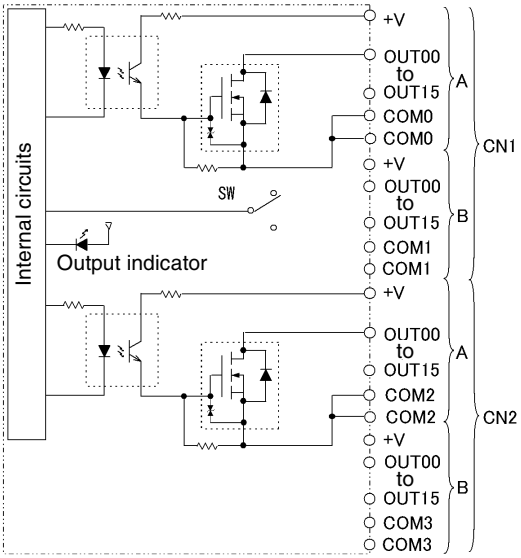


- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.

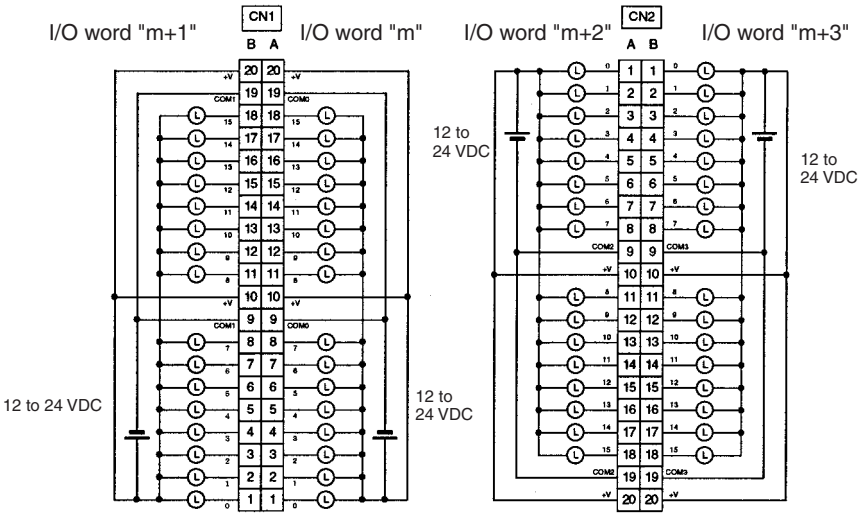
CJ1W-OD261 Transistor Output Unit (Fujitsu Connectors, 64 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 6.4 A/Unit
Maximum Inrush Current	3.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	64 (16 points/common, 4 circuits)
Internal Current Consumption	5 V DC, 170 mA max.
Fuse	None
External Power Supply	10.2 to 26.4 V DC, 50 mA min.
Weight	110 g max.
Accessories	None

Circuit Configuration



Terminal Connections

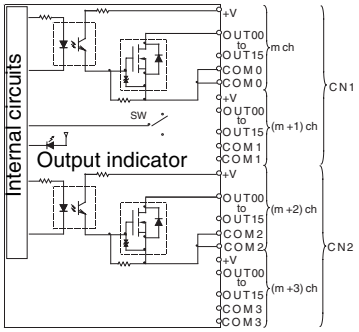


- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.
- Although the +V and COM terminals of rows A and B of CN1 and CN2 are internally connected, wire all points completely.

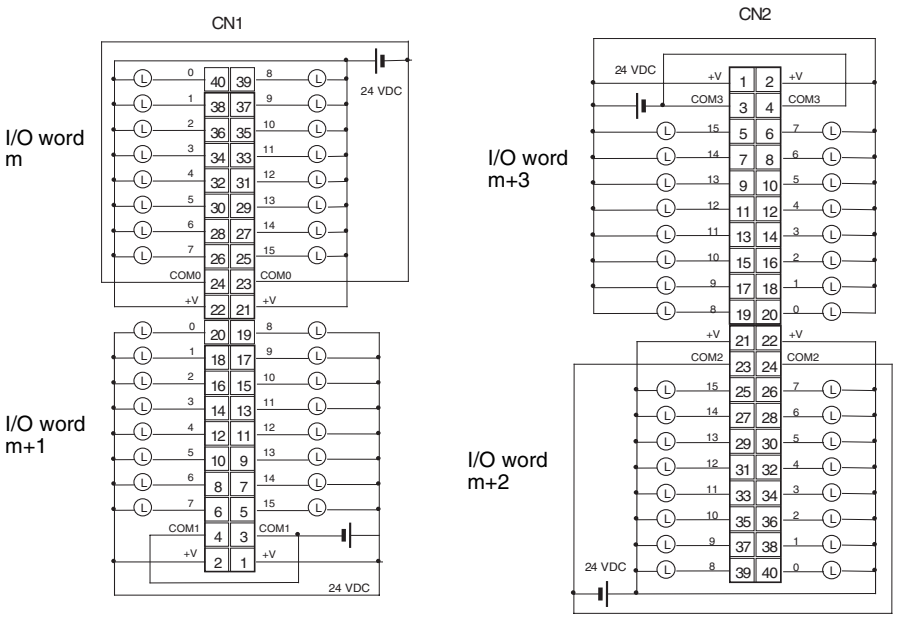
CJ1W-OD263 Transistor Output Unit (MIL Connectors, 62 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 6.4 A/Unit
Maximum Inrush Current	3.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	64 (16 points/common, 4 circuits)
Internal Current Consumption	170 mA max.
Fuse	None
External Power Supply	12 to 24 V DC, 50 mA min.
Weight	110 g max.
Accessories	None

Circuit Configuration



Terminal Connections

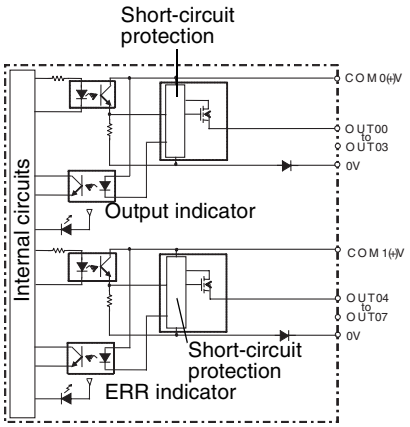


- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.

CJ1W-OD202 Transistor Output Unit (Terminal Block, 8 Points, Sourcing)

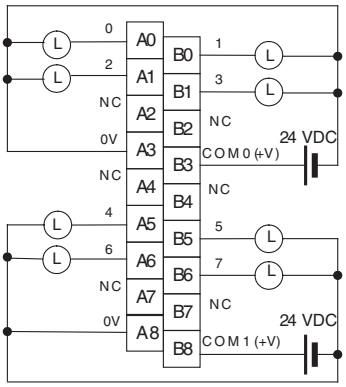
Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	2 A/point, 8 A/Unit
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Protection	Detection current: 6.0 A min. Automatic restart after error clearance. (Refer to page 389.)
Line Disconnection Detection	Detection current: 200 mA (Refer to page 389.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	8 (4 points/common)
Internal Current Consumption	110 mA max.
Fuse	None
External Power Supply	24 V DC, 50 mA min.
Weight	120 g max.

Circuit Configuration



- The ERR indicator will light and the corresponding bit in A050 to A069 (Basic I/O Unit Information, two points per bit) will turn ON if an overcurrent or line disconnection is detected.

Terminal Connections

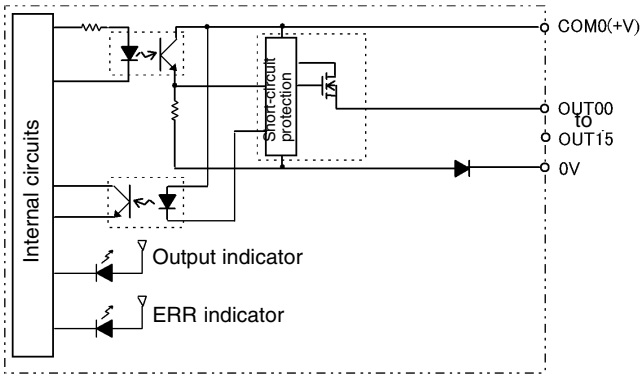


- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.

CJ1W-OD212 Transistor Output Unit (Terminal Block, 16 Points, Sourcing)

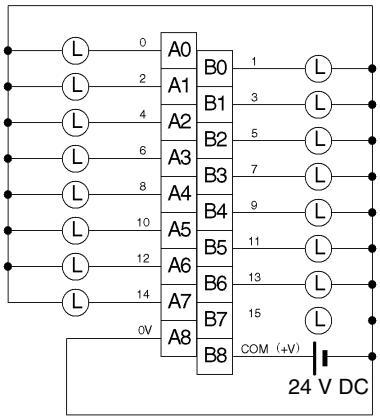
Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.5 A/point, 5.0 A/Unit
Maximum Inrush Current	0.1 mA max.
Leakage Current	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 389.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	16 (16 points/common, 1 circuits)
Internal Current Consumption	5 V DC, 100 mA max.
External Power Supply	20.4 to 26.4 V DC, 40 mA min.
Weight	120 g max.

Circuit Configuration



When overcurrent is detected, the ERR indicator will light, and the corresponding flag in the Basic I/O Unit Information Area (A050 to A069) will turn ON.

Terminal Connections



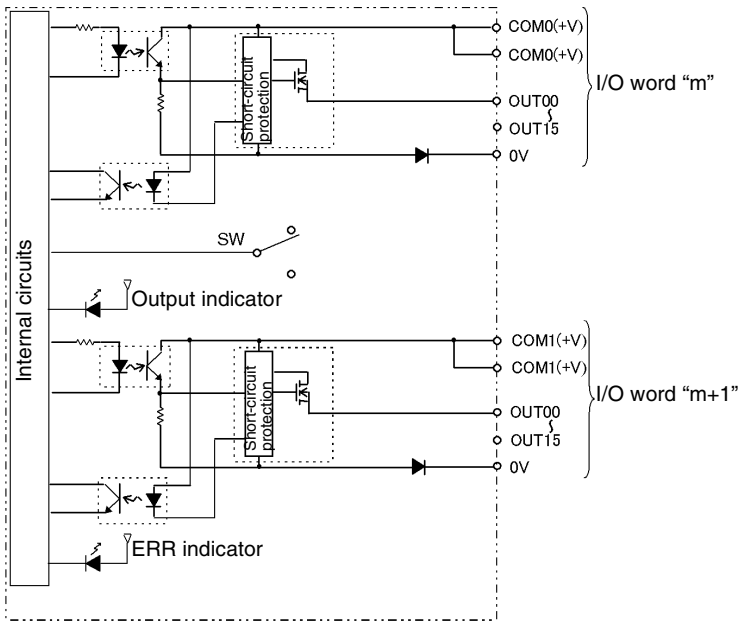
When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed.

CJ1W-OD232 Transistor Output Unit (MIL Connector, 32 Points, Sourcing)

Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2.0 A/common, 4.0 A/Unit
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 389.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	32 (16 points/common, 2 circuits)
Internal Current Consumption	5 V DC 150 mA max.
External Power Supply	20.4 to 26.4 V DC, 70 mA min.
Weight	80 g max.
Accessories	None

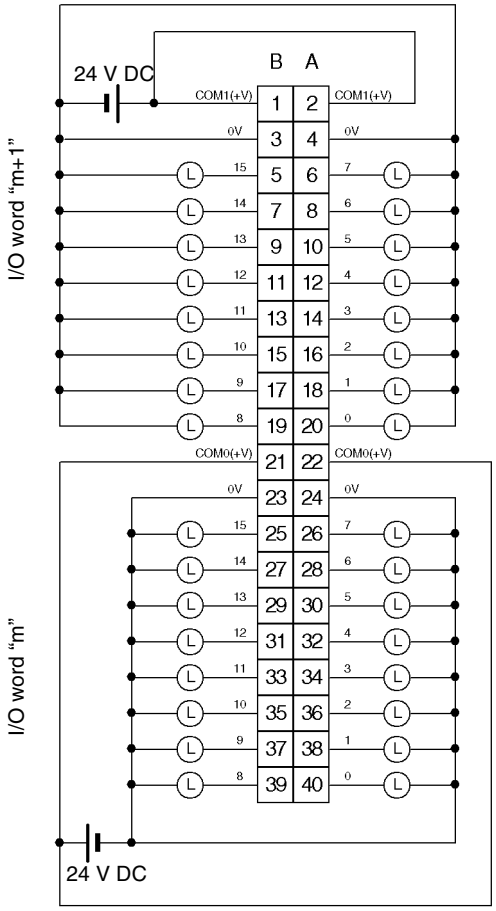
Note The maximum load currents will be 2.0 A/common and 4.0 A/Unit if a pressure-welded connector is used.

Circuit Configuration



When the output current of any output exceeds the detection current, the output for that point will turn OFF. At the same time, the ERR indicator will light and the corresponding flag (one for each common) in the Basic I/O Unit Information Area (A050 to A069) will turn ON.

Terminal Connections

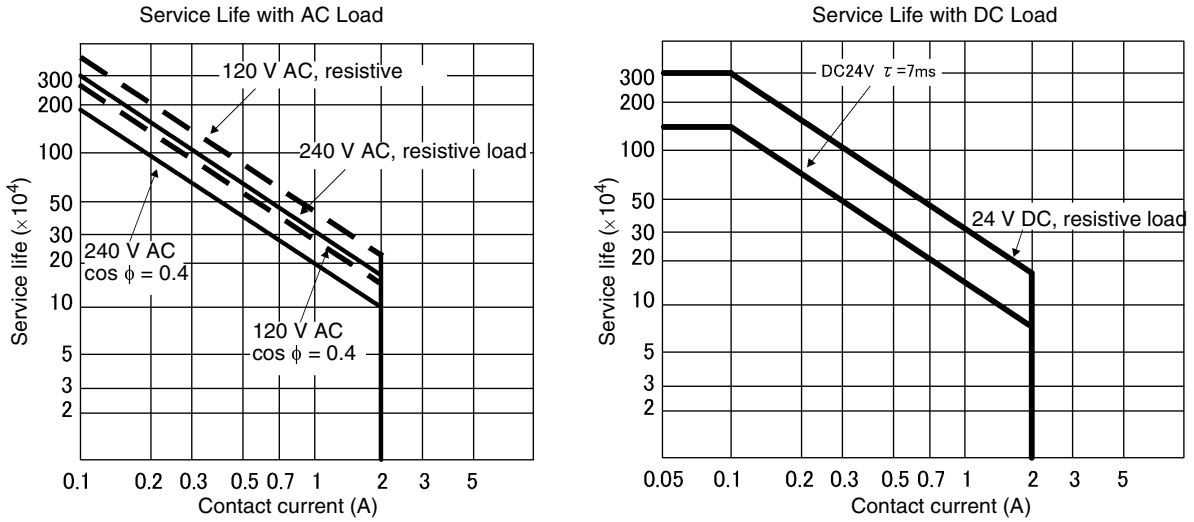


- When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed.
- Although the COM(+V) and 0V of rows A and B are internally connected, wire all points completely.

Life Expectancy of CJ1W-OC201/211 Relays

The life expectancy of the relays (NY-24W-K-IE) in the CJ1W-OC201/211 Contact Output Units is shown in the following diagrams. Use the diagrams to calculate the relay service life based on the operating conditions, and replace the relay before the end of its service life.

Note The diagrams show the life expectancy of the relay itself. Do not use a contact current, therefore, that exceeds the maximum switching capacity specified in the specifications for each Contact Output Unit. If a switching capacity exceeding the specifications is used, the reliability and life expectancy of other parts will be reduced and the Unit may malfunction.



Inductive Load

The life of the Relay varies with the load inductance. If any inductive load is connected to the Contact Output Unit, use an arc killer with the Contact Output Unit using an inductive load.

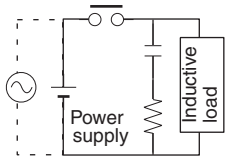
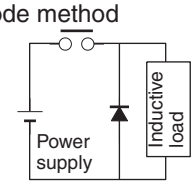
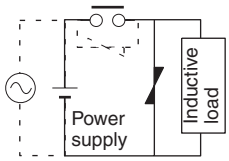
Be sure to connect a diode in parallel with every DC inductive load that is connected to the Contact Output Unit.

Contact Protection Circuit

Arc killers are used with the Contact Output Unit in order to prolong the life of each Relay mounted to the Contact Output Unit, prevent noise, and reduce the generation of carbide and nitrate deposits. Arc killers can, however, reduce relay life if not use correctly.

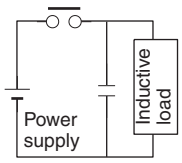
Note Arc killers used with the Contact Output Unit can delay the resetting time required by each Relay mounted to the Contact Output Unit.

Arc killer circuit examples are listed in the following table.

Circuit	Current		Characteristic	Required element
	AC	DC		
CR method 	Yes	Yes	If the load is a relay or solenoid, there is a time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the arc killer in parallel with the load. If the supply voltage is 100 to 200 V, insert the arc killer between the contacts.	The capacitance of the capacitor must be 1 to 0.5 μF per contact current of 1 A and resistance of the resistor must be 0.5 to 1 Ω per contact voltage of 1 V. These values, however, vary with the load and the characteristics of the relay. Decide these values from experiments, and take into consideration that the capacitance suppresses spark discharge when the contacts are separated and the resistance limits the current that flows into the load when the circuit is closed again. The dielectric strength of the capacitor must be 200 to 300 V. If the circuit is an AC circuit, use a capacitor with no polarity.
Diode method 	No	Yes	The diode connected in parallel with the load changes energy accumulated by the coil into a current, which then flows into the coil so that the current will be converted into Joule heat by the resistance of the inductive load. This time lag, between the moment the circuit is opened and the moment the load is reset, caused by this method is longer than that caused by the CR method.	The reversed dielectric strength value of the diode must be at least 10 times as large as the circuit voltage value. The forward current of the diode must be the same as or larger than the load current. The reversed dielectric strength value of the diode may be two to three times larger than the supply voltage if the arc killer is applied to electronic circuits with low circuit voltages.
Varistor method 	Yes	Yes	The varistor method prevents the imposition of high voltage between the contacts by using the constant voltage characteristic of the varistor. There is time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the varistor in parallel with the load. If the supply voltage is 100 to 200 V, insert the varistor between the contacts.	---

Note Do not connect a capacitor as an arc killer in parallel with an inductive load as shown in the following diagram. This arc killer is very effective for preventing spark discharge at the moment when the circuit is opened. However when the contacts are closed, the contacts may be welded due to the current charged in the capacitor.

DC inductive loads can be more difficult to switch than resistive loads. If appropriate arc killers are used, however, DC inductive loads will be as easy to switch as resistive loads.



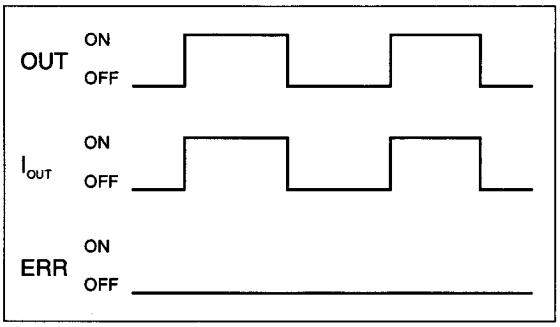
About Contact Output Units

Load Short-circuit Protection and Line Disconnection Detection

This section describes the load short-circuit protection of the CJ1W-OD202 Output Units.

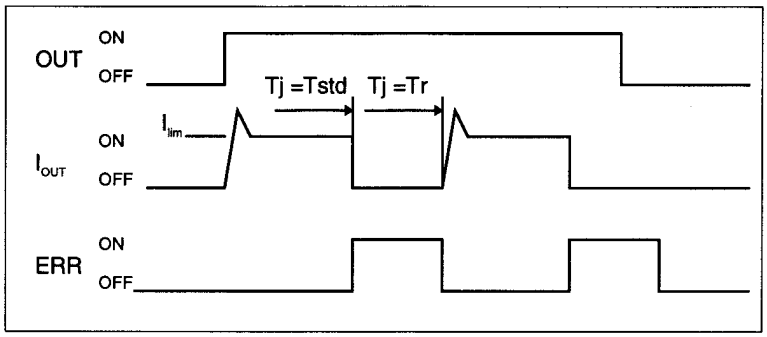
As shown below, normally when the output bit turns ON (OUT), the transistor will turn ON and then output current (Iout) will flow. If the output (Iout) is overloaded or short-circuited exceeding the detection current (Ilim), the output current (Iout) will be limited as shown in *Figure 2* below. When the junction temperature (Tj) of the output transistor reaches the thermal shutdown temperature (Tstd), the output will turn OFF to protect the transistor from being damaged, and the alarm output bit will turn ON to light the ERR indicator. When the junction temperature (Tj) of the transistor drops down to the reset temperature (Tr), the ERR indicator will be automatically reset and the output current will start flowing.

Figure 1: Normal Condition



OUT: OUTPUT instruction
I_{OUT}: Output current
ERR: Alarm output, ERR indicator
I_{lim}: Detection current
Tj: Junction temperature of transistor
Tstd: Thermal shutdown temperature
Tr: Reset temperature

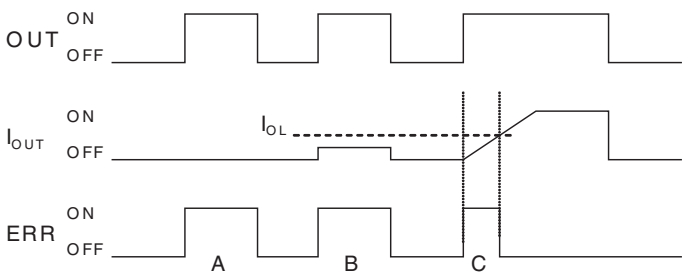
Figure 2: Overload or Short-circuit



Line Disconnection

If the line is disconnected and the output current (Iout) drops below the line disconnection detection current (I_{OL}), the ERR indicator will light as shown in Figure 3.

Figure 3: Line Disconnections



A: Load not connected or load line broken.

B: Current to load at or below line disconnection detection current.

C: Rise of current to load too slow and error detected before the disconnection detection current was reached.

When load L is connected, the ERR indicator may light and the Alarm Output Bit may turn ON for approximately 100 ms. The programming example given later in this section can be used so that an error is not detected in this case.

Operating Restrictions

Although the CJ1W-OD202 is provided with short-circuit protection, these are for protecting internal circuits against momentary short-circuiting in the load. As shown in *Figure 2* below, the short-circuit protection is automatically released when the Tj equals to Tr. Therefore, unless the cause of short-circuit is removed, ON/OFF operations will be repeated in the output. Leaving short-circuits for any length of time will cause internal temperature rise, deterioration of elements, discoloration of the case or PCBs, etc. Therefore, observe the following restrictions.

Restrictions

If a short-circuit occurs in an external load, immediately turn OFF the corresponding output and remove the cause. The CJ1W-OD202 turns ON an alarm output bit that corresponds to the external load output number. There is an alarm output bit for every common.

When an alarm output bit turns ON, use a self-holding bit for the alarm in the user program and turn OFF the corresponding output.

The alarm output bit is allocated in the Basic I/O Unit Information Area (A050 to A089) for every Unit mounting slot.

The following table shows the correspondence between output bits and bits in the Basic I/O Unit Information Area.

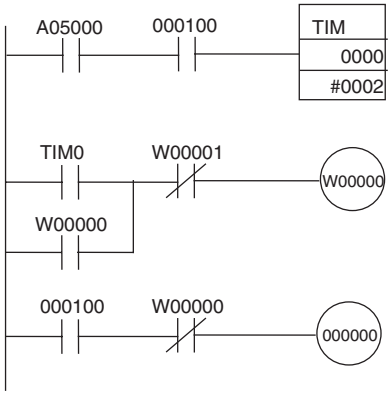
Output bit		0 or 1	2 or 3	4 0r 5	6 or 7
CJ1W-OD202	Mounted in even slot	0	1	2	3
	Mounted in odd slot	8	9	10	11

For example, when the CJ1W-OD202 is mounted in slot 0 on Rack 0, A05000 will turn ON if the output 8 is short-circuited. When the CJ1W-OD202 is mounted in slot 1 of Rack 0, A05011 will turn ON if the output m+3 is short-circuited

Programming Example

In this example, CJ1W-OD212 is mounted in slot 0 of the Rack 0.

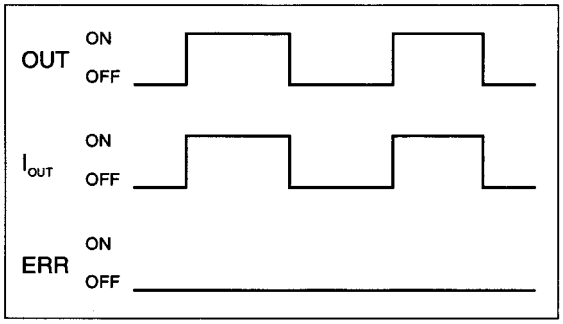
This example shows how to turn OFF output bits CIO 000000 to CIO 000007 immediately if the alarm output bit A05000 turns ON and how to keep the output bits OFF until the cause is removed and the bit is reset using work bit W000001.



Load Short-circuit Protection for CJ1W-OD212/OD232 Output Units

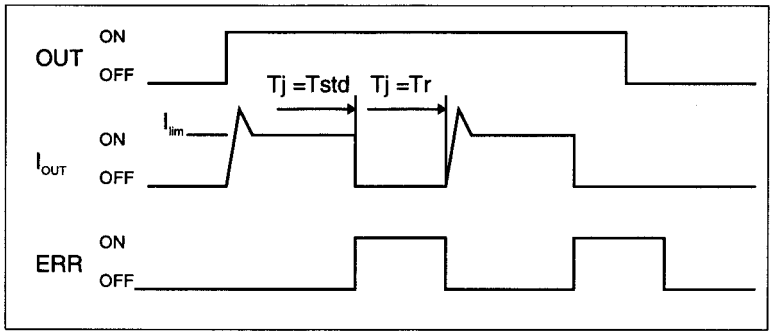
As shown below, normally when the output bit turns ON (OUT), the transistor will turn ON and then output current (Iout) will flow. If the output (Iout) is overloaded or short-circuited exceeding the detection current (Ilim), the output current (Iout) will be limited as shown in *Figure 2* below. When the junction temperature (Tj) of the output transistor reaches the thermal shutdown temperature (Tstd), the output will turn OFF to protect the transistor from being damaged, and the alarm output bit will turn ON to light the ERR indicator. When the junction temperature (Tj) of the transistor drops down to the reset temperature (Tr), the ERR indicator will be automatically reset and the output current will start flowing.

Figure 1: Normal Condition



OUT: OUTPUT instruction
I_{OUT}: Output current
ERR: Alarm output, ERR indicator
I_{lim}: Detection current
Tj: Junction temperature of transistor
Tstd: Thermal shutdown temperature
Tr: Reset temperature

Figure 2: Overload or Short-circuit



Operating Restrictions for the CJ1W-OD212/OD232

These Units are provided with short-circuit protection, these are for protecting internal circuits against momentary short-circuiting in the load. As shown in *Figure 2* below, the short-circuit protection is automatically released when the Tj equals to Tr. Therefore, unless the cause of short-circuit is removed, ON/OFF operations will be repeated in the output. Leaving short-circuits for any length of time will cause internal temperature rise, deterioration of elements, discoloration of the case or PCBs, etc. Therefore, observe the following restrictions.

Restrictions

If a short-circuit occurs in an external load, immediately turn OFF the corresponding output and remove the cause. An an alarm output bit that corresponds to the external load output number is turned ON. There is an alarm output bit for every common.

When an alarm output bit turns ON, use a self-holding bit for the alarm in the user program and turn OFF the corresponding output.

The alarm output bit is allocated in the Basic I/O Unit Information Area (A050 to A069) for every Unit mounting slot.

The following table shows the correspondence between output bits and bits in the Basic I/O Unit Information Area.

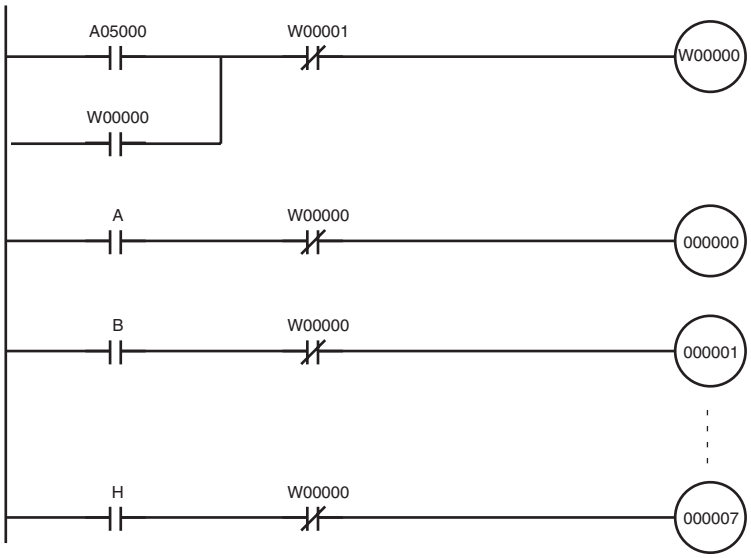
Output bit		m		m+1	m+2	m+3
		0 to 7	8 to 15	0 to 15	0 to 15	0 to 15
CJ1W-OD212	Mounted in even slot	0	---	---	---	---
	Mounted in odd slot	8	---	---	---	---
CJ1W-OD232	Mounted in even slot	0		1	---	---
	Mounted in odd slot	8		9	---	---

For example, when the CJ1W-OD212 is mounted in slot 0 on Rack 0, A05000 will turn ON if the output 8 is short-circuited. When the CJ1W-OD232 is mounted in slot 1 of Rack 0, A05009 will turn ON if the output m+1 is short-circuited

Programming Example

In this example, CJ1W-OD212 is mounted in slot 0 of the Rack 0.

This example shows how to turn OFF output bits CIO 000000 to CIO 000007 immediately if the alarm output bit A05000 turns ON and how to keep the output bits OFF until the cause is removed and the bit is reset using work bit W000001.



Appendix B
Auxiliary Area

A000 to A447: Read-only Area, A448 to A959: Read/Write Area

Read-only Area (Set by System)

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	Bits							
A050	A05000 to A05007	Basic I/O Unit Information, Rack 0 Slot 0	A bit will turn ON to indicate when the load short-circuit protection function alarm output has been given. Only the 4 most LSB are used for the CJ1W-OD202 (2 points per bit), only the LSB is used for the CJ1W-OD212 and only the two most LSB are used for the CJ1W-OD232. Each bit indicates the status for one circuit.	1: Short circuited 0: Normal	---	---	Every cycle	---
	A05008 to A05015	Basic I/O Unit Information, Rack 0 Slot 1			---	---		---
A051 to A069	A05100 to A06915	Basic I/O Unit Information, Racks 2 to 7			---	---		---
A090 to A093	---	User Program Date	These words contain in BCD the date and time that the user program was last overwritten. A09000 to A09007: Seconds (00 to 59) A09008 to A09015: Minutes (00 to 59) A09100 to A09107: Hour (00 to 23) A09108 to A09115: Day of month (00 to 31) A09200 to A09207: Month (01 to 12) A09208 to A09215: Year (00 to 99) A09308 to A09307: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	---	Retained	Retained	---	---
A094 to A097	---	Parameter Date	These words contain in BCD the date and time that the parameters were last overwritten. The format is the same as above	---	Retained	Retained	---	---
A099	A09914	IR/DR Operation between Tasks (CJ1-H CPU Units only)	Turn ON this bit to share index and data registers between all tasks. Turn OFF this bit to use separate index and data registers between in each task.	0: Independent 1: Shared (default)	Retained	Cleared	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A100 to A199	All	Error Log Area	When an error has occurred, the error code, error contents, and error's time and date are stored in the Error Log Area. Information on the 20 most recent errors can be stored. Each error record occupies 5 words; the function of these 5 words is as follows: 1) Error code (bits 0 to 15) 2) Error contents (bits 0 to 15) 3) Minutes (bits 8 to 15), Seconds (bits 0 to 7) 4) Day of month (bits 8 to 15), Hours (bits 0 to 7) 5) Year (bits 8 to 15), Month (bits 0 to 7) Errors generated by FAL(006) and FALS(007) will also be stored in this Error Log. The Error Log Area can be reset from a Programming Device. If the Error Log Area is full (20 records) and another error occurs, the oldest record in A100 to A104 will be cleared, the other 19 records are shifted down, and the new record is stored in A195 to A199.	Error code Error contents: Address of Aux. Area word with details or 0000. Seconds: 00 to 59, BCD Minutes: 00 to 59, BCD Hours: 00 to 23, BCD Day of month: 00 to 31, BCD Year: 00 to 99, BCD	Retained	Retained	Written when error occurs	A50014 A300 A400
A200 A200	A20011	First Cycle Flag	ON for one cycle after PC operation begins (after the mode is switched from PROGRAM to RUN or MONITOR, for example).	ON for the first cycle	---	---	---	---
	A20012	Step Flag	ON for one cycle when step execution is started with STEP(008). This flag can be used for initialization processing at the beginning of a step.	ON for the first cycle after execution of STEP(008).	Cleared	---	---	---
	A20014	Task Started Flag (CJ1-H CPU only)	When a task switches from WAIT or INI to RUN status, this flag will be turned ON within the task for one cycle only. The only difference between this flag and A20015 is that this flag also turns ON when the task switches from WAIT to RUN status.	1: ON for first cycle (including transitions from WAIT and IN) 0: Other				
	A20015	First Task Startup Flag	ON when a task is executed for the first time. This flag can be used to check whether the current task is being executed for the first time so that initialization processing can be performed if necessary.	1: First execution 0: Not executable for the first time or not being executed.	Cleared	---	---	---
A201	A20110	Online Editing Wait Flag	ON when an online editing process is waiting. (If another online editing command is received while waiting, the other command won't be recorded and an error will occur.)	1: Waiting for online editing 0: Not waiting for online editing	Cleared	Cleared	---	A527
	A20111	Online Editing Flag	ON when an online editing process is being executed.	1: Online editing in progress 0: Online editing not in progress	Cleared	Cleared	---	A527

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A202	A20200 to A20207	Communications Port Enabled Flags	ON when a network instruction (SEND, RECV, CMND, or PMCR) or background execution (CJ1-H CPU Units only) can be executed with the corresponding port number. Bits 00 to 07 correspond to communications ports 0 to 7. When two or more network instructions are programmed with the same port number, use the corresponding flag as an execution condition to prevent the instructions from being executed simultaneously. (The flag for a given port is turned OFF while a network instruction with that port number is being executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated, and the corresponding Flag will be turned OFF.)	1: Network instruction is not being executed 0: Network instruction is being executed (port busy)	Cleared	---	---	---
A203 to A210	All	Communications Port Completion Codes	These words contain the completion codes for the corresponding port numbers when network instructions (SEND, RECV, CMND, or PMCR) or background execution (CJ1-H CPU Units only) have been executed. (The corresponding word will be cleared when background execution has been completed for CJ1-H CPU Units.) Words A203 to A210 correspond to communications ports 0 to 7. (The completion code for a given port is cleared to 0000 when a network instruction with that port number is executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated, and a completion code will be stored in the corresponding word.)	Non-zero: Error code 0000: Normal condition	Cleared	---	---	---
A219	A21900 to A21907	Communications Port Error Flags	ON when an error occurred during execution of a network instruction (SEND, RECV, CMND, or PMCR). Bits 00 to 07 correspond to communications ports 0 to 7. (All of these flags are turned OFF at the start of program execution and the flag for a given port is turned OFF when a network instruction with that port number is executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CJ1-H CPU Unit, a communications port will be automatically allocated, and the corresponding Flag will be turned OFF if an error occurs.)	1: Error occurred 0: Normal condition	Cleared	---	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A220 to A259	A22000 to 25915	Basic I/O Unit Input Response Times	These words contain the actual input response times for CJ-series Basic I/O Units. When the Basic I/O Unit input response time setting is changed in the PC Setup while the PC is in PROGRAM mode, the setting in the PC Setup will not match the actual value in the Basic I/O Unit unless the power is turned OFF and then ON again. In that case, the actual value can be monitored in these words.	0 to 17 hexadecimal	Retained	See function column.	---	PC Setup (Basic I/O Unit Input response time settings)
A260	All	I/O Allocation Status	Indicates the current status of I/O allocation, i.e., Automatic I/O Allocation at Startup or User-set I/O Allocations.	0000 Hex: Automatic I/O Allocation at Startup BBBB Hex: User-set I/O Allocations	Retained	Retained	---	---
A261	A26100	CPU Bus Unit Setup Area Initialization Error Flag (CJ1-H CPU Units only)	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	ON: Error in CPU Bus Unit Setup OFF: I/O tables generated normally	Retained	Cleared	When I/O tables are generated	---
	A26102	I/O Overflow Flag (CJ1-H CPU Units only)	ON: Overflow in maximum number of I/O points Turns OFF when I/O tables are generated normally.	ON: Overflow in maximum number of I/O points OFF: I/O tables generated normally				A40111 (Too many I/O points)
	A26103	Duplication Error Flag (CJ1-H CPU Units only)	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.	ON: The same unit number was used more than once. OFF: I/O tables generated normally				A40113 (duplicated number)
	A26104	I/O Bus Error Flag (CJ1-H CPU Units only)	ON: I/O bus error Turns OFF when I/O tables are generated normally.	ON: I/O bus error OFF: I/O tables generated normally				A40114 (I/O but error)
	A26107	Special I/O Unit Error Flag (CJ1-H CPU Units only)	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.	ON: Error in a Special I/O Unit OFF: I/O tables generated normally				---
	A26109	I/O Unconfirmed Error Flag (CJ1-H CPU Units only)	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.	ON: I/O detection has not been completed. OFF: I/O tables generated normally				---
A262 and A263	All	Maximum Cycle Time	These words contain the maximum cycle time (the maximum cycle time of the program execution cycle for a Parallel Processing Mode) since the start of PC operation. The cycle time is recorded in 8-digit hexadecimal with the leftmost 4 digits in A263 and the rightmost 4 digits in A262.	0 to FFFFFFFF: 0 to 429,496,729.5 ms (0.1ms units)	---	---	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A264 and A265	All	Present Cycle Time	These words contain the present cycle time (the maximum cycle time of the program execution cycle for a Parallel Processing Mode) in 8-digit hexadecimal with the leftmost 4 digits in A265 and the rightmost 4 digits in A264.	0 to FFFFFFFF: 0 to 429,496,729.5 ms	---	---	---	---
A266 and A267	All	Program Execution Time+ Priority Peripheral Servicing Time	Total of all slice times for program execution and all slice times for peripheral servicing. A267 (Upper bytes) A266 (Lower bytes)	00000000 to FFFFFFFF Hex 0.0 to 429,496,729.5 ms (0.1-ms increments)	Cleared	Cleared	Each cycle	---
A268	---	Peripheral Servicing Cycle Time (CJ1-H CPU Units only)	In Parallel Processing with Synchronous or Asynchronous Memory Access, this word contains the peripheral servicing cycle time. The time is updated every cycle and is recorded in 16-bit binary.	0 to 4E20 Hex, (0.0 to 2,000.0 ms in units of 0.1 ms)	---	---	Each cycle	A40515
A294	All	Task Number when Program Stopped	This word contains the task number of the task that was being executed when program execution was stopped because of a program error. (A298 and A299 contain the program address where program execution was stopped.)	Normal tasks: 0000 to 001F (task 0 to 31) Interrupt tasks: 8000 to 80FF (task 0 to 255)	Cleared	Cleared	---	A298/ A299

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A295	A29508	Instruction Processing Error Flag	This flag and the Error Flag (ER) will be turned ON when an instruction processing error has occurred and the PC Setup has been set to stop operation for an instruction error. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Error Flag ON 0: Error Flag OFF	Cleared	Cleared	---	A294, A298/A299 PC Setup (Operation when instruction error has occurred)
	A29509	Indirect DM/EM BCD Error Flag	This flag and the Access Error Flag (AER) will be turned ON when an indirect DM/EM BCD error has occurred and the PC Setup has been set to stop operation an indirect DM/EM BCD error. (This error occurs when the content of an indirectly addressed DM or EM word is not BCD although BCD mode has been selected.) CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Not BCD 0: Normal	Cleared	Cleared	---	A294, A298/A299 PC Setup (Operation when instruction error has occurred)
	A29510	Illegal Access Error Flag	This flag and the Access Error Flag (AER) will be turned ON when an illegal access error has occurred and the PC Setup has been set to stop operation an illegal access error. (This error occurs when a region of memory is access illegally.) CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. The following operations are considered illegal access: 1) Reading/writing the system area 2) Reading/writing EM File Memory 3) Writing to a write-protected area 4) Indirect DM/EM BCD error (in BCD mode) (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Illegal access occurred 0: Normal condition	Cleared	Cleared	---	A294, A298/A299 PC Setup (Operation when instruction error has occurred)

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A295	A29511	No END Error Flag	ON when there isn't an END(001) instruction in each program within a task. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: No END 0: Normal condition	Cleared	Cleared	---	A294, A298/ A299
	A29512	Task Error Flag	ON when a task error has occurred. The following conditions generate a task error. There isn't even one regular task that is executable (started). •There isn't a program allocated to the task. •(The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Error 0: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29513	Differentiation Overflow Error Flag	The allowed value for Differentiation Flags which correspond to differentiation instructions has been exceeded. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Error 0: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29514	Illegal Instruction Error Flag	ON when a program that cannot be executed has been stored. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	1: Error 0: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29515	UM Overflow Error Flag	ON when the last address in UM (User Memory) has been exceeded. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON.	1: Error 0: Normal	Cleared	Cleared	---	A294, A298/ A299
A298	All	Program Address Where Program Stopped (Rightmost 4 digits)	These words contain the 8-digit binary program address of the instruction where program execution was stopped due to a program error. (A294 contains the task number of the task where program execution was stopped.)	Right 4 digits of the program address	Cleared	Cleared	---	A294
A299		Program Address Where Program Stopped (Leftmost 4 digits)		Left 4 digits of the program address	Cleared	Cleared	---	

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A300	All	Error Log Pointer	When an error occurs, the Error Log Pointer is incremented by 1 to indicate the location where the next error record will be recorded as an offset from the beginning of the Error Log Area (A100 to A199). The Error Log Pointer can be cleared to 00 by turning A50014 (the Error Log Reset Bit) from OFF to ON. When the Error Log Pointer has reached 14 (20 decimal), the next record is stored in A195 to A199 when the next error occurs.	00 to 14 hexadecimal	Retained	Retained	Written when error occurs	A50014
A301	All	Current EM Bank	This word contains the current EM bank number in 4-digit hexadecimal. The current bank number can be changed with the EMBC(281) instruction.	0000 to 000C hexadecimal	Cleared	Cleared	---	---
A302	A30200 to A30215	CPU Bus Unit Initializing Flags	These flags are ON while the corresponding CPU Bus Unit is initializing after its CPU Bus Unit Restart Bit (A50100 to A50115) is turned from OFF to ON or the power is turned ON. Bits 00 to 15 correspond to unit numbers 0 to 15. Use these flags in the program to prevent the CPU Bus Unit's refresh data from being used while the Unit is initializing. IORF(097) cannot be executed while an CPU Bus Unit is initializing. These bits are turned OFF automatically when initialization is completed.	0: Not initializing 1: Initializing (Reset to 0 automatically after initialization.)	Retained	Cleared	Written during initialization	A50100 to A50115
A330 to A335	A33000 to A33515	Special I/O Unit Initializing Flags	These flags are ON while the corresponding Special I/O Unit is initializing after its Special I/O Unit Restart Bit (A50200 to A50715) is turned from OFF to ON or the power is turned ON. The bits in these words correspond to unit numbers 0 to 95 as follows: A33000 to A33015: Units 0 to 15 A33100 to A33115: Units 16 to 31 ---- A33500 to A33515: Units 80 to 95 Use these flags in the program to prevent the Special I/O Unit's refresh data from being used while the Unit is initializing. Also, IORF(097) cannot be executed while a Special I/O Unit is initializing. These bits are turned OFF automatically when initialization is completed.	0: Not initializing 1: Initializing (Reset to 0 automatically after initialization.)	Retained	Cleared	---	A50200 to A50715
A336	A33600 to A33616	Units Detected at Startup (Racks 0 to 3) (CJ1-H CPu Unit only)	The number of Units detected on each Rack is stored in 1-digit hexadecimal (0 to A Hex). Example: The following would be stored if Rack 0 had 1 Unit, Rack 1 had 4 Units, Rack 2 had 8 Units and Rack 3 had 10 Units: A336 = A 8 4 1	Rack 0: A33600 to A33603 Rack 1: A33604 to A33607 Rack 2: A33608 to A33611 Rack 3: A33612 to A33615	---	---	---	---
A339 and A340	All	Maximum Differentiation Flag Number	These words contain the maximum value of the differentiation flag numbers being used by differentiation instructions.		See Function column.	Cleared	Written at the start of operation	A29513

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A343	A34300 to A34302	Memory Card Type	Indicates the type of Memory Card, if any, installed. This information is recorded when the PC power is turned ON or the Memory Card power switch is turned ON.	0: None 4: Flash ROM	Retained	See Function column.	See Function column.	---
	A34306	EM File Memory Format Error Flag	ON when a format error occurs in the first EM bank allocated for file memory. (The flag is turned OFF when formatting is completed normally.)	1: Format error 0: No format error	Retained	Cleared	---	---
	A34307	Memory Card Format Error Flag	ON when the Memory Card is not formatted or a formatting error has occurred. (The flag is turned OFF when formatting is completed normally.) This flag is written when the PC power is turned ON or the Memory Card power switch is turned ON.	1: Format error 0: No format error	Retained	See Function column.	See Function column.	
	A34308	File Transfer Error Flag	ON when an error occurred while writing data to file memory. (The flag is turned OFF when PC operation begins or data is written successfully.)	1: Error 0: No error	Retained	Cleared	Written when file data is written	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A343	A34309	File Write Error Flag	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory. (The flag is turned OFF when PC operation begins or data is written successfully.)	1: Write not possible 0: Normal condition	Retained	Cleared	Written when file data is written	---
	A34310	File Read Error	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted). (The flag is turned OFF when PC operation begins or data is read successfully.)	1: Read not possible 0: Normal condition	Retained	Cleared	Written when file data is read	---
	A34311	File Missing Flag	ON when an attempt is made to read a file that doesn't exist, or an attempt is made to write to a file in a directory that doesn't exist. (The flag is turned OFF when PC operation begins or data is read successfully.)	1: Specified file or directory is missing 0: Normal condition	Retained	Cleared	Written when file data is read	---
	A34313	File Memory Operation Flag	ON while any of the following operations is being executed. OFF when none of them are being executed. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Easy backup operation. (The flag is turned OFF when PC operation begins.)	1: Instruction being executed. 0: Instruction not being executed.	Retained	Cleared	Written when file memory instruction is executed	---
	A34314	Accessing File Data Flag	ON while file data is being accessed. Use this flag to prevent two file memory instructions from being executed at the same time. (The flag is turned OFF when PC operation begins.)	1: File being accessed 0: File not being accessed	Retained	Cleared	---	---
	A34315	Memory Card Detected Flag	ON when a Memory Card has been detected. OFF when a Memory Card has not been detected.	1: Memory Card detected 0: Memory Card not detected	Retained	Cleared	Written when Memory Card is inserted, or the power is turned ON.	
A344	All	EM File Memory Starting Bank	Contains the starting bank number of EM file memory (bank number of the first formatted bank). All EM banks from this starting bank to the last bank in EM are formatted for use as file memory. To convert the EM Area for use as file memory, first set the PC Setup's EM File Memory Function setting to 1, set the PC Setup's EM File Memory Starting Bank setting (0 to 2), and then format the EM Area from a Programming Device The PC Setup's EM file memory settings won't agree with the actual settings unless the EM Area is formatted after the PC Setup's EM file memory settings have been changed. In that case, the actual settings can be determined with this word.	0000 to 0002 Hex Bank 0 to C2 Hex	Retained	Retained	Written when EM file formatting is performed	PC Setup (EM File Memory Function setting and EM File Memory Starting Bank setting)

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A346 and A347	All	Number of Remaining Words to Transfer	These words contain the 8-digit hexadecimal number of words remaining to be transferred by FREAD(700) or FWRIT(701). When one of these instructions is executed, the number of words to be transferred is written to A346 and A347. While the data is being transferred, the value in these words is decremented. A326 contains the rightmost 4-digits and A347 contains the leftmost 4-digits. Check the content of these words to determine whether or not the planned number of words have been transferred successfully.	Data remaining in transfer	Retained	Cleared	Written as FREAD or FWRIT is being executed. Decremented as data is actually transferred.	---
A351 to A354	All	Calendar/ Clock Area	These words contain the CPU Unit's internal clock data in BCD. The clock can be set from a Programming Device such as a Programming Console, with the DATE(735) instruction, or with a FINS command (CLOCK WRITE, 0702).		Retained	Retained	Written every cycle	---
	A35100 to A35107		Seconds (00 to 59) (BCD)					
	A35108 to A35115		Minutes (00 to 59) (BCD)					
	A35200 to A35207		Hours (00 to 23) (BCD)					
	A35208 to A35215		Day of the month (01 to 31) (BCD)					
	A35300 to A35307		Month (01 to 12) (BCD)					
	A35308 to A35315		Year (00 to 99) (BCD)					
	A35400 to A35407		Day of the week (00 to 06) (BCD) 00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday					
A360 to A391	A36001 to A39115	Executed FAL Number Flags	The flag corresponding to the specified FAL number will be turned ON when FAL(006) is executed. Bits A36001 to A39115 correspond to FAL numbers 001 to 511. The flag will be turned OFF when the error is cleared.	1: That FAL was executed 0: That FAL wasn't executed	Retained	Cleared	Written when error occurs	A40215

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A392	A39204	RS-232C Port Error Flag	ON when an error has occurred at the RS-232C port. (Not valid in peripheral bus mode or NT Link mode.)	1: Error 0: No error	Retained	Cleared	Written when error occurs	---
	A39205	RS-232C Port Send Ready Flag (No-protocol mode)	ON when the RS-232C port is able to send data in no-protocol mode.	1: Able-to-send 0: Unable-to-send	Retained	Cleared	Written after transmission	---
	A39206	RS-232C Port Reception Completed Flag (No-protocol mode)	ON when the RS-232C port has completed the reception in no-protocol mode. • When the number of bytes was specified: ON when the specified number of bytes is received. • When the end code was specified: ON when the end code is received or 256 bytes are received.	1: Reception completed 0: Reception not completed	Retained	Cleared	Written after reception	---
	A39207	RS-232C Port Reception Overflow Flag (No-protocol mode)	ON when a data overflow occurred during reception through the RS-232C port in no-protocol mode. • When the number of bytes was specified: ON when more data is received after the reception was completed but before RXD(235) was executed. • When the end code was specified: ON when more data is received after the end code was received but before RXD(235) was executed. ON when 257 bytes are received before the end code.	1: Overflow 0: No overflow	Retained	Cleared	---	---
	A39212	Peripheral Port Communications Error Flag	ON when a communications error has occurred at the peripheral port. (Not valid in peripheral bus mode or NT Link mode.)	1: Error 0: No error	Retained	Cleared	---	---
A393	A39300 to A39307	RS-232C Port PT Communications Flag	The corresponding bit will be ON when the RS-232C port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	1: Communicating 0: Not communicating	Retained	Cleared	Written when there is a normal response to the token	---
	A39308 to A39315	RS-232C Port PT Priority Registered Flags	The corresponding bit will be ON for the PT that has priority when the RS-232C port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7. These flags are written when the priority registration command is received.	1: Priority registered 0: Priority not registered	Retained	Cleared	See *Function* column.	---
	A39300 to A39315	RS-232C Port Reception Counter (No-protocol mode)	Indicates (in binary) the number of bytes of data received when the RS-232C port is in no-protocol mode.		Retained	Cleared	Written when data is received	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A394	A39400 to A39407	Peripheral Port PT Communications Flag	The corresponding bit will be ON when the peripheral port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	1: Communicating 0: Not communication	Retained	Cleared	Written when there is a normal response to the token	---
	A39408 to 39415	Peripheral Port PT Priority Registered Flags	The corresponding bit will be ON for the PT that has priority when the peripheral port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7. These flags are written when the priority registration command is received.	1: Priority registered 0: Priority not registered	Retained	Cleared	See *Function* column.	---
A395	A39506	File Deleted Flags	The system deleted the remainder of an EM file memory file that was being updated when a power interruption occurred.	1: File deleted 0: No files deleted	Cleared	Cleared	Written when the system deletes the file.	---
	A39507		The system deleted the remainder of a Memory Card file that was being updated when a power interruption occurred.	1: File deleted 0: No files deleted	Cleared	Cleared	Written when the system deletes the file.	---
	A39511	Memory Corruption Detected Flag	ON when memory corruption is detected when the power supply is turned ON.	1: Memory corruption 0: Normal operation	Retained	See Function column.	Written when power is turned ON.	---
	A39512	DIP Switch Pin 6 Status Flag	The status of pin 6 on the DIP switch on the front of the CPU Unit is written to this flag every cycle.	1: Pin 6 ON 0: Pin 6 OFF	Retained	See Function column.	Written every cycle	---
A397	---	Simple Backup Write Capacity (CJ1-H CPU Units only)	If a write for a simple backup operation fails, A397 will contain the Memory Card capacity that would have been required to complete the write operation. The value is in Kbytes. (This indicates that the Memory Card did not have the specified capacity when the write operation was started.) A397 will be cleared to 0000 Hex when the write is completed successfully for a simple backup operation.	0000 Hex: Write completed normally 0001 to FFFF Hex: Write error (value indicates required capacity from 1 to 65,535 Kbytes).	Retained	Retained	When write is executed	
A400	All	Error code	When a non-fatal error (user-defined FALS(006) or system error) or a fatal error (user-defined FALS(007) or system error) occurs, the 4-digit hexadecimal error code is written to this word. When two or more errors occur simultaneously, the highest error code will be recorded. Refer to page 418 for details on error codes.	Error code	Cleared	Cleared	Written when error occurs	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A401	A40106	FALS Error Flag (Fatal error)	ON when a non-fatal error is generated by the FALS(006) instruction. The CPU Unit will continue operating and the ERR/ALM indicator will flash. The corresponding error code will be written to A400. Error codes C101 to C2FF correspond to FALS numbers 001 to 511. This flag will be turned OFF when the FALS errors are cleared.	1: FALS(006) executed 0: FALS(006) not executed	Cleared	Cleared	Written when error occurs	A400
	A40108	Cycle Time Too Long Flag (Fatal error)	ON if the cycle time exceeds the maximum cycle time set in the PC Setup (the cycle time monitoring time). CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. This flag will be turned OFF when the error is cleared.	0: Cycle time under max. 1: Cycle time over max.	Cleared	Cleared	Written when the cycle time exceeds max.	PC Setup (Cycle time monitoring time)
	A40109	Program Error Flag (Fatal error)	ON when program contents are incorrect. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299. The type of program error that occurred will be stored in bits 8 to 15 of A295. Refer to the description of A295 for more details on program errors. This flag will be turned OFF when the error is cleared.	1: Error 0: No error	Cleared	Cleared	---	A294, A295, A298 and A299
	A40110	I/O Setting Error Flag (Fatal error)	ON when a Basic I/O Unit registered in the I/O Table does not match the Basic I/O Unit actually installed in the PC or, for a CJ1-H CPU Unit, an Interrupt Input Unit is connected in the wrong position (not slot 0 to 4). CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. This flag will be turned OFF when the error is cleared.	1: Error 0: No error	Cleared	Cleared	---	---
	A40111	Too Many I/O Points Flag (Fatal error)	ON when the number of I/O points being used in Basic I/O Units exceeds the maximum allowed for the PC. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. This flag will be turned OFF when the error is cleared.	1: Error 0: No error	Cleared	Cleared	---	A407

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A401	A40113	Duplication Error Flag (Fatal error)	ON in the following cases: • Two CPU Bus Units have been assigned the same unit number. • Two Special I/O Units have been assigned the same unit number. • Two Basic I/O Units have been allocated the same data area words. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The duplicated unit number is indicated in A409 to A416. (This flag will be turned OFF when the error is cleared.)	1: Duplication error 0: No duplication	Cleared	Cleared	---	A410 to A416
	A40114	I/O Bus Error Flag (Fatal error)	ON when an error occurs in a data transfer between the CPU Unit and a Unit mounted to a slot or when the End Cover is not connected to the CPU Rack or an Expansion Rack. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The slot number (00 to 09) where the I/O Bus Error occurred is written to A40400 to A40407 in binary and the rack number (00 to 03) is written to A40408 to A40415 in binary. When the End Cover is not connected to the CPU Rack or an Expansion Rack, 0E Hex will be stored in both locations. (This flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	A404
	A40115	Memory Error Flag (Fatal error)	ON when an error occurred in memory or there was an error in automatic transfer from the Memory Card when the power was turned ON. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The location where the error occurred is indicated in A40300 to A40308, and A40309 will be turned ON if there was an error during automatic transfer at start-up. This flag will be turned OFF when the error is cleared. (The automatic transfer at start-up error cannot be cleared without turning off the PC.)	1: Error 0: No error	Cleared	Cleared	---	A40300 to A40308, A40309
A402	A40202	Special I/O Unit Setting Error Flag (Non-fatal error)	ON when an installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The unit number of the Unit where the setting error occurred is indicated in A428 to A433. (This flag will be turned OFF when the error is cleared.)	1: Setting error detected 0: No setting error	Cleared	Cleared	---	A428 to A433

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A402	A40203	CPU Bus Unit Setting Error Flag (Non-fatal error)	ON when an installed CPU Bus Unit does not match the CPU Bus Unit registered in the I/O table. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The unit number of the Unit where the setting error occurred is written to A427. (This flag will be turned OFF when the error is cleared.)	1: Setting error detected 0: No setting error	Cleared	Cleared	---	A427
	A40204	Battery Error Flag (Non-fatal error)	ON if the CPU Unit's battery is disconnected or its voltage is low and the Detect Battery Error setting has been set in the PC Setup. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. This flag can be used to control an external warning light or other indicator to indicate that the battery needs to be replaced. (This flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	PC Setup (Detect Battery Error)
	A40206	Special I/O Unit Error Flag (Non-fatal error)	ON when an error occurs in a data exchange between the CPU Unit and a Special I/O Unit (including an error in the Special I/O Unit itself). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The Special I/O Unit where the error occurred will stop operating and the unit number of the Unit where the data exchange error occurred is indicated in A418 through A423. (This flag will be turned OFF when the error is cleared.)	1: Error in one or more Units 0: No errors in any Unit	Cleared	Cleared	---	A418 to A423
	A40207	CPU Bus Unit Error Flag (Non-fatal error)	ON when an error occurs in a data exchange between the CPU Unit and an CPU Bus Unit (including an error in the CPU Bus Unit itself). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The CPU Bus Unit where the error occurred will stop operating and the unit number of the Unit where the data exchange error occurred is indicated in A417. (This flag will be turned OFF when the error is cleared.)	1: Error in one or more Units 0: No error in any Unit	Cleared	Cleared	---	A417

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	Bits							
A402	A40210	PC Setup Error Flag (Non-fatal error)	ON when there is a setting error in the PC Setup. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The location of the error will be written to A406. (This flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	A406
	A40212	Basic I/O Unit Error Flag (Non-fatal error)	ON when an error has occurred in a Basic I/O Unit. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The location of the error will be written to A408. (This flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	A408
	A40213	Interrupt Task Error Flag (Non-fatal error)	ON when the Detect Interrupt Task Errors setting in the PC Setup is set to "Detect" and an interrupt task is executed for more than 10 ms during I/O refreshing of a Special I/O Unit. This flag will also be turned ON if an attempt is made to refresh a Special I/O Unit's I/O from an interrupt task with IORF(097) while the Unit's I/O is being refreshed by cyclic I/O refreshing (duplicate refreshing). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (This flag will be turned OFF when the error is cleared.)	1: Interrupt task error 0: No error	Cleared	Cleared	---	A426, PC Setup (Detect Interrupt Task Errors setting)
	A40215	FAL Error Flag (Non-fatal error)	ON when a non-fatal error is generated by executing FAL(006). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The bit in A360 to A391 that corresponds to the FAL number specified in FALS(006) will be turned ON and the corresponding error code will be written to A400. Error codes 4101 to 42FF correspond to FAL numbers 001 to 2FF (0 to 511). (This flag will be turned OFF when the error is cleared.)	1: FALS(006) error occurred 0: FALS(006) not executed	Cleared	Cleared	Written when error occurs	A360 to A391, A400
A403	A40300 to A40308	Memory Error Location	When a memory error occurs, the Memory Error Flag (A40115) is turned ON and one of the following flags is turned ON to indicate the memory area where the error occurred A40300: User program A40304: PC Setup A40305: Registered I/O Table A40307: Routing Table A40308: CPU Bus Unit Settings When a memory error occurs, the CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (The corresponding flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	A40115

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	Bits							
A403	A40309	Memory Card Start-up Transfer Error Flag	ON when automatic transfer at start-up has been selected and an error occurs during automatic transfer. An error will occur if there is a transfer error, the specified file does not exist, or the Memory Card is not installed. (This flag will be turned OFF when the error is cleared by turning the power off. The error cannot be cleared without turning the power off.)	1: Error 0: No error	Cleared	Cleared	Written when power is turned ON	---
	A40310	Flash Memory Error Flag (CJ1-H CPU Units only)	ON when the flash memory is physically destroyed.	1: Error 0: No error	Cleared	Cleared	When error is detected.	---
A404	A40400 to A40407	I/O Bus Error Slot Number	Contains the 8-bit binary slot number (00 to 09) where an I/O Bus Error occurred. When the End Cover is not connected to the CPU Rack or an Expansion Rack, 0E Hex will be stored. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The I/O Bus Error Flag (A40114) will be ON. (This flag will be turned OFF when the error is cleared.)	00 to 09 (slot number 00 to 09)	Cleared	Cleared	---	A40114
	A40408 to A40415	I/O Bus Error Rack Number	Contains the 8-bit binary rack number (00 to 03) where an I/O Bus Error occurred. When the End Cover is not connected to the CPU Rack or an Expansion Rack, 0E Hex will be stored. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The I/O Bus Error Flag (A40114) will be ON. (This flag will be turned OFF when the error is cleared.)	00 to 03 (rack number 00 to 03)	Cleared	Cleared	---	A40114
A405	A40508	Interrupt Input Unit Position Error Flag (CJ1-H CPU Units only)	ON when the Interrupt Input Unit is not connected in one of the five positions (slots 0 to 4) next to the CPU Unit on the CPU Rack. Even if a Unit is physically in one of the first 5 positions, a Dummy Unit can be registered in the I/O table, causing a Unit to be defined in a position different from its physical position. (This flag will be turned OFF when the error is cleared.)	1: Position not correct 0: Position correct	Cleared	Cleared	Written when error occurs	A40110
	A40515	Peripheral Servicing Too Long Flag (CJ1-H CPU Units only)	Turns ON when the peripheral servicing time in a Parallel Processing Mode exceeds 2 s. This will also cause a cycle time error and operation will stop.	1: Too long (Parallel processing cannot be used.) 0: Not too long (Parallel processing can be used.)	Cleared	Cleared	Written when error occurs	A268
A406	All	PC Setup Error Location	When there is a setting error in the PC Setup, the location of that error is written to A406 in 4-digit hexadecimal. The location is given as the address displayed on a Programming Console. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (A406 will be cleared when the cause of the error is eliminated.)	000A to 009F hexadecimal	Cleared	Cleared	Written when error occurs	A40210

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	Bits							
A407	A40700 to A40712	Too Many I/O Points, Details	The 6 possible causes of the Too Many I/O Points Error are listed below. The 3-digit binary value in A40713 to A40715 indicates the cause of the error (values 0 to 5 correspond to causes 1 to 6, below). The 13-bit binary value in A40700 to A40712 indicates the details: the excessive value or the duplicated unit number. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. 1) The number of I/O points will be written here when the total number of I/O points set in the I/O Table (excluding Slave Racks) exceed the maximum allowed for the CPU Unit. 2) The number of Racks will be written here when the number of Expansion Racks exceeds the maximum. (The relevant value will be written here (A40700 to A40712) when the error occurs. These bits will be cleared when the error is cleared.)	0000 to 1FFF hexadecimal	Cleared	Cleared	Written when error occurs	A40111, A40713 to A40715
A407	A40713 to A40715	Too Many I/O Points, Cause	The 3-digit binary value of these bits indicates the cause of the Too Many I/O Points Error and shows the meaning of the value written to bits A40700 to A40712. Values of 000 to 101 (0 to 5) correspond to causes 1 through 6 described in "Too Many I/O Points, Cause 1," above. (These bits will be cleared when the error is cleared.)	000: Too many I/O total 101: Too many Racks 111: Too many Units on a Rack	Cleared	Cleared	Written when error occurs	---
A408	A40800 to A40807	Basic I/O Unit Error, Slot Number	When an error has occurred in a Basic I/O Unit, A40212 will be turned ON and the slot number where the error occurred will be written here in binary. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (These bits will be cleared when the error is cleared.)	00 to 09 hexadecimal (Slots 0 to 9)	Cleared	Cleared	---	A40212
	A40808 to A40815	Basic I/O Unit Error, Rack Number	When an error has occurred in a Basic I/O Unit, A40212 will be turned ON and the Rack number where the error occurred will be written here in binary. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (These bits will be cleared when the error is cleared.)	00 to 03 hexadecimal (Racks 0 to 3)	Cleared	Cleared	---	A40212
A409	A40900 to A40903	Expansion Rack Number Duplication Flags	The corresponding flag will be turned ON when an Expansion Rack's starting word address was set from a Programming Device and two Racks have overlapping word allocations or a Rack's starting address exceeds CIO 0901. Bits 00 to 03 correspond to Racks 0 to 3. (The corresponding flag will be cleared when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	Bits							
A410	A41000 to A41015	CPU Bus Unit Number Duplication Flags	The Duplication Error Flag (A40113) and the corresponding flag in A410 will be turned ON when an CPU Bus Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light.	1: Duplication detected 0: No duplication	Cleared	Cleared	---	A40113
A411 to A416	A41100 to A41615	Special I/O Unit Number Duplication Flags	The Duplication Error Flag (A40113) and the corresponding flag in A411 through A416 will be turned ON when a Special I/O Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F. (Bits A41100 to A41615 correspond to unit numbers 000 to 05F (0 to 95).) CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The corresponding bit will also be turned ON when the Special I/O Unit's words are also allocated to a Basic I/O Unit on an Expansion Rack because of the Expansion Rack's starting word setting.	1: Duplication detected 0: No duplication	Cleared	Cleared	---	A40113
A417	A41700 to A41715	CPU Bus Unit Error, Unit Number Flags	When an error occurs in a data exchange between the CPU Unit and an CPU Bus Unit, the CPU Bus Unit Error Flag (A40207) is turned ON and the bit in A417 corresponding to the unit number of the Unit where the error occurred is turned ON. Bits 00 to 15 correspond to unit numbers 0 to F. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	1: Error 0: No error	Cleared	Cleared	---	A40207
A418 to A423	A41800 to A42315	Special I/O Unit Error, Unit Number Flags	When an error occurs in a data exchange between the CPU Unit and a Special I/O Unit, the Special I/O Unit Error Flag (A40206) will be turned ON. Each bit corresponds to a unit number. Bit 00 in A418 to bit 15 in A423 correspond to unit numbers 0 to 95. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (Bits A41800 to A42315 correspond to unit numbers 000 to 05F (0 to 95).) The unit number of the Unit where the error occurred is indicated in A417. If the unit number of the Unit is uncertain, none of the flags will be turned ON. (The flag will be turned OFF when the error is cleared.)	1: Error 0: No error	Cleared	Cleared	---	A40206

Address		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related flags, settings
Words	**Bits**							
A426	A42600 to A42611	Interrupt Task Error, Unit Number	An attempt was made to refresh a Special I/O Unit's I/O from an interrupt task with IORF(097) while the Unit's I/O is being refreshed by cyclic I/O refreshing (duplicate refreshing). A42600 to A42611: contain the Special I/O Unit's unit number. These bits will be cleared when the error is cleared.	Unit number: 000 to 05F (0 to 95)	Cleared	Cleared	---	A40213 A42615
	A42615	Interrupt Task Error Cause Flag	When A40213 (the Interrupt Task Error Flag) is ON, this flag indicates the cause of the error. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	1: Duplicated refreshing	Cleared	Cleared	---	A40213, A42600 to A42611
A427	A42700 to A42715	CPU Bus Unit Setting Error, Unit Number Flags	When an CPU Bus Unit Setting Error occurs, A40203 and the bit in this word corresponding to the Unit's unit number are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	1: Setting error 0: No setting error	Cleared	Cleared	Written when power is turned ON or I/O is recognized	A40203
A428 to A433	A42800 to A43315	Special I/O Unit Setting Error, Unit Number Flags	When a Special I/O Unit Setting Error occurs, A40202 and the bit in these words corresponding to the Unit's unit number are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F. (Bits A42800 to A43315 correspond to unit numbers 000 to 05F (0 to 95).) The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	1: Setting error 0: No setting error	Cleared	Cleared	Written when power is turned ON or I/O is recognized	A40202
A440	All	Max. Interrupt Task Processing Time	Contains the Maximum Interrupt Task Processing Time in units of 0.1 ms. (This value is written after the interrupt task with the max. processing time is executed and cleared when PC operation begins.)	0000 to FFFF hexadecimal	Cleared	Cleared	See Function column.	---
A441	All	Interrupt Task With Max. Processing Time	Contains the task number of the interrupt task with the maximum processing time. Hexadecimal values 8000 to 80FF correspond to task numbers 00 to FF. Bit 15 is turned ON when an interrupt has occurred. (This value is written after the interrupt task with the max. processing time is executed and cleared when PC operation begins.)	8000 to 80FF hexadecimal	Cleared	Cleared	See Function column.	---

Read/Write Area (Set by User)

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	Bit							
A500	A50012	IOM Hold Bit	Turn this bit ON to preserve the status of the I/O Memory when shifting from PROGRAM to RUN or MONITOR mode or vice versa. The I/O Memory includes the CIO Area, Transition Flags, Timer Flags and PVs, Index Registers, Data Registers, and the Current EM Bank Number. (If the status of the IOM Hold Bit itself is preserved in the PC Setup (IOM Hold Bit Status), the status of the I/O Memory Area will be retained when the PC is turned ON or power is interrupted.)	1: Retained 0: Not retained	Retained	See Function column.	See Function column.	PC Setup (IOM Hold Bit Status setting)
	A50013	Forced Status Hold Bit	Turn this bit ON to preserve the status of bits that have been force-set or force-reset when shifting from PROGRAM to MONITOR mode or vice versa. Bits that have been force-set or force-reset will always return to their default status when shifting to RUN mode. (If the status of the Forced Status Hold Bit itself is preserved in the PC Setup (Forced Status Hold Bit Status), the status of force-set and force-reset bits will be retained when the PC is turned ON or power is interrupted.)	1: Retained 0: Not retained	Retained	See Function column.	See Function column.	PC Setup (Forced Status Hold Bit Status setting)
	A50014	Error Log Reset Bit	Turn this bit ON to reset the Error Log Pointer (A300) to 00. The contents of the Error Log Area itself (A100 to A199) are not cleared. (This bit is automatically reset to 0 after the Error Log Pointer is reset.)	0 → 1: Clear	Retained	Cleared	---	A100 to A199, A300
	A50015	Output OFF Bit	Turn this bit ON to turn OFF all outputs from Basic I/O Units and Special I/O Units. The INH indicator on the front of the CPU Unit will light while this bit is ON. (The status of the Output OFF Bit is retained through power interruptions.)		Retained	Retained	---	---
A501	A50100 to A50115	CPU Bus Unit Restart Bits	Turn these bits ON to restart (initialize) the CPU Bus Unit with the corresponding unit number. Bits 00 to 15 correspond to unit numbers 0 to F. When a restart bit is turned ON, the corresponding CPU Bus Unit Initializing Flag (A30200 to A30215) will be turned ON. Both the restart bit and initializing flag will be turned OFF automatically when initialization is completed.	0 to 1: Restart 1 to 0: Restart completed Turned OFF by the system when the Unit has been restarted.	Retained	Cleared	---	A30200 to A30215
A502 to A507	A50200 to A50715	Special I/O Unit Restart Bits	Turn these bits ON to restart (initialize) the Special I/O Unit with the corresponding unit number. Bits A50200 to A50715 correspond to unit numbers 0 to 95. When a restart bit is turned ON, the corresponding Special I/O Unit Initializing Flag (A33000 to A33515) will be turned ON. Both the restart bit and initializing flag will be turned OFF automatically when initialization is completed.	0 to 1: Restart 1 to 0: Restart completed Turned OFF by the system when the Unit has been restarted.	Retained	Cleared	---	A33000 to A33515

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	Bit							
A508	A50809	Differentiate Monitor Completed Flag	ON when the differentiate monitor condition has been established during execution of differentiation monitoring. (This flag will be cleared to 0 when differentiation monitoring starts.)	1: Monitor condition established 0: Not yet established	Retained	Cleared	---	---
	A50811	Trace Trigger Monitor Flag	ON when a trigger condition is established by the Trace Start Bit (A50814). OFF when the next Data Trace is started by the Sampling Start bit (A50815).	1: Trigger condition established 0: Not yet established or not tracing	Retained	Cleared	---	---
	A50812	Trace Completed Flag	ON when sampling of a region of trace memory has been completed during execution of a Trace. OFF when the next time the Sampling Start Bit (A50815) is turned from OFF to ON.	1: Trace completed 0: Not tracing or trace in progress	Retained	Cleared	------	---
	A50813	Trace Busy Flag	ON when the Sampling Start Bit (A50815) is turned from OFF to ON. OFF when the trace is completed.	1: Trace in progress 0: Not tracing (not sampling)			---	---
A508	A50814	Trace Start Bit	Turn this bit from OFF to ON to establish the trigger condition. The offset indicated by the delay value (positive or negative) determines which data samples are valid.	1: Trace trigger condition established 0: Not established			---	---
	A50815	Sampling Start Bit	When a data trace is started by turning this bit from OFF to ON from a Programming Device, the PC will begin storing data in Trace Memory by one of the three following methods: 1) Data is sampled at regular intervals (10 to 2,550 ms). 2) Data is sampled when TRSM(045) is executed in the program. 3) Data is sampled at the end of every cycle. The operation of A50815 can be controlled only from a Programming Device.	0 to 1: Starts data trace (sampling) Turned ON from Programming Device.			---	---
A510 to A511		Start-up Time	These words contain the time at which the power was turned ON. The contents are updated every time that the power is turned ON. The data is stored in BCD. A51000 to A51007: Second (00 to 59) A51008 to A51015: Minute (00 to 59) A51100 to A51107: Hour (00 to 23) A51108 to A51115: Day of month (00 to 31)	See Function column.	Retained	See Function column.	Written when power is turned ON	---
A512 to A513		Power Interruption Time	These words contain the time at which the power was interrupted. The contents are updated every time that the power is interrupted. The data is stored in BCD. A51200 to A51207: Second (00 to 59) A51208 to A51215: Minute (00 to 59) A51300 to A51307: Hour (00 to 23) A51308 to A51315: Day of month (00 to 31) (These words are not cleared at start-up.)	See Function column.	Retained	Retained	Written at power interruption	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	**Bit**							
A514		Number of Power Interruptions	Contains the number of times that power has been interrupted since the power was first turned ON. The data is stored in binary. To reset this value, overwrite the current value with 0000. (This word is not cleared at start-up, but it is cleared when the Memory Corruption Detected Flag (A39511) goes ON.)	0000 to FFFF hexadecimal	Retained	Retained	Written when power is turned ON	A39511
A523		Total Power ON Time	Contains the total time that the PC has been on in 10-hour units. The data is stored in binary and it is updated every 10 hours. To reset this value, overwrite the current value with 0000. (This word is not cleared at start-up, but it is cleared to 0000 when the Memory Corruption Detected Flag (A39511) goes ON.)	0000 to FFFF hexadecimal	Retained	Retained	---	---
A526	A52600	RS-232C Port Restart Bit	Turn this bit ON to restart the RS-232C port. (Do not use this bit when the port is operating in peripheral bus mode.) This bit is turned OFF automatically when the restart processing is completed.	0 to 1: Restart	Retained	Cleared	---	---
	A52601	Peripheral Port Restart Bit	Turn this bit ON to restart the peripheral port. This bit is turned OFF automatically when the restart processing is completed.	0 to1: Restart	Retained	Cleared	---	---
A527	A52700 to A52707	Online Editing Disable Bit Validator	The Online Editing Disable Bit (A52709) is valid only when this byte contains 5A. To disable online editing from a Programming Device, set this byte to 5A and turn ON A52709. (Online editing refers to changing or adding to the program while the PC is operating in MONITOR mode.)	5A: A52709 enabled Other value: A52709 disabled	Retained	Cleared	---	A52709
	A52709	Online Editing Disable Bit	Turn this bit ON to disable online editing. The setting of this bit is valid only when A52700 to A52707 have been set to 5A.	1: Disabled 0: Not disabled	Retained	Cleared	---	A52700 to A52707

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	Bit							
A528	A52800 to A52807	RS-232C Port Error Flags	These flags indicate what kind of error has occurred at the RS-232C port; they are automatically turned OFF when the RS-232C port is restarted. (These flags are not valid in peripheral bus mode and only bit 5 is valid in NT Link mode.) Bits 0 and 1: Not used. Bit 2: ON when there was a parity error. Bit 3: ON when there was a framing error. Bit 4: ON when there was an overrun error. Bit 5: ON when there was a timeout error. Bits 6 and 7: Not used.	See Function column.			---	---
	A52808 to A52815	Peripheral Port Error Code	These flags indicate what kind of error has occurred at the peripheral port; they are automatically turned OFF when the peripheral port is restarted. Bits 8 and 9: Not used. Bit 10: ON when there was a parity error. Bit 11: ON when there was a framing error. Bit 12: ON when there was an overrun error. Bit 13: ON when there was a timeout error. Bits 14 and 15: Not used.	See Function column.	---	---	---	---
A529	---	FAL/FALS Number for System Error Simulation (CJ1-H CPU Units only)	Set a dummy FAL/FALS number to use to simulate the system error using FAL(006) or FALS(007). When FAL(006) or FALS(007) is executed and the number in A529 is the same as the one specified in the operand of the instruction, the system error given in the operand of the instruction will be generated instead of a user-defined error.	0001 to 01FF Hex: FAL/FALS numbers 1 to 511 0000 or 0200 to FFFF Hex: No FAL/FALS number for system error simulation. (No error will be generated.)	Retained	Cleared	---	---
A530	---	Power Interruption Disable Setting (CJ1-H CPU Units only)	Set to A5A5 Hex to disable power interrupts (except the Power OFF Interrupt task) between DI(693) and EI(694) instructions.	A5A5 Hex: Masking power interruption processing enabled Other: Masking power interruption processing not enabled.	Cleared	Cleared	---	---
A595 and A596	---	IR00 Output for Background Execution (CJ1-H CPU Units only)	When an index register is specified as the output for an instruction processed in the background, A595 and A596 receive the output instead of IR00.	0000 0000 to FFFF FFFF Hex (A596 contains the leftmost digits.)	Cleared	Cleared	---	---
A597	---	DR00 Output for Background Execution (CJ1-H CPU Units only)	When a data register is specified as the output for an instruction processed in the background, A597 receives the output instead of DR00.	0000 to FFFF Hex	Cleared	Cleared	---	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	Bit							
A598	A59800	FPD Teaching Bit	Turn this bit ON to set the monitoring time automatically with the teaching function. While A59800 is ON, FPD(269) measures how long it takes for the diagnostic output to go ON after the execution condition goes ON. If the measured time exceeds the monitoring time, the measured time is multiplied by 1.5 and that value is stored as the new monitoring time. (The teaching function can be used only when a word address has been specified for the monitoring time operand.)	1: Teach monitoring time 0: Teaching function off	Cleared	Cleared	---	---
	A59801	Equals Flag for Background Execution (CJ1-H CPU Units only)	Turns ON if matching data is found for an SRCH(181) instruction executed in the background.	1: Search data found in table 0: Search data not found	Cleared	Cleared	---	---
A604 to A607		Macro Area Output Words	After the subroutine specified in MCRO(099) has been executed, the results of the subroutine are transferred from A604 through A607 to the specified destination words. (output parameter words)	Output data: 4 words	Cleared	Cleared	---	---
A619	A61901	Peripheral Port Settings Changing Flag	ON while the peripheral port's communications settings are being changed. This flag will be turned ON when STUP(237) is executed and it will be turned OFF after the settings have been changed.	1: Changing 0: Not changing	Retained	Cleared	---	---
	A61902	RS-232C Port Settings Changing Flag	ON while the RS-232C port's communications settings are being changed. This flag will be turned ON when STUP(237) is executed and it will be turned OFF after the settings have been changed.	1: Changing 0: Not changing	Retained	Cleared	---	---
A620	A62001	Communications Unit 0, Port 1 Settings Changing Flag	The corresponding flag will be ON when the settings for that port are being changed. The flag will be turned ON when STUP(237) is executed and it will be turned OFF by an event issued from the Serial Communications Unit after the settings have been changed. It is also possible for the user to indicate a change in serial port settings by turning these flags ON.	1: Changing 0: Not changing	Retained	Cleared	---	---
A620	A62002	Communications Unit 0, Port 2 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---
	A62003	Communications Unit 0, Port 3 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---
	A62004	Communications Unit 0, Port 4 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---
A621 to A635	A62100 to A63504	Communications Units 0 to 15, Ports 1 to 4 Settings Changing Flag	Same as above.	1: Changing 0: Not changing	Retained	Cleared	---	---

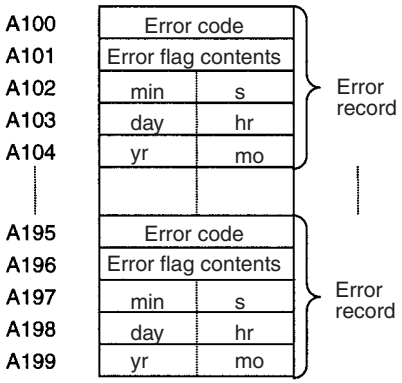
Addresses		Name	Function	Settings	Status after mode change	Status at startup	Write timing	Related Flags, Settings
Word	**Bit**							
A650	A65014	Replacement Error Flag	ON when the Replacement Start Bit (A65015) is turned ON to replace the program, but there is an error. If the Replacement Start Bit is turned ON again, the Replacement Error Flag will be turned OFF.	1: Replacement error 0: No replacement error, or the Replacement Start Bit (A65015) is ON.	Retained	Cleared	---	---
	A65015	Replacement Start Bit	Program replacement starts when the Replacement Start Bit is turned ON if the Program Password (A651) is valid (A5A5 Hex). Do not turn OFF the Replacement Start Bit during program replacement. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error. It is possible to confirm if program replacement is being executed by reading the Replacement Start Bit using a Programming Device, PT, or host computer.	1: Program replaced 0: Replacement completed, or after power is turned ON	Retained	Cleared	---	---
A651	---	Program Password	Type in the password to replace a program. A5A5 Hex: Replacement Start Bit (A65015) is enabled. Any other value: Replacement Start Bit (A65015) is disabled. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error.	---	Retained	Cleared	---	---
A654 to 657	---	Program File Name	When program replacement starts, the program file name will be stored in ASCII. File names can be specified up to eight characters in length excluding the extension. File names are stored in the following order: A654 to A657 (i.e., from the lowest word to the highest), and from the highest byte to the lowest. If a file name is less than eight characters, the lowest remaining bytes and the highest remaining word will be filled with spaces (20 Hex). Null characters and space characters cannot be used within file names. Example: File name is ABC.OBJ 15 0 A654 41 42 A655 43 20 A656 20 20 A657 20 20	---	Retained	Cleared	---	---

Note In CJ-series PCs, the following flags are provided in a special read-only area and can be specified with the labels given in the table. These flags are not contained in the Auxiliary Area.

Flag area	Name	Label	Meaning
Condition Code Area	Error Flag	**ER**	Turns ON when an error occurs in processing an instructions, indicating an error end to the instruction.
	Access Error Flag	**AER**	Turns ON when an attempt is made to access an illegal area. The status of this flag is maintain only during the current cycle and only in the task in which it occurred.
	Carry Flag	**CY**	Turns ON when there is a carry or borrow in a math operation, when a bit is shifted into the Carry Flag, etc.
	Greater Than Flag	**>**	Turns ON when the result of comparing two values is "greater than," when a value exceeds a specified range, etc.
	Equals Flag	**=**	Turns ON when the result of comparing two values is "equals," when the result of a math operation is 0, etc.
	Less Than Flag	**<**	Turns ON when the result of comparing two values is "less than," when a value is below a specified range, etc.
	Negative Flag	**N**	Turns ON when the MSB in the result of a math operation is 1.
	Overflow Flag	**OF**	Turns ON when the result of a math operation overflows.
	Underflow Flag	**UF**	Turns ON when the result of a math operation underflows.
	Greater Than or Equals Flag	**>=**	Turns ON when the result of comparing two values is "greater than or equals."
	Not Equal Flag	**<>**	Turns ON when the result of comparing two values is "not equal."
	Less than or Equals Flag	**<=**	Turns ON when the result of comparing two values is "less than or equals."
	Always ON Flag	**A1**	This flag is always ON.
	Always OFF Flag	**A0**	This flag is always OFF.
Clock Pulse Area	0.02-s clock pulse	**0.02s**	Repeatedly turns ON for 0.02 s and OFF for 0.02 s.
	0.1-s clock pulse	**0.1s**	Repeatedly turns ON for 0.1 s and OFF for 0.1 s.
	0.2-s clock pulse	**0.2s**	Repeatedly turns ON for 0.2 s and OFF for 0.2 s.
	1-s clock pulse	**1s**	Repeatedly turns ON for 1 s and OFF for 1 s.
	1-min clock pulse	**1min**	Repeatedly turns ON for 1 min and OFF for 1 min.

Details on Auxiliary Area Operation

A100 to A199: Error Log Area



The following data would be generated in an error record if a memory error (error code 80F1) occurred on 1 April 1998 at 17:10:30 with the error located in the PC Setup (04 Hex).

80	F1
00	04
10	30
01	17
98	04

The following data would be generated in an error record if an FALS error with FALS number 001 occurred on 2 May 1997 at 8:30:15.

C1	01
00	00
30	15
02	08
97	05

Error Codes and Error Flags

Classification	Error code	Meaning	Error flags
System-defined fatal errors	80F1	Memory error	A403
	80C0 to 80C7 80CE, 80CF	I/O bus error	A404
	80E9	Duplicate number error	A410, A411 to 416 (See note 3.)
	80E1	Too many I/O error	A407
	80E0	I/O setting error	---
	80F0	Program error	A295 to 299 (See note 4.)
	809F	Cycle time too long error	---
	80EA	Duplicate Expansion Rack number error	A40900 to 40907
User-defined fatal errors	C101 to C2FF	FALS instruction executed (See note 1.)	---
User-defined non-fatal errors	4101 to 42FF	FAL instruction executed (See note 2.)	---
System-defined non-fatal errors	008B	Interrupt task error	A426
	009A	Basic I/O error	A408
	009B	PC Setup setting error	A406
	0200 to 020F	CPU Bus Unit error	A417
	0300 to 035F	Special I/O Unit error	A418 to 423 (See note 5.)
	00F7	Battery error	---
	0400 to 040F	CPU Bus Unit setup error	A427
	0500 to 055F	Special I/O Unit setup error	A428 to 433 (See note 5.)

Note 1. C101 to C2FF will be stored for FALS numbers 001 to 511.

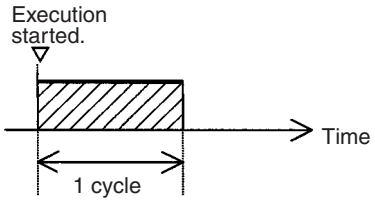
2. 4101 to 42FF will be stored for FAL numbers 001 to 511.

3. The contents of the error flags for a duplicate number error are as follows:
Bits 0 to 7: Unit number (binary), 00 to 5F Hex for Special I/O Units, 00 to 0F Hex for CPU Bus Units
Bits 8 to 14: All zeros.
Bit 15: Unit type, 0 for CPU Bus Units and 1 for Special I/O Units.

4. Only the contents of A295 is stored as the error flag contents for program errors.

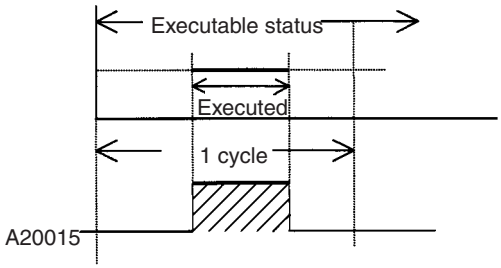
5. 0000 Hex will be stored as the error flag contents.

A20011: First Cycle Flag

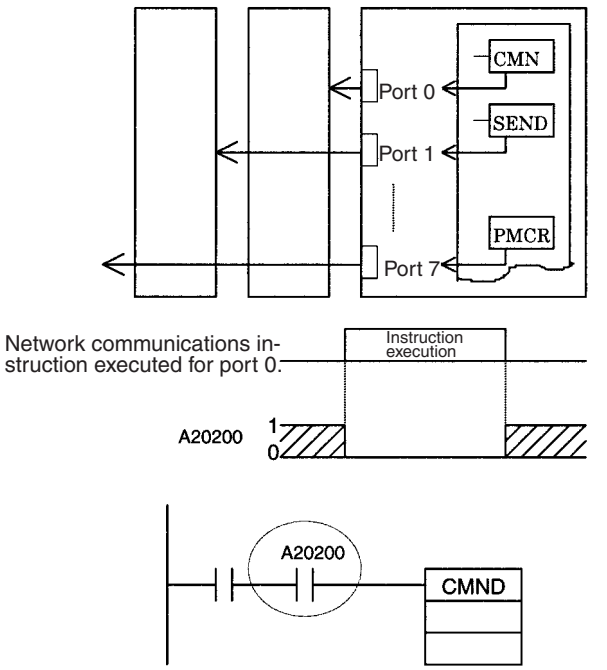


A20015: Initial Task Flag

A20015 will turn ON during the first time a task is executed after it has reached executable status. It will be ON only while the task is being executed and will not turn ON if following cycles.

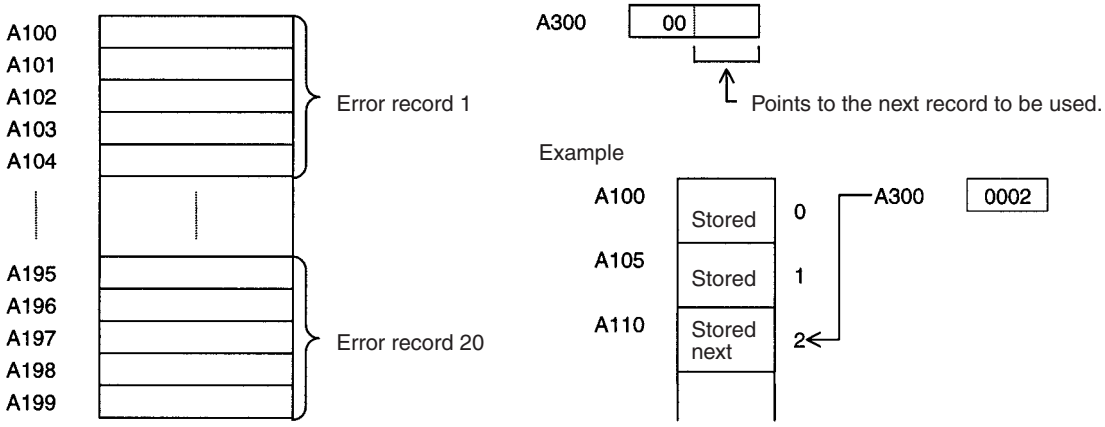


A20200 to A20207: Communications Port Enabled Flags

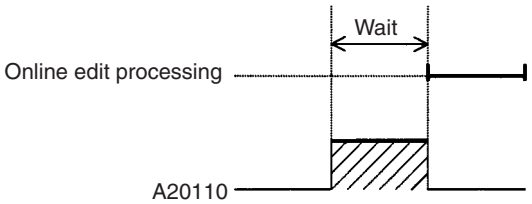


The program is designed so that CMND(490) will be executed only when A20200 is ON.

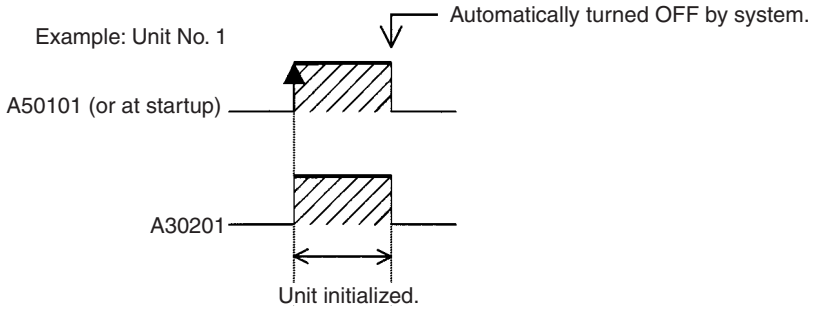
A300: Error Record Pointer



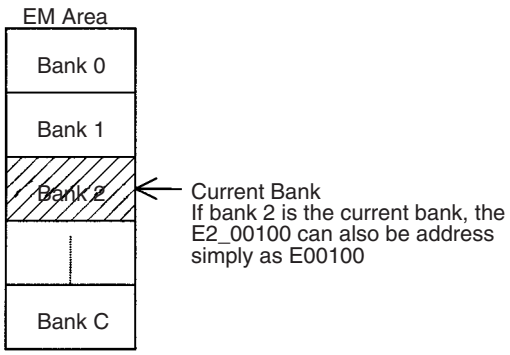
A20110: Online Editing Wait Flag



A50100 to A50115: CPU Bus Unit Restart Bits and A30200 to A30215: CPU Bus Unit Initialization Flags



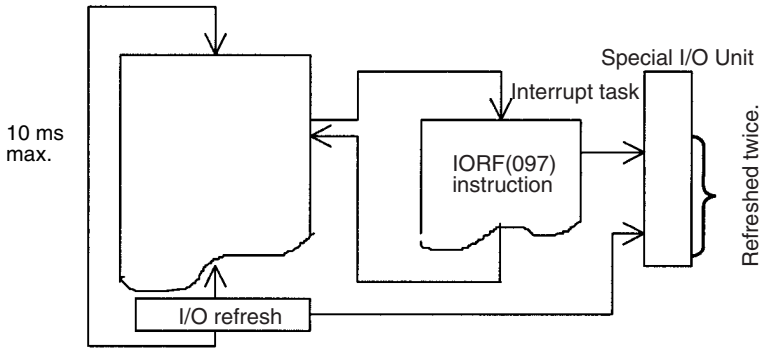
A301: Current EM Bank



A40109: Program Error

Error	Address
UM Overflow Error Flag	A29515
Illegal Instruction Flag	A29514
Distribution Overflow Error Flag	A29513
Task Error Flag	A25912
No END(001) Error Flag	A29511
Illegal Area Access Error Flag	A29510
Indirect DM/EM Addressing Error Flag	A29509
Instruction Processing Error Flag (ER Flag goes ON)	A29508

A42615: Interrupt Task Error Cause Flag



Appendix C
Memory Map of PC Memory Addresses

PC Memory Addresses

PC memory addresses are set in Index Registers (IR00 to IR15) to indirectly address I/O memory. Normally, use the MOVE TO REGISTER (MOVR(560)) and MOVE TIMER/COUNTER PV TO REGISTER (MOVRW(561)) instructions to set PC memory addresses into the Index Registers.

Some instructions, such as DATA SEARCH (SRCH(181)), FIND MAXIMUM (MAX(182)), and FIND MINIMUM (MIN(183)), output the results of processing to an Index Register to indicate an PC memory address.

There are also instructions for which Index Registers can be directly designated to use the PC memory addresses stored in them by other instructions. These instructions include DOUBLE MOVE (MOVL(498)), some symbol comparison instructions (=L,<>L, <L, >L,<=L, and >=L), DOUBLE COMPARE (CMPL(060)), DOUBLE DATA EXCHANGE (XCGL(562)), DOUBLE INCREMENT BINARY (++L(591)), DOUBLE DECREMENT BINARY (—L(593)), DOUBLE SIGNED BINARY ADD WITHOUT CARRY (+L(401)), DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY (–L(411)), SET RECORD LOCATION (SETR(635)), and GET RECORD LOCATION (GETR(636)).

The PC memory addresses all are continuous and the user must be aware of the order and boundaries of the memory areas. As reference, the PC memory addresses are provided in a table at the end of this appendix.

Note Directly setting PC memory addresses in the program should be avoided whenever possible. If PC memory addresses are set in the program, the program will be less compatible with new CPU Unit models or CPU Units for which changed have been made to the layout of the memory.

Memory Configuration

There are two classifications of the RAM memory (with battery backup) in a CJ-series CPU Unit.

Parameter Areas: These areas contain CPU Unit system setting data, such as the PC Setup, CJ-series CPU Bus Unit Setups, etc. An illegal access error will occur if an attempt is made to access any of the parameter areas from an instruction in the user program.

I/O Memory Areas: These are the areas that can be specified as operands in the instructions in user programs.

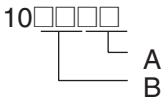
Memory Map

Classification	PC memory addresses (Hex)	User addresses	Area
Parameter areas	00000 to 0B0FF	---	PC Setup Area Registered I/O Table Area Routing Table Area CJ-series CPU Bus Unit Setup Area Real I/O Table Area Unit Profile Area
I/O memory areas	0B100 to 0B1FF	---	Reserved for system.
	0B200 to 0B7FF	---	Reserved for system.
	0B800 to 0B801	TK00 to TK31	Task Flag Area
	0B802 to 0B83F	---	Reserved for system.
	0B840 to 0B9FF	A000 to A447	Read-only Auxiliary Area
	0BA00 to 0BBFF	A448 to A959	Read/Write Auxiliary Area
	0BC00 to 0BDFF	---	Reserved for system.
	0BE00 to 0BEFF	T0000 to T4095	Timer Completion Flags
	0BF00 to 0BFFF	C0000 to C4095	Counter Completion Flags
	0C000 to 0D7FF	CIO 0000 to CIO 6143	CIO Area
	0D800 to 0D9FF	H000 to H511	Holding Area
	0DA00 to 0DDFF	---	Reserved for system.
	0DE00 to 0DFFF	W000 to W511	Work Area
	0E000 to 0EFFF	T0000 to T4095	Timer PVs
	0F000 to 0FFFF	C0000 to C4095	Counter PVs
	10000 to 17FFF	D00000 to D32767	DM Area
	18000 to 1FFFF	E0_00000 to E0_32767	EM Area bank 0
	20000 to 27FFF	E1_00000 to E1_32767	EM Area bank 1
	Etc.	Etc.	Etc.
	48000 to 4FFFF	E6_00000 to E6_32767	EM Area bank 6

Appendix D
PC Setup Coding Sheets for Programming Console

Use the following coding sheets when setting the PC Setup from a Programming Console.

Address



	Value (Hex)	Rack 0, Slot 0 I/O Response Time
A	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms
B	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms

Address

11□□□□

A

B

	Value (Hex)	Rack 0, Slot 2 I/O Response Time
A	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms
	Value (Hex)	**Rack 0, Slot 3 I/O Response Time**
B	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms

Address

29□□□□

A

B

	Value (Hex)	Rack 7, Slot 8 I/O Response Time
A	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms
	Value (Hex)	**Rack 7, Slot 9 I/O Response Time**
B	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms

Address

80□□□□

A

	Value (Hex)	IOM Hold Bit Status at Startup	Forced Status Hold Bit Status at Startup
A	C000	Retained	Retained
	8000	Retained	Cleared
	4000	Cleared	Retained
	0000	Cleared	Cleared

Address

81□□□□

A

	Display	Startup Mode
A	PRCN	Mode on Programming Console's mode switch
	PRG	PROGRAM mode
	MON	MONITOR mode
	RUN	RUN mode

Address

128□□□□

A

	Value (Hex)	Low Battery Voltage Detection	Interrupt Task Error Detection
A	C000	Do not detect	Do not detect
	8000	Do not detect	Detect
	4000	Detect	Do not detect
	0000	Detect	Detect

Address

136□□□□

A

	Value (Hex)	EM File Memory Conversion
A	0000	None
	0080	EM File Memory Enabled: Bank No. 0
	0081	EM File Memory Enabled: Bank No. 1
	0082	EM File Memory Enabled: Bank No. 2

Address

144□□□□
- A
- B

Peripheral Port

	Value (Hex)	Data bits	Stop bits	Parity
A	00	7 bits	2 bits	Even
	01	7 bits	2 bits	Odd
	02	7 bits	2 bits	None
	04	7 bits	1 bit	Even
	05	7 bits	1 bit	Odd
	06	7 bits	1 bit	None
	08	8 bits	2 bits	Even
	09	8 bits	2 bits	Odd
	0A	8 bits	2 bits	None
	0C	8 bits	1 bit	Even
	0D	8 bits	1 bit	Odd
	0E	8 bits	1 bit	None

	Value (Hex)	Communications mode
B	00	Default (Rightmost 2 digits ignored.)
	80	Host link
	82	NT link
	84	Peripheral bus
	85	Host link

Address

145□□□□
- A

Peripheral Port

	Value (Hex)	Baud rate
A	0000	9,600 bps
	0001	300 bps
	0002	600 bps
	0003	1,200 bps
	0004	2,400 bps
	0005	4,800 bps
	0006	9,600 bps
	0007	19,200 bps
	0008	38,400 bps
	0009	57,600 bps
	000A	115,200 bps

Note Set 0000 to 0009 Hex for standard NT Links and 000A Hex for high-speed NT Links.

Address

147□□□□

A

Peripheral Port

	Value (Hex)	Host link Unit No.
A	0000	No. 0
	0001	No. 1
	0002	No. 2
	to	to
	001F	No. 31

Address

150□□□□

A

Peripheral Port

	Value (Hex)	NT Link Mode Maximum Unit No.
A	0000	No. 0
	0001	No. 1
	to	to
	0007	No. 7

Address

160□□□□

A

B

RS-232C Port

	Value (Hex)	Data bits	Stop bits	Parity
A	00	7 bits	2 bits	Even
	01	7 bits	2 bits	Odd
	02	7 bits	2 bits	None
	04	7 bits	1 bit	Even
	05	7 bits	1 bit	Odd
	06	7 bits	1 bit	None
	08	8 bits	2 bits	Even
	09	8 bits	2 bits	Odd
	0A	8 bits	2 bits	None
	0C	8 bits	1 bit	Even
	0D	8 bits	1 bit	Odd
	0E	8 bits	1 bit	None

	Value (Hex)	Communications mode
B	00	Default (Rightmost 2 digits ignored.)
	80	Host link
	82	NT link
	83	No-protocol
	84	Peripheral bus
	85	Host link

Address

161□□□□

A

RS-232C Port

	Value (Hex)	Baud rate
A	0000	9,600 bps
	0001	300 bps
	0002	600 bps
	0003	1,200 bps
	0004	2,400 bps
	0005	4,800 bps
	0006	9,600 bps
	0007	19,200 bps
	0008	38,400 bps
	0009	57,600 bps
	000A	115,200 bps

Note Set 0000 to 0009 Hex for standard NT Links and 000A Hex for high-speed NT Links.

Address

162□□□□

A

RS-232C Port

	Value (Hex)	No-protocol mode delay
A	0000	0 ms
	0001	10 ms
	to	to
	270F	99,990 ms

Address

163□□□□

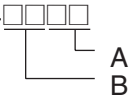
A

RS-232C Port

	Value (Hex)	Host link Unit No.
A	0000	No. 0
	0001	No. 1
	0002	No. 2
	to	to
	001F	No. 31

Address

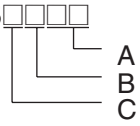
164□□□□



	Value (Hex)	No-protocol Mode End Code
A	00	00
	to	to
	FF	FF
	Value (Hex)	**No-protocol Mode Start Code**
B	00	00
	to	to
	FF	FF

Address

165□□□□



RS-232C Port

	Value (Hex)	No-protocol Mode reception data volume
A	00	256
	01	1
	to	to
	FF	256
	Value (Hex)	**No-protocol Mode end code setting**
B	0	None (Specify the amount of data being received)
	1	Yes (Specify the end code)
	2	End code is set to CF+LF
	Value (Hex)	**No-protocol Mode start code setting**
C	0	None
	1	Yes

Address

166□□□□

RS-232C Port

	Value (Hex)	Maximum Unit No. in NT Link Mode
A	0000	No. 0
	0001	No. 1
	to	to
	0007	No. 7

Address

195□□□□

	Value (Hex)	Scheduled interrupt time unit
A	0000	10 ms
	0001	1.0 ms

Address

197□□□□

A

	Value (Hex)	Instruction Error Operation
A	0000	Continue operation
	8000	Stop operation

Address

208□□□□

A

	Value (Hex)	Minimum Cycle Time
A	0000	Cycle time not fixed
	0001	Cycle time fixed: 1 ms
	to	to
	7D00	Cycle time fixed: 32,000 ms

Address

209□□□□

A

	Value (Hex)	Watch Cycle Time
A	0000	Default: 1,000 ms (1 s)
	8001	10 ms
	to	to
	8FA0	40,000 ms

Address

218□□□□

A

	Value (Hex)	Fixed Peripheral Servicing Time
A	0000	Default (4% of the cycle time)
	8000	00 ms
	8001	0.1 ms
	to	to
	80FF	25.5 ms

Address

219□□□□

A

B

	Value (Hex)	Slice Time for Peripheral Servicing
A	00	Disable Peripheral Servicing Priority Mode.
	01 to FF	0.1 to 25.5 ms (in 0.1-ms increments)
	Value (Hex)	**Slice Time for Program Execution**
B	00	Disable Peripheral Servicing Priority Mode.
	05 to FF	5 to 255 (in 1-ms increments)

Address

220□□□□

A

B

	Value (Hex)	Unit/Port for Priority Servicing
A	00	Disable Peripheral Servicing Priority Mode.
	10 to 1F	CPU Bus Unit unit number (0 to 15) + 10 Hex
	20 to 7F	CPU Special I/O Unit unit number (0 to 96) + 20 Hex
	FC	RS-232C port
	FD	Peripheral port
	Value (Hex)	**Unit/Port for Priority Servicing**
B	00	Disable Peripheral Servicing Priority Mode.
	10 to 1F	CPU Bus Unit unit number (0 to 15) + 10 Hex
	20 to 7F	CPU Special I/O Unit unit number (0 to 96) + 20 Hex
	FC	RS-232C port
	FD	Peripheral port

Address

221□□□□

A

B

	Value (Hex)	Unit/Port for Priority Servicing
A	00	Disable Peripheral Servicing Priority Mode.
	10 to 1F	CPU Bus Unit unit number (0 to 15) + 10 Hex
	20 to 7F	CPU Special I/O Unit unit number (0 to 96) + 20 Hex
	FC	RS-232C port
	FD	Peripheral port
	Value (Hex)	**Unit/Port for Priority Servicing**
B	00	Disable Peripheral Servicing Priority Mode.
	10 to 1F	CPU Bus Unit unit number (0 to 15) + 10 Hex
	20 to 7F	CPU Special I/O Unit unit number (0 to 96) + 20 Hex
	FC	RS-232C port
	FD	Peripheral port

Address

222□□□□

Not used.

A

	Value (Hex)	Unit/Port for Priority Servicing
A	00	Disable Peripheral Servicing Priority Mode.
	10 to 1F	CPU Bus Unit unit number (0 to 15) + 10 Hex
	20 to 7F	CPU Special I/O Unit unit number (0 to 96) + 20 Hex
	FC	RS-232C port
	FD	Peripheral port

Address

225□□□□

└── A

	Value (Hex)	Power OFF Interrupt Task	Power OFF Detection Delay Time
A	0000	Disabled	0 ms
	0001		1 ms
	to		to
	000A		10 ms
	8000	Enabled	0 ms
	8001		1 ms
	to		to
	800A		10 ms

Address

226□□□□

└── A

	Value (Hex)	Special I/O Unit Cyclic Refreshing 0: Yes 1: No															
		Unit number															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
	to																
	FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Addresses 227 through 231 are the same as 226.

Appendix E
Connecting to the RS-232C Port on the CPU Unit

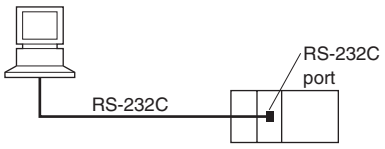
Connection Examples

The wiring diagrams for connecting to the RS-232C port are provided in this appendix. In actual wiring, we recommend the use of shielded twisted-pair cables and other methods to improve noise resistance. Refer to *Recommended Wiring Methods* later in this appendix for recommended wiring methods.

Connections to Host Computers

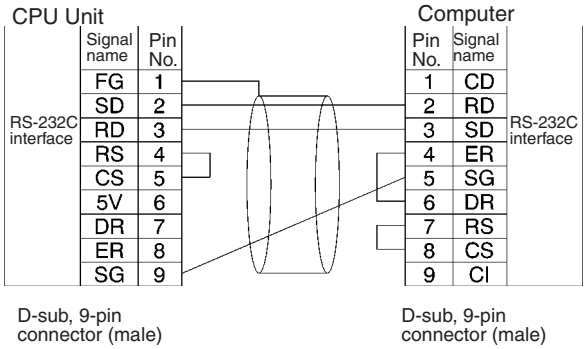
Note Connections to a computer running the CX-Programmer are the same as those shown here.

1:1 Connections via RS-232C Port

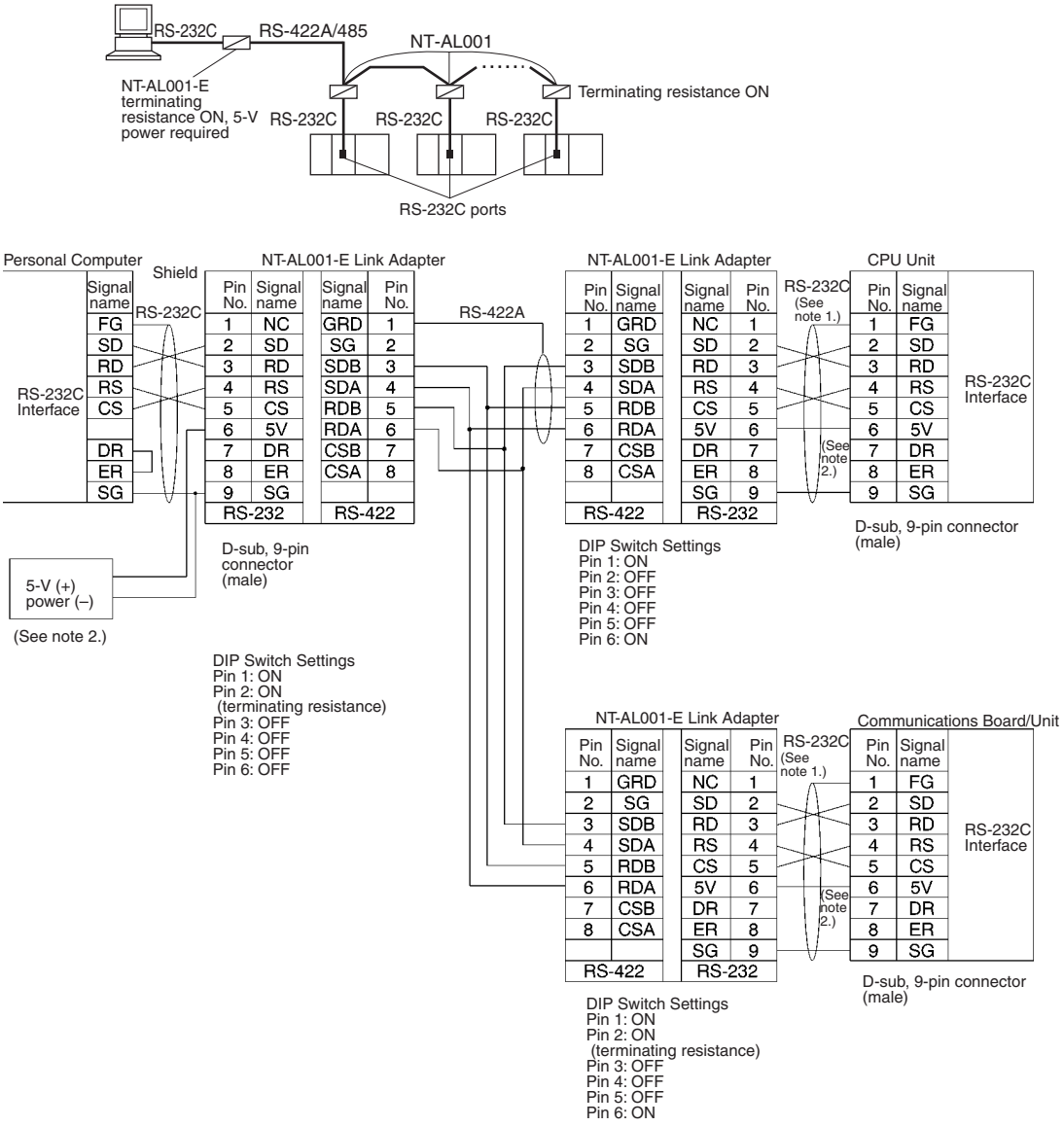


Note The maximum cable length for an RS-232C connection is 15 m. RS-232C communications specifications, however, do not cover transmissions at 19.2 Kbps. Refer to documentation of the device being connected when using this baud rate.

IBM PC/AT or Compatible Computer



1:N Connections via RS-232C Port

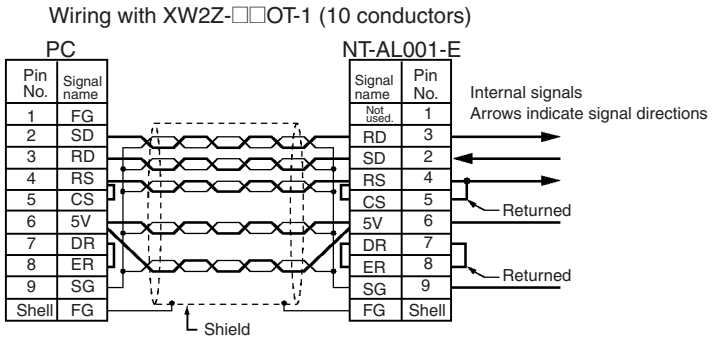


Note 1. We recommend using the following NT-AL001-E Link Adapter Connecting Cables to connect to NT-AL001-E Link Adapters.

XW2Z-070T-1: 0.7 m
XW2Z-200T-1: 2 m

The recommended cables should be wired as shown below. Each signal wire should be twisted with the SG (signal ground) wire and placed in a shielded cable to prevent the effects of noise in noise-prone environments. The 5-V wires can also be twisted with the SG wire to increase noise immunity.

Although this wiring is different from that shown in the example above, it can be used to increase noise immunity if required.



2. When the NT-AL001-E Link Adapter is connected to the RS-232C port on the CPU Unit, 5 V is supplied from pin 6, eliminating the need for a 5-V power supply.
3. Do not use the 5-V power from pin 6 of the RS-232C port for anything but the NT-AL001-E Link Adapter. Using this power supply for any other external device may damage the CPU Unit or the external device.
4. The XW1Z-□□0T-1 Cable is designed to connect the NT-AL001-E and contains special wiring for the CS and RS signals. Do not use this cable for any other application. Connecting this cable to other devices can damage them.

DIP Switch Settings on the NT-AL001-E Link Adapter

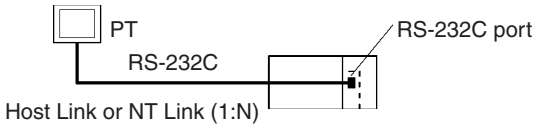
There is a DIP switch on the NT-AL001-E Link Adapter that is used to set RS-422A/485 communications parameters. Set the DIP switch as required for the serial communications mode according to the following table.

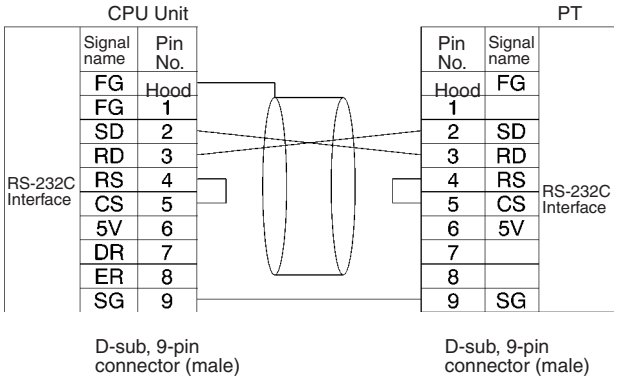
Pin	Function	Default setting
1	Not used. (Leave set to ON.)	ON
2	Internal terminating resistance setting. ON: Terminating resistance connected. OFF: Terminating resistance not connected.	ON
3	2-wire/4-wire setting Both pins ON: 2-wire communications Both pins OFF: 4-wire communications	OFF
4		OFF
5	Communications mode (See note.) Both pins OFF: Always send. 5 OFF/6 ON: Send when RS-232C's CS is high. 5 ON/6 OFF: Send when RS-232C's CS is low.	ON
6		OFF

Note Turn OFF pin 5 and turn ON pin 6 when connected to a CJ-series CPU Unit.

Connection Example to Programmable Terminal (PT)

Direct Connection from RS-232C to RS-232C





- Communications Mode: Host Link (unit number 0 only for Host Link)
  NT Link (1:N, N = 1 Unit only)
- OMRON Cables with Connectors:
  XW2Z-200T-1: 2 m
  XW2Z-500T-1: 5 m

Recommended Wiring Methods

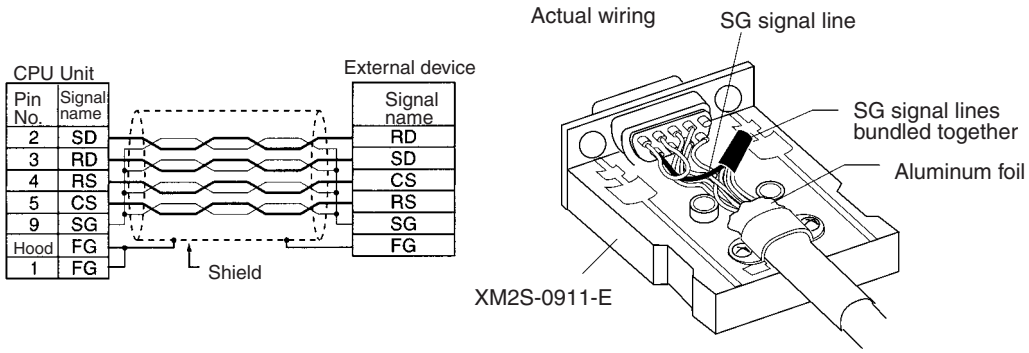
We recommend the following wiring methods for RS-232C, especially in environment prone to noise.

1. Use shielded twisted-pair cable for communications cables. The following RS-232C cables are recommended.

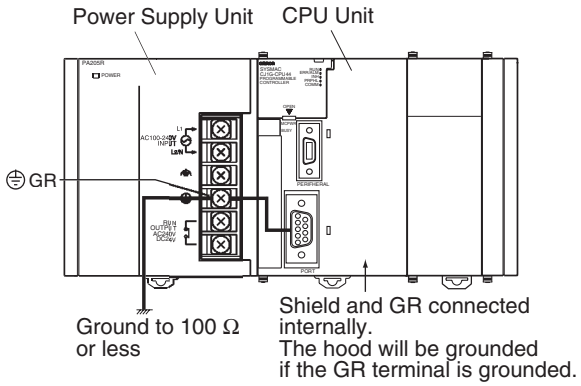
Model	Manufacturer
UL2464 AWG28×5P IFS-RVV-SB (UL approved) AWG28×5P IFVV-SB (not UL approved)	Fujikura Ltd.
UL2464-SB (MA) 5P×28AWG (7/0.127) (UL approved) CO-MA-VV-SB 5P×28AWG (7/0.127) (not UL approved)	Hitachi Cable, Ltd.

2. Use a twisted-pair cable for each signal line and SG (signal ground) to connect the CPU Unit to a communications partner. Also, bundle all the SG lines at the Unit and at the other device and connect them together.
3. Connect the shield line of the communications cable to the hood (FG) of the RS-232C connector at the Unit. Also, ground the protective earth (GR) terminal of the Power Supply Units on the CPU Rack and the CJ-series Expansion Racks to a resistance of 100 Ω or less. The following example shows connecting

SD-SG, RD-SG, RS-SG, and CS-SG for Serial Communications Mode using a twisted-pair cable using the peripheral bus.



Note The hood (FG) is internally connected to the protective earth (GR) terminal on the Power Supply Unit through the CPU Rack or CJ-series Expansion Rack. FG can thus be connected by connecting the protective earth (GR) terminal on the Power Supply Unit. The hood (FG) is also electrically connected to pin 1 (FG), but the connection resistance between the shield and the FG is smaller for the hood. To reduce contact resistance between the hood (FG) and the FG, connect the shield both to the hood (FG) and to pin 1 (FG).



Wiring Connectors

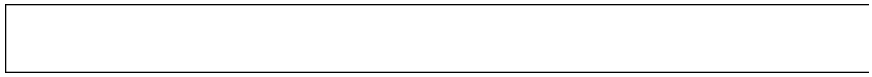
Use the following procedures to wire connectors.

Preparing the Cable

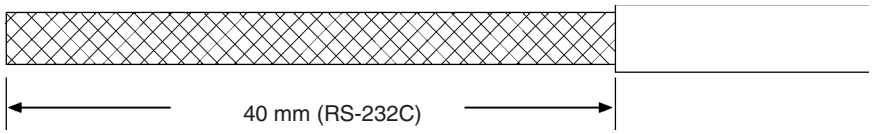
Lengths for steps in the procedure are provided in the diagrams.

Connecting the Shield Line to the Hood (FG)

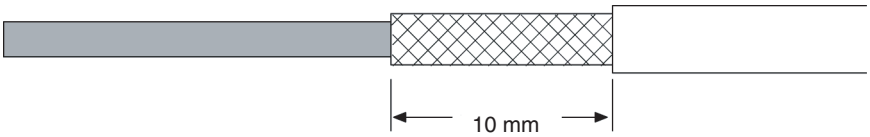
1. Cut the cable to the required length, leaving leeway for wiring and laying the cables.



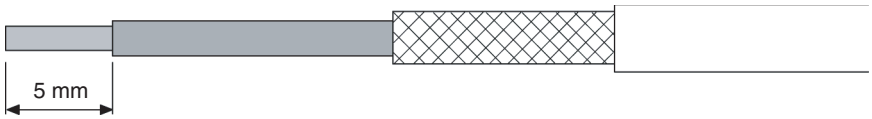
2. Use a razor blade to cut away the sheath, being careful not to damage the braiding.



3. Use scissors to cut away all but 10 mm of the exposed braiding.



4. Use wire strippers to remove the insulation from the end of each wire.



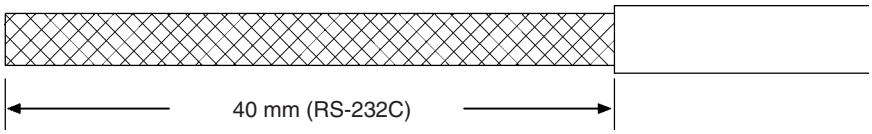
5. Fold the braiding back over the end of the sheath.

6. Wrap aluminum foil tape over the top of the braiding for one and a half turns.

Not Connecting the Shield to the Hood (FG)

1. Cut the cable to the required length, leaving leeway for wiring and laying the cables.

2. Use a razor blade to cut away the sheath, being careful not to damage the braiding.



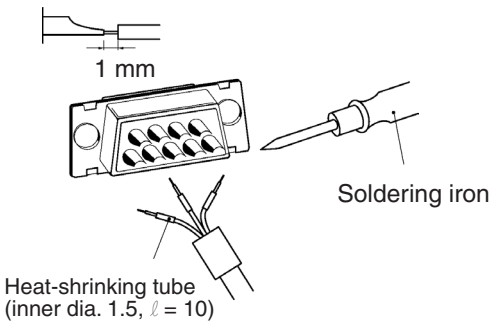
3. Use scissors to cut away the exposed braiding.

4. Use wire strippers to remove the insulation from the end of each wire.

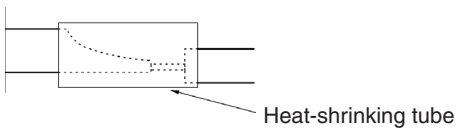
5. Wrap electrician's tape over the top and end of the the cut sheath.

Soldering

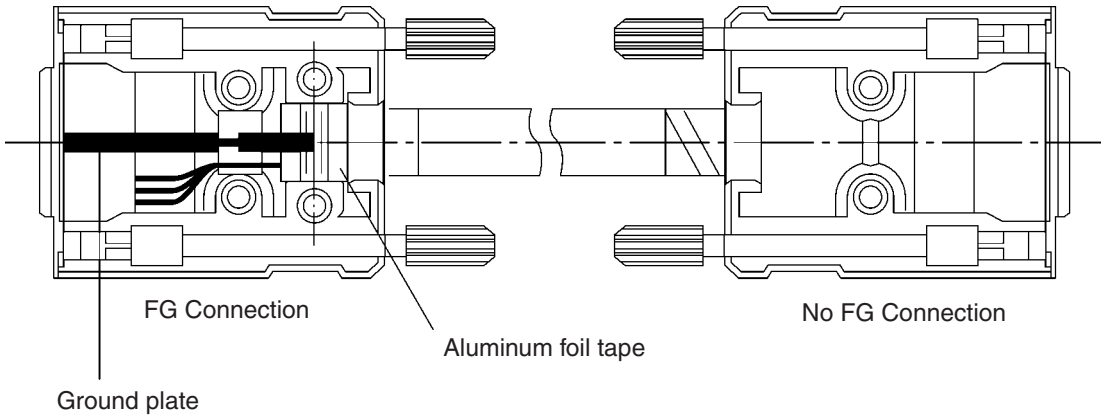
1. Place heat-shrinking tubes over all wires.
2. Pre-solder all wires and connector terminals.
3. Solder the wires.



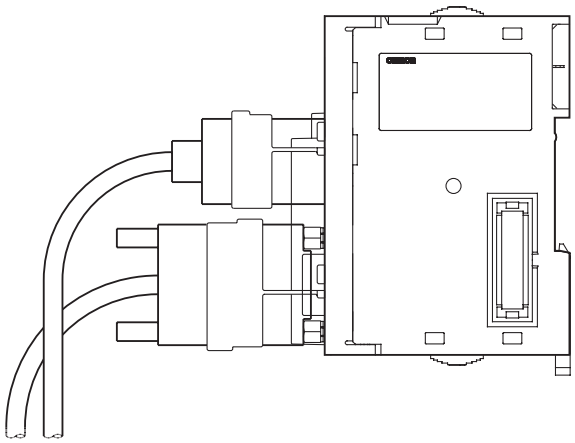
4. Move the heat-shrinking tubes onto the soldered area and shrink them into place.



Assembling the Hood
Assemble the connector hood as shown.



Connections to the CPU Unit



- Always turn OFF the power supply to the PC before connecting or disconnecting communications cables.
- Tighten the communications connector attachment screws to 0.4 N•m.

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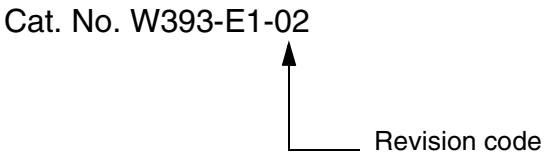
Revision History

A manual revision code appears as a suffix to the catalog number on the front cover of the manual.



The following table outlines the changes made to the manual during each revision. Page numbers refer to the previous version.

Revision code	Date	Revised content
01	April 2001	Original production
02	October 2001	New products added to the manual, including the new High-speed CPU Units (CJ1-H CPU Units). (Extensive changes too numerous to list.)

OMRON

Authorized Distributor:

Cat. No. W393-E1-02 Note: Specifications subject to change without notice Printed in Japan